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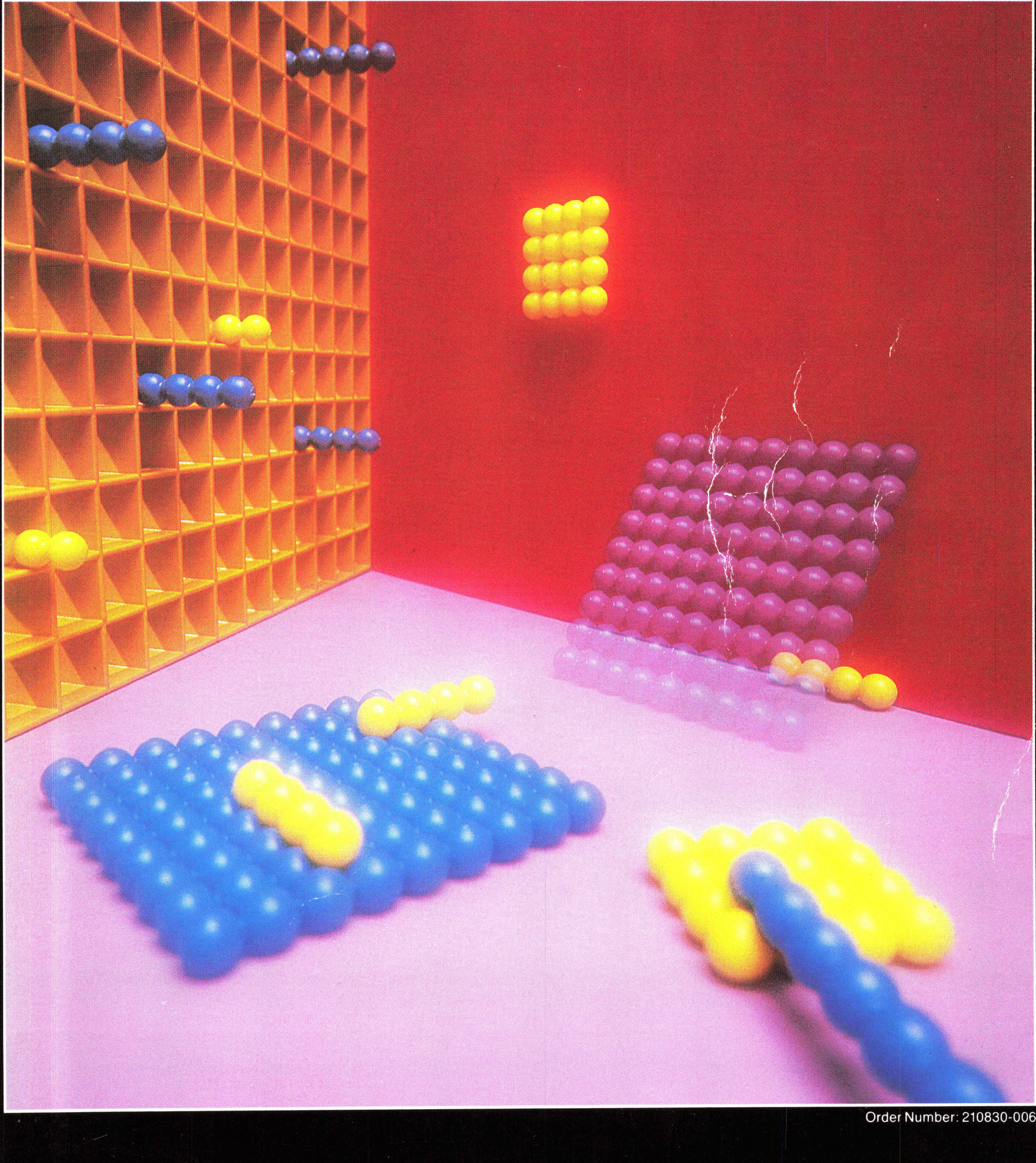

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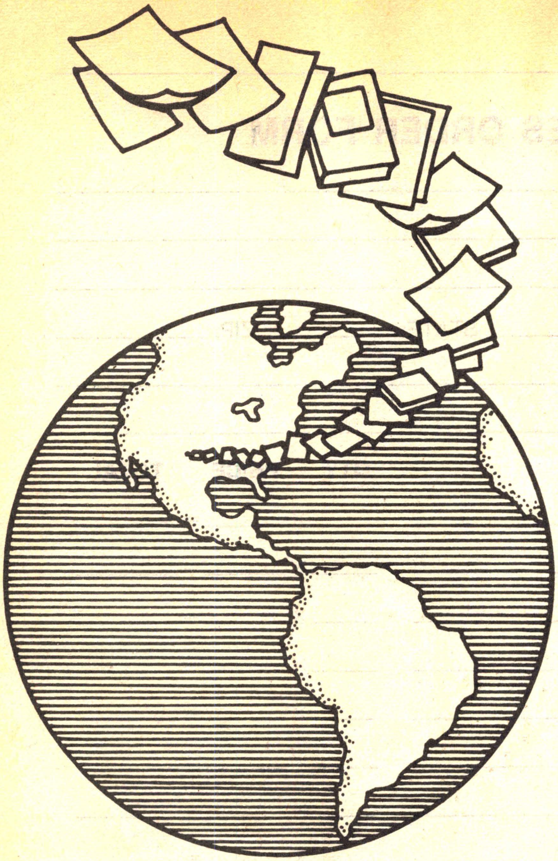

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MEMORY COMPONENTS HANDBOOK

1987

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Memory Overview

1

CHAPTER 1: MEMORY OVERVIEW

MEMORY BACKGROUND AND DEVELOPMENT

Only fifteen years ago MOS LSI memories were little more than laboratory curiosities. Any engineer brave enough to design with semiconductor memories had a simple choice of which memory type to use. The 2102 Static RAM for ease of use or the 1103 Dynamic RAM for low power were the only two devices available. Since then, the memory market has come a long way, the types of memory devices have proliferated, and more than 3,000 different memory devices are now available. Consequently, the designer has many to choose from but the choice is more difficult, and therefore, effective memory selection is based on matching memory characteristics to the application.

Memory devices can be divided into two main categories: volatile and non-volatile. Volatile memories retain their data only as long as power is applied. In a great many applications this limitation presents no problem. The generic term random access memory (RAM) has come to be almost synonymous with a volatile memory in which there is a constant rewriting of stored data.

In other situations, however, it is imperative that a non-volatile device be used because it retains its data whether or not power is applied. An example of this requirement would be retaining data during a power failure. (Tape and disk storage are also non-volatile memories but are not included within the scope of this book, which confines itself to solid-state technologies in IC form.)

Thus, when considering memory devices, it's helpful to see how the memory in computer systems is segmented by applications and then look at the state-of-the-art in these cases.

Read/Write Memory

First examine read/write memory (RAM), which permits the access of stored memory (reading) and the ability to alter the stored data (writing).

Before the advent of solid-state read/write memory, active data (data being processed) was stored and retrieved from non-volatile core memory (a magnetic-storage technology). Solid-state RAMs solved the size and power consumption problems associated with core, but added the element of volatility. Because RAMS lose their memory when you turn off their power, you must leave systems on all the time, add battery backup or store important data on a non-volatile medium before the power goes down.

Despite their volatility, RAMs have become very popular, and an industry was born that primarily fed computer systems' insatiable appetites for higher bit capacities and faster access speeds.

RAM Types

Two basic RAM types have evolved since 1970. Dynamic RAMs are noted for high capacity, moderate speeds and low power consumption. Their memory cells are basically charge-storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted by the RAM's sense line as a logical 1 or 0. Because of the charge's natural tendency to distribute itself into a lower energy-state configuration, however, dynamic RAMs require periodic charge refreshing to maintain data storage.

Traditionally, this requirement has meant that system designers had to implement added circuitry to handle dynamic RAM subsystem refresh. And at certain times, refresh procedures made the RAM unavailable for writing and reading; the memory's control circuitry had to arbitrate access. LSI dynamic memory controllers reduce the refresh requirement to a minimal design by offering a monolithic controller solution.

Where users are less concerned with space and cost than with speed and reduced complexity, the second RAM type—static RAMs—generally prove best. Unlike their dynamic counterparts, static RAMs store ones and zeros using traditional flip-flop logic-gate configurations. They are faster and require no refresh. A user simply addresses the static RAM, and after a very brief delay, obtains the bit stored in that location. Static devices are also simpler to design with than dynamic RAMs, but the static cell's complexity puts these non-volatile chips far behind dynamics in bit capacity per square mil of silicon.

Read-Only Memory

Another memory class, read-only memory (ROM), is similar to RAM in that a computer addresses it and then retrieves data stored at that address. However, ROM includes no mechanism for altering the data stored at that address—hence, the term read only.

ROM is basically used for storing information that isn't subject to change—at least not frequently. Unlike RAM, when system power goes down, ROM retains its contents.

ROM devices became very popular with the advent of microprocessors. Most early microprocessor applications were dedicated systems; the system's program was fixed and stored in ROM. Manipulated data could vary and was therefore stored in RAM. This application split caused ROM to be commonly called program storage, and RAM, data storage.

The first ROMs contained cell arrays in which the sequence of ones and zeros was established by a metallization interconnect mask step during fabrication. Thus, users had to supply a ROM vendor with an interconnect program so the vendor could complete the mask and build the ROMs. Set-up charges were quite high—in fact, even prohibitive unless users planned for large volumes of the same ROM.

To offset this high set-up charge, manufacturers developed a user-programmable ROM (or PROM). The first such devices used fusible links that could be melted or programmed with a special hardware system.

Once programmed, a PROM was just like a ROM. If the program was faulty, the chip had to be discarded. But, PROMs furnished a more cost-effective way to develop program memory or firmware for low-volume purposes than did ROMs.

As one alternative to fusable-link programming, Intel pioneered an erasable MOS-technology PROM (termed an EPROM) that used charge-storage programming. It came in a standard ceramic DIP package but had a window that permitted die exposure to light. When the chip was exposed to ultraviolet light, high energy photons could collide with the EPROM's electrons and scatter them at random, thus erasing the memory.

The EPROM was not intended for use in read/write applications, but it proved very useful in research and development for prototypes, where the need to alter the program several times is quite common. Indeed, the EPROM market originally consisted almost exclusively of development labs. As the fabrication process became mature, however, and volumes increased, EPROM's lower prices made them attractive even for medium-volume production-system applications.

Intel currently supplies EPROMs in all densities ranging from 16K to 1 Megabit.

Another ROM technology advance occurred in 1980 with the introduction of Intel's 2816—a 16K ROM that's user programmable and electrically erasable. Thus, instead of removing it from its host system and placing it under ultraviolet light to erase its program, the 2816 can be reprogrammed in its socket. Moreover, single bits or entire bytes can be erased in one operation instead of erasing the entire chip.

Such E^{2}PROMs (for electrically erasable programmable ROM) are opening up new applications. In point-of-sale terminals, for example, each terminal connects to a central computer but each can also handle moderate amounts of local processing. An E^{2}PROM can store discount information to be automatically figured in during a sales transaction. Should the discount change, the central computer can update each terminal via telephone lines by reprogramming that portion of the E^{2}PROM.

In digital instrumentation, an instrument could become self-calibrating using an E^{2}PROM. Should the instrument's calibration drift outside specification limits, the system could employ a built-in diagnostic to reprogram a parametric setting in an E^{2}PROM and bring the calibration back within limits.

Today, Intel is supplying 64K bit E^{2}PROM memories, providing a cost effective solution for updating information in the system.

APPLICATIONS OF MEMORY DEVICES

Besides the particular characteristics of each device that has been discussed, there are a number of other factors to consider when choosing a memory product, such as cost, power consumption, performance, memory architecture and organization, and size of the memory. Each of these factors plays an important role in the final selection process.

Performance

Generally, the term performance relates to how fast the device can operate in a given system environment. This parameter is usually rated in terms of the access time. Fast SRAMs can provide access times as fast as 20 ns, while the fastest DRAM cannot go much beyond the 100 ns mark. A bipolar PROM has an access time of 35 ns. RAM and PROM access is usually controlled by a signal most often referred to as Chip Select ($\overline{CS}$). $\overline{CS}$ often appears in device specifications. In discussing access times, it is important to remember that in SRAMs and PROMs, the access time equals the cycle time of the system whereas in DRAMs, the access time is always less than the cycle time.

Cost

There are many ramifications to consider when evaluating cost. Cost can be spread over factors such as

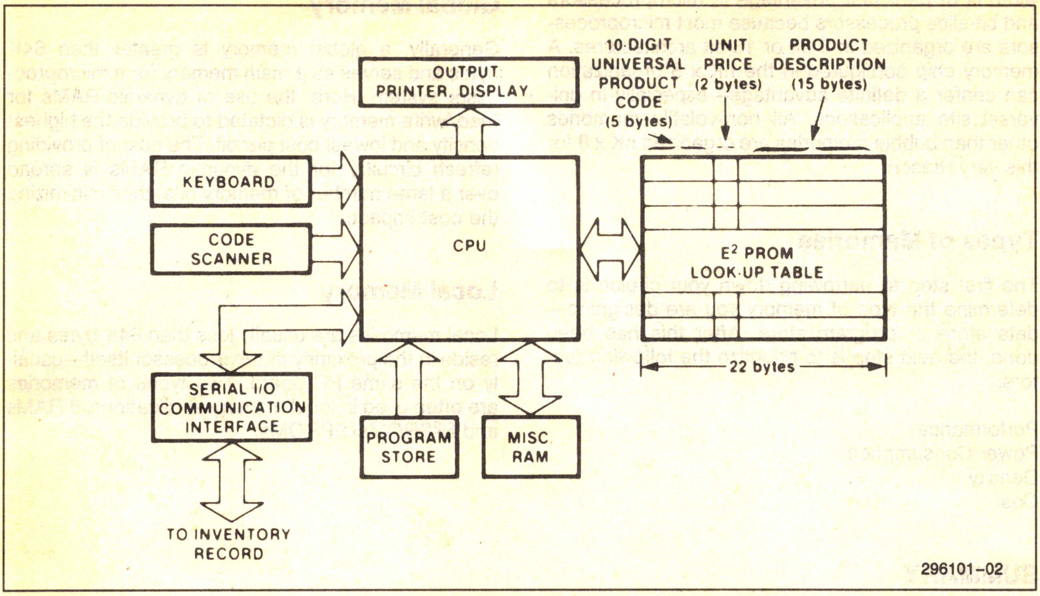


Figure 1. Typical E²PROM Application

design-in time, cost per device, cost per bit, size of memory, power consumption, etc.

Cost of design time is proportional to design complexity. For example, SRAMs generally require less design-in time than DRAMs because there is no refresh circuitry to consider. Conversely, the DRAM provides the lowest cost per bit because of its higher packing density.

Memory Size

Memory size is generally specified in the number of bytes (a byte is a group of eight bits). The memory size of a system is usually segmented depending upon the general equipment category. Computer mainframes and most of today's minicomputers use blocks of RAM substantially beyond 64K bytes—usually in the hundreds of thousands of bytes. For this size of memory, the DRAM has a significantly lower cost per bit. The additional costs of providing the refresh and timing circuitry are spread over many bits.

The microprocessor user generally requires memory sizes ranging from 2K bytes up to 64K bytes. In memories of this size, the universal site concept allows maximum flexibility in memory design.

Power Consumption

Power consumption is important because the total power required for a system directly affects overall cost. Higher power consumption requires bigger power supplies, more cooling, and reduced device density per board—all affecting cost and reliability. All things considered, the usual goal is to minimize power. Many memories now provide automatic power-down. With today's emphasis on saving energy and reducing cost, the memories that provide these features will gain an increasingly larger share of the market.

In some applications, extremely low power consumption is required, such as battery operation. For these applications, the use of devices made by the CMOS technology have a distinct advantage over the NMOS products. CMOS devices offer power savings of several magnitudes over NMOS. Non-volatile devices such as E²PROMs are usually independent of power problems in these applications.

Power consumption also depends upon the organization of the device in the system. Organization usually refers to the width of the memory word. At the time of their inception, memory devices were organized as nK x 1 bits. Today, they are available in various configurations such as 4K x 1, 16K x 1, 64K x 1, 1K x 4, 2K x 8, etc. As the device width increases, fewer devices are required to configure a given memory word—although the total number of bits remains constant. The wider organization can provide significant savings in power consumption, because a fewer number of devices are required to be powered up for access to a given memory word. In addition, the board layout design is simpler due to fewer traces and better layout advantages. The wider width is of particular advantage in microprocessors and bit-slice processors because most microprocessors are organized in 8-bit or 16-bit architectures. A memory chip configured in the nK x 8 organization can confer a definite advantage—especially in universal site applications. All non-volatile memories other than bubble memories are organized nK x 8 for this very reason.

Types of Memories

The first step to narrowing down your choice is to determine the type of memory you are designing—data store or program store. After this has been done, the next step is to prioritize the following factors:

Performance
Power Consumption
Density
Cost

Global Memory

Generally, a global memory is greater than 64K bytes and serves as a main memory for a microprocessor system. Here, the use of dynamic RAMs for read/write memory is dictated to provide the highest density and lowest cost per bit. The cost of providing refresh circuitry for the dynamic RAMs is spread over a large number of memory bits, thus minimizing the cost impact.

Local Memory

Local memories are usually less than 64K bytes and reside in the proximity of the processor itself—usually on the same PC board. Two types of memories are often used in local memory applications: 5 RAMs and E^2PROMs/EPROMs.

SUMMARY

Table 1 provides a summary of the various memory devices that have been discussed.

Table 1. Segmentation of Memory Devices

Operating From	Read Speed		Write Speed		Size		Removable (Archive)	System Level
	Fast	Slow	Fast	Slow	Small	Large		
Mass		Disk		Disk		Disk	Disk	Add on RAM
Boot	EPROM		N/A	N/A	All(1)			N/A
Monitor	EPROM		N/A	N/A	All			N/A
Buffer	Bytewide		Bytewide	N/A	All	X1		Add in RAM
Diagnostics	E^2/EPROM/ RAM		Bytewide	E^2PROM	All	All(2)	Disk	N/A
Operating System	EPROM		N/A	N/A	All	X1	Disk	Add in/ Add on RAM
APP/PGM/ Data Store	E^2EPROM/ RAM		Bytewide X1	E^2PROM	All	X1	Disk	Add in/ Add on RAM

NOTES:
1. E^2/EPROM Bytewides
2. X1 DRAM Disk

Memory Technologies

2

CHAPTER 2:
INTEL MEMORY TECHNOLOGIES

Most of this handbook is devoted to techniques and information to help you design and implement semiconductor memory in your application or system. In this section, however, the memory chip itself will be examined and the processing technology required to turn a bare slice of silicon into high performance memory devices is described. The discussion has been limited to the basics of MOS (Metal Oxide Semiconductor) technologies as they are responsible for the overwhelming majority of memory devices manufactured at Intel.

There are three major MOS technology families—PMOS, NMOS, and CMOS (Figure 1). They refer to the channel type of the MOS transistors made with the technology. PMOS technologies implement p-channel transistors by diffusing p-type dopants (usually Boron) into an n-type silicon substrate to form the source and drain. P-channel is so named because the channel is comprised of positively charged carriers. NMOS technologies are similar, but use n-type dopants (normally phosphorus or arsenic) to make n-channel transistors in p-type silicon substrates. N-channel is so named because the channel is comprised of negatively charged carriers. CMOS or Complementary MOS technologies combine both p-channel and n-channel devices on the same silicon. Either p- or n-type silicon substrates can be used, however, deep areas of the opposite doping type (called wells) must be defined to allow fabrication of the complementary transistor type.

Most of the early semiconductor memory devices, like Intel's pioneering 1103 dynamic RAM and 1702 EPROM were made with PMOS technologies. As higher speeds and greater densities were needed, most new devices were implemented with NMOS. This was due to the inherently higher speed of n-channel charge carriers (electrons) in silicon along with improved process margins. The majority of MOS memory devices in production today are fabricated with NMOS technologies. CMOS technology has begun to see widespread commercial use in memory devices. It allows for very low power devices and these have been used for battery operated or battery back-up applications. Historically, CMOS has been slower than any NMOS device. Recently, however, CMOS technology has been improved to produce higher speed devices. Up to now, the extra cost processing required to make both transistor types has kept CMOS memories limited to those areas where the technology's special characteristics would justify the extra cost. In the future, the learning curve for high performance CMOS costs will make a larger and larger number of memory devices practical in CMOS.

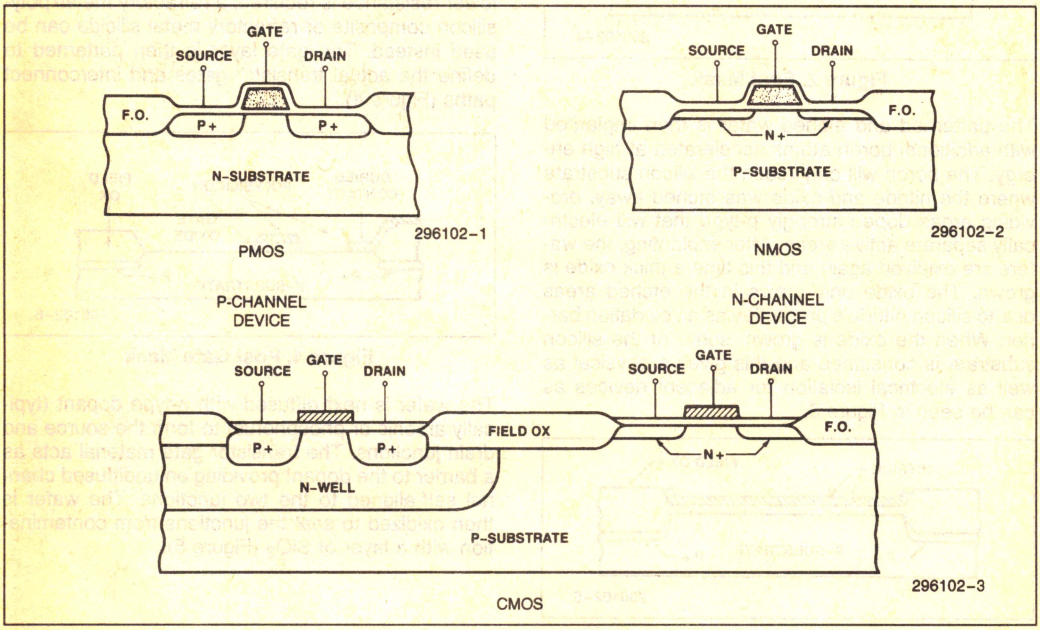


Figure 1. MOS Process Cross-sections

In the following section, the basic fabrication sequence for an HMOS circuit will be described. HMOS is a high performance n-channel MOS process developed by Intel for 5V single supply circuits. HMOS, along with its evolutionary counterparts HMOS II and HMOS III, CHMOS and CHMOS II (and their variants), comprise the process family responsible for most of the memory components produced by Intel today.

The MOS IC fabrication process begins with a slice (or wafer) of single crystal silicon. Typically, it's 100 or 150 millimeter in diameter, about a half millimeter thick, and uniformly doped p-type. The wafer is then oxidized in a furnace at around 1000°C to grow a thin layer of silicon dioxide (SiO_2) on the surface. Silicon nitride is then deposited on the oxidized wafer in a gas phase chemical reactor. The wafer is now ready to receive the first pattern of what is to become a many layered complex circuit. The pattern is etched into the silicon nitride using a process known as photolithography, which will be described in a later section. This first pattern (Figure 2) defines the boundaries of the active regions of the IC, where transistors, capacitors, diffused resistors, and first level interconnects will be made.

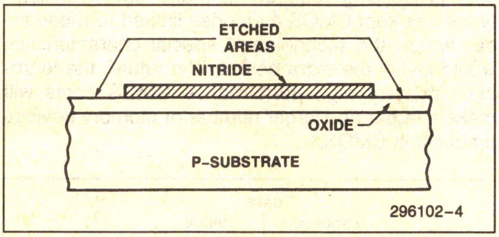


Figure 2. First Mask

The patterned and etched wafer is then implanted with additional boron atoms accelerated at high energy. The boron will only reach the silicon substrate where the nitride and oxide was etched away, providing areas doped strongly p-type that will electrically separate active areas. After implanting, the wafers are oxidized again and this time a thick oxide is grown. The oxide only grows in the etched areas due to silicon nitride's properties as an oxidation barrier. When the oxide is grown, some of the silicon substrate is consumed and this gives a physical as well as electrical isolation for adjacent devices as can be seen in Figure 3.

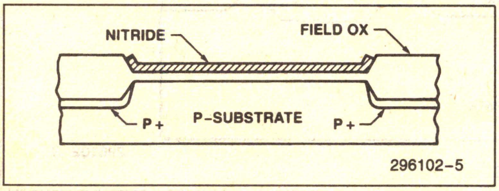


Figure 3. Post Field Oxidation

Having fulfilled its purpose, the remaining silicon nitride layer is removed. A light oxide etch follows taking with it the underlying first oxide but leaving the thick (field) oxide.

Now that the areas for active transistors have been defined and isolated, the transistor types needed can be determined. The wafer is again patterned and then if special characteristics (such as depletion mode operation) are required, it is implanted with dopant atoms. The energy and dose at which the dopant atoms are implanted determines much of the transistor's characteristics. The type of the dopant provides for depletion mode (n-type) or enhancement mode (p-type) operation.

The transistor types defined, the gate oxide of the active transistors are grown in a high temperature furnace. Special care must be taken to prevent contamination or inclusion of defects in the oxide and to ensure uniform consistent thickness. This is important to provide precise, reliable device characteristics. The gate oxide layer is then masked and holes are etched to provide for direct gate to diffusion ("buried") contacts where needed.

The wafers are now deposited with a layer of gate material. This is typically poly crystaline silicon ("poly") which is deposited in a gas phase chemical reactor similar to that used for silicon nitride. The poly is then doped (usually with phosphorus) to bring the sheet resistance down to 10–20 Ω/square. This layer is also used for circuit interconnects and if a lower resistance is required, a refractory metal/polysilicon composite or refractory metal silicide can be used instead. The gate layer is then patterned to define the actual transistor gates and interconnect paths (Figure 4).

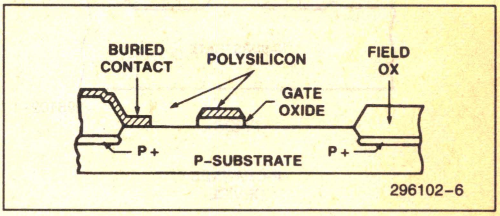


Figure 4. Post Gate Mask

The wafer is next diffused with n-type dopant (typically arsenic or phosphorus) to form the source and drain junctions. The transistor gate material acts as a barrier to the dopant providing an undiffused channel self-aligned to the two junctions. The wafer is then oxidized to seal the junctions from contamination with a layer of SiO_2 (Figure 5).

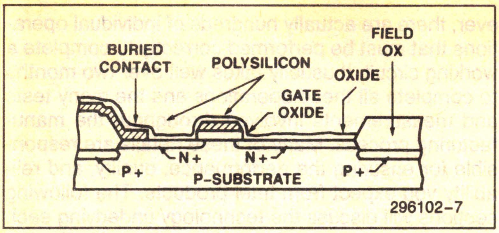

BURIED CONTACT
POLYSILICON
FIELD OX
OXIDE
GATE OXIDE
N+
N+
P+
P+
P-SUBSTRATE
296102-7

Figure 5. Post Oxidation

A thick layer glass is then deposited over the wafer to provide for insulation and sufficiently low capacitance between the underlying layers and the metal interconnect signals. (The lower the capacitance, the higher the inherent speed of the device.) The glass layer is then patterned with contact holes and placed in a high temperature furnace. This furnace step smooths the glass surface and rounds the contact edges to provide uniform metal coverage. Metal (usually aluminum or aluminum/silicon) is then deposited on the wafer and the interconnect patterns and external bonding pads are defined and etched (Figure 6). The wafers then receive a low temperature (approximately 500°C) alloy that insures good ohmic contact between the Al and diffusion or poly.

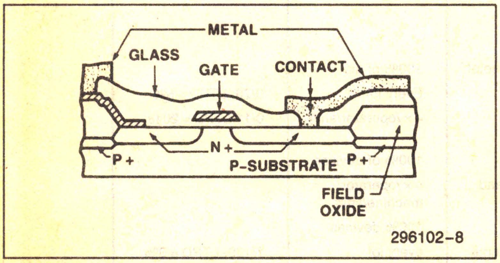
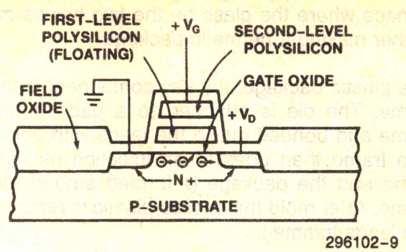

METAL
GLASS
GATE
CONTACT
N+
P+
P-SUBSTRATE
P+
FIELD OXIDE
296102-8

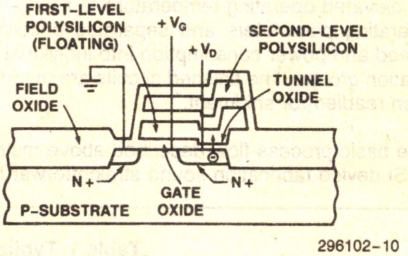
Figure 6. Complete Circuit (without passivation)

At this point the circuit is fully operational, however, the top metal layer is very soft and easily damaged by handling. The device is also susceptible to contamination or attack from moisture. To prevent this the wafers are sealed with a passivation layer of silicon nitride or a silicon and phosphorus oxide composite. Patterning is done for the last time opening up windows only over the bond pads where external connections will be made.

This completes basic fabrication sequence for a single poly layer process. Double poly processes such as those used for high density Dynamic RAMs, EPROMs, and E^{2}PROMs follow the same general process flow with the addition of gate, poly deposition, doping, and interlayer dielectric process modules required for the additional poly layer (Figure 7). These steps are performed right after the active areas have been defined (Figure 3) providing the capacitor or floating gate storage nodes on those devices.


FIRST-LEVEL POLYSILICON (FLOATING)
+V_G
SECOND-LEVEL POLYSILICON
GATE OXIDE
FIELD OXIDE
+V_D
N+
P-SUBSTRATE
296102-9

EPROM CELL


FIRST-LEVEL POLYSILICON (FLOATING)
+V_G
+V_D
SECOND-LEVEL POLYSILICON
TUNNEL OXIDE
FIELD OXIDE
N+
N+
GATE OXIDE
P-SUBSTRATE
296102-10

E^{2}PROM CELL

Figure 7. Double Poly Structure

After fabrication is complete, the wafers are sent for testing. Each circuit is tested individually under conditions designed to determine which circuits will operate properly both at low temperature and at conditions found in actual operation. Circuits that fail these tests are inked to distinguish them from good circuits. From here the wafers are sent from assembly where they are sawed into individual circuits with a paper-thin diamond blade. The inked circuits are then separated out and the good circuits are sent on for packaging.

Packages fall into two categories—hermetic and non-hermetic. Hermetic packages are Cerdip, where two ceramic halves are sealed with a glass fritt, or ceramic with soldered metal lids. An example of hermetic package assembly is shown in Table 1. Non-hermetic packages are molded plastics.

The ceramic package has two parts, the base, which has the leads and die (or circuit) cavity, and the metal lid. The base is placed on a heater block and a metal alloy preform is inserted. The die is placed on top of the preform which bonds it to the package. Once attached, wires are bonded to the circuit and then connected to the leads. Finally the package is placed in a dry inert atmosphere and the lid is soldered on.

The cerdip package consists of a base, lead frame, and lid. The base is placed on a heater block and the lead frame placed on top. This sets the lead frame in glass attached to the base. The die is then attached and bonded to the leads. Finally the lid is placed on the package and it is inserted in a seal furnace where the glass on the two halves melt together making a hermetic package.

In a plastic package, the key component is the lead frame. The die is attached to a pad on the lead frame and bonded out to the leads with gold wires. The frame then goes to an injection molding machine and the package is formed around the lead frame. After mold the excess plastic is removed and the leads trimmed.

After assembly, the individual circuits are retested at an elevated operating temperature to assure critical operating parameters and separated according to speed and power consumption into individual specification groups. The finished circuits are marked and then readied for shipment.

The basic process flow described above may make VLSI device fabrication sound straightforward, however, there are actually hundreds of individual operations that must be performed correctly to complete a working circuit. It usually takes well over two months to complete all these operations and the many tests and measurements involved throughout the manufacturing process. Many of these details are responsible for ensuring the performance, quality, and reliability you expect from Intel products. The following sections will discuss the technology underlying each of the major process elements mentioned in the basic process flow.

PHOTOLITHOGRAPHY

The photo or masking technology is the most important part of the manufacturing flow if for no other reason than the number of times it is applied to each wafer. The manufacturing process gets more complex in order to make smaller and higher performance circuits. As this happens the number of mask

Table 1. Typical Hermetic Package Assembly

Flow	Process/Materials	Typical Item	Frequency	Criteria
	Wafer			
	Die saw, wafer break			
	Die wash and plate			
	Die visual inspection	Passivation, metal	100% of die	
	QA gate		Every lot	0/76, LTPD = 5%
	Die attach (Process monitor)	Wet out	4 x /operator/shift	0/11 LTPD = 20%
	Post die attach visual		100% of devices	
	Wire bond (Process monitor)	Orientation, lead dressing, etc.	4 x /operator/ machine/shift	
	Post bond inspection		100% devices	
	QA gate	All previous items	every lot	1/129, LTPD = 3%
	Seal and Mark (Process monitor)	Cap align, glass integrity, moisture	4 x /furnace/shift	0/15, LTPD = 15%
	Temp cycle		10 x to mil std. 883 cond. C	1/11, LTPD = 20%
	Hermeticity check (Process monitor)	F/G leak	100% devices	
	Lead Trim (Process monitor)	Burrs, etc. (visual) Fine leak	4 x /station/shift 2 x /station/shift	0/15, LTPD = 15% 1/129, LTPD = 3%
	External visual	Solder voids, cap alignment, etc.	100% devices	
1.	QA gate	All previous items	All lots	1/129, LTPD = 3%
	Class test (Process monitor)	Run standards (good and reject) Calibrate every system using "autover" program	Every 48 hrs.	
	Mark and Pack			
2.	Final QA	(See attached)		

296102-11

NOTES:

1. Units for assembly reliability monitor.
2. Units for product reliability monitor.

ing steps increases, the features get smaller, and the tolerance required becomes tighter. This is largely because the minimum size of individual pattern elements determine the size of the whole circuit, effecting its cost and limiting its potential complexity. Early MOS IC's used minimum geometries (lines or spaces) of 8–10 microns (1 micron = 10^{-6} meter ≅ 1/25,000 inch). The n-channel processes of the mid 1970's brought this down to approximately 5 microns, and today minimum geometries are less than 2 microns in production. This dramatic reduction in feature size was achieved using the newer high resolution photo resists and optimizing their processing to match improved optical printing systems.

A second major factor in determining the size of the circuit is the registration or overlay error. This is how accurately one pattern can be aligned to a previous one. Design rules require that space be left in all directions according to the overlay error so that unrelated patterns do not overlap or interfere with one another. As the error space increases the circuit size increases dramatically. Only a few years ago standard alignment tolerances were ≥ ±2 microns; now advanced Intel processes have reduced this dramatically due mostly to the use of advanced projection and step and repeat exposure equipment.

The wafer that is ready for patterning must go through many individual steps before that pattern is complete. First the wafer is baked to remove moisture from its surface and is then treated with chemicals that ensure good resist adhesion. The thick photoresist liquid is then applied and the wafer is spun flat to give a uniform coating, critical for high resolution. The wafer is baked at a low temperature to solidify the resist into gel. It is then exposed with a machine that aligns a mask with the new pattern on it to a previously defined layer. The photo-resist will replicate this pattern on the wafer.

Negative working resists are polymerized by the light and the unexposed resist can be rinsed off with solvents. Positive working resists use photosensitive polymerization inhibitors that allow a chemically reactive developer to remove the exposed areas. The positive resists require much tighter control of exposure and development but yield higher resolution patterns than negative resistance systems.

The wafer is now ready to have its pattern etched. The etch procedure is specialized for each layer to be etched. Wet chemical etchants such as hydrofluoric acid for silicon oxide or phosphoric acid for aluminum are often used for this. The need for smaller features and tighter control of etched dimensions is increasing the use of plasma etching in fabrication. Here a reactor is run with a partial vacuum into which etchant gases are introduced and an electrical field is applied. This yields a reactive plasma which etches the required layer.

The wafer is now ready for the next process step. Its single journey through the masking process required the careful engineering of mechanics, optics, organic chemistry, inorganic chemistry, plasma chemistry, physics, and electronics.

DIFFUSION

The picture of clean room garbed operators tending furnace tubes glowing cherry red is the one most often associated with IC fabrication. These furnace operations are referred to collectively as diffusion because they employ the principle of sold state diffusion of matter to accomplish their results. In MOS processing, there are three main types of diffusion operations: predeps, drives, and oxidations.

Predeposition, or "predep," is an operation where a dopant is introduced into the furnace from a solid, liquid, or gaseous source and at the furnace temperature (usually 900°C–1200°C) a saturated solution is formed at the silicon surface. The temperature of the furnace, the dopant atom, and rate of introduction are all engineered to give a specific dose of the dopant on the wafer. Once this is completed the wafer is given a drive cycle where the dopant left at the surface by the predep is driven into the wafer by high temperatures. These are generally at different temperatures than the predeps and are designed to give the required junction depth and concentration profile.

Oxidation, the third category, is used at many steps of the process as was shown in the process flow. The temperature and oxidizing ambient can range from 800°C to 1200°C and from pure oxygen to mixtures of oxygen and other gases to steam depending on the type of oxide required. Gate oxides require high dielectric breakdown strength for thin layers (between 0.01 and 0.1 micron) and very tight control over thickness (typically ±0.005 micron or less than ±1/5,000,000 inch), while isolation oxides need to be quite thick and because of this their dielectric breakdown strength per unit thickness is much less important.

The properties of the diffused junctions and oxides are key to the performance and reliability of the finished device so the diffusion operations must be extremely well controlled for accuracy, consistency and purity.

ION IMPLANT

Intel's high performance products require such high accuracy and repeatability of dopant control that even the high degree of control provided by diffusion operations is inadequate. However, this limitation has been overcome by replacing critical predeps with ion implantation. In ion implantation, ionized dopant atoms are accelerated by an electric field and implanted directly into the wafer. The acceleration potential determines the depth to which the dopant is implanted.

The charged ions can be counted electrically during implantation giving very tight control over dose. The ion implanters used to perform this are a combination of high vacuum system, ion source, mass spectrometer, linear accelerator, ultra high resolution current integrator, and ion beam scanner. You can see that this important technique requires a host of sophisticated technologies to support it.

THIN FILMS

Thin film depositions make up most of the features on the completed circuit. They include the silicon nitride for defining isolation, polysilicon for the gate and interconnections, the glass for interlayer dielectric, metal for interconnection and external connections, and passivation layers. Thin film depositions are done by two main methods: physical deposition and chemical vapor deposition. Physical deposition is most common for deposition metal. Physical depositions are performed in a vacuum and are accomplished by vaporizing the metal with a high energy electron beam and redepositing it on the wafer or by sputtering it from a target to the wafer under an electric field.

Chemical vapor deposition can be done at atmospheric pressure or under a moderate vacuum. This type of deposition is performed when chemical gases react at the wafer surface and deposit a solid film of the reaction product. These reactors, unlike their general industrial counterparts, must be controlled on a microscale to provide exact chemical and physical properties for thin films such as silicon dioxide, silicon nitride, and polysilicon.

The fabrication of modern memory devices is a long, complex process where each step must be monitored, measured and verified. Developing a totally new manufacturing process for each new product or even product line takes a long time and involves significant risk. Because of this, Intel has developed process families, such as HMOS, on which a wide variety of devices can be made. These families are scalable so that circuits need not be totally redesigned to meet your needs for higher performance.(1) They are evolutionary (HMOS I, HMOS II, HMOS III, CHMOS) so that development time of new processes and products can be reduced without compromising Intel's commitment to consistency, quality, and reliability.

The manufacture of today's MOS memory devices requires a tremendous variety of technologies and manufacturing techniques, many more than could be mentioned here. Each requires a team of experts to design, optimize, control and maintain it. All these people and thousands of others involved in engineering, design, testing and production stand behind Intel's products.

Because of these extensive requirements, most manufacturers have not been able to realize their needs for custom circuits on high performance, high reliability processes. To address this Intel's expertise in this area is now available to industry through the silicon foundry. Intel supplies design rules and support to design and debug circuits. This includes access to Intel's n-well CHMOS technology. Users of the foundry can now benefit from advanced technology without developing processes and IC manufacturing capability themselves.

(1) R. Pashley, K. Kokkonen, E. Boleky, R. Jecmen, S. Liu, and W. Owen, "H-MOS Scales Traditional Devices to Higher Performance Level," *Electronics*, August 18, 1977.

Static RAMs (Random Access Memories)

3

intel®

2114A
1024 x 4 BIT STATIC RAM

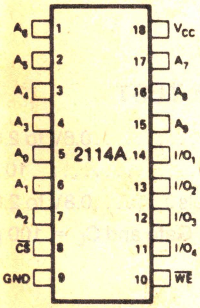
	2114AL-1	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	100	120	150	200	200	250
Max. Current (mA)	40	40	40	40	70	70

- **HMOS II Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **High Reliability Plastic or Cerdip**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**

The Intel 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS II, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

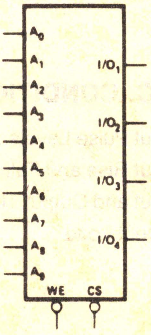
The 2114A is designed for memory applications where the high performance and high reliability of HMOS II, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is assembled in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 WE
2114A

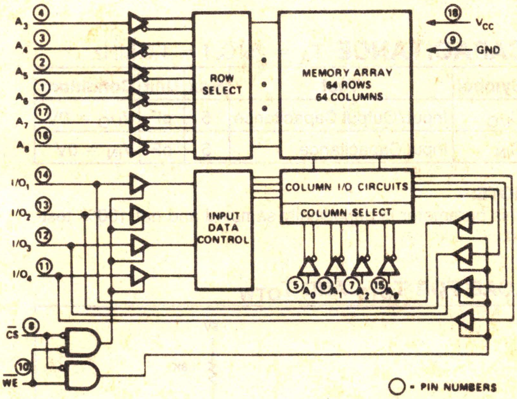
290083-1

Pin Configuration


A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
I/O1
I/O2
I/O3
I/O4
WE
CS

290083-2

Logic Symbol


A3 4
A4 3
A5 2
A6 1
A7 17
A8 16
ROW SELECT
MEMORY ARRAY
64 ROWS
64 COLUMNS
18 VCC
9 GND
I/O1 14
I/O2 13
I/O3 12
I/O4 11
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
5 A0
6 A1
7 A2
15 A9
CS 8
WE 10
○ - PIN NUMBERS

290083-3

Block Diagram

Pin Names

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

© Intel Corporation, 1986

Order Number: 290083-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin
With Respect to Ground .... −3.5V to +7V
Power Dissipation 1.0W
D.C. Output Current .... 5 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted

Symbol	Parameter	2114AL-1/L-2/L-3/L-4			2114A-4/-5			Unit	Conditions
		Min	Typ(1)	Max	Min	Typ(1)	Max		
$\lvert I_{LI} \rvert$	Input Load Current (All Input Pins)		0.01	1			1	μA	V_{IN} = 0V to 5.5V
$\lvert I_{LO} \rvert$	I/O Leakage Current		0.1	10			10	μA	$\overline{CS} = V_{IH}$ $V_{I/O}$ = 0V to 5.5V
I_{CC}	Power Supply Current		25	40		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	4.0	9.0		4.0	9.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	−2.0	−2.5		−2.0	−2.5		mA	V_{OH} = 2.4V
I_{OS}(2)	Output Short Circuit Current			40			40	mA	V_{OUT} = GND

NOTES:

1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 1 second.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE:
This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels .... 0.8V to 2.0V
Input Rise and Fall Times .... 10 ns
Input and Output Timing Levels .... 0.8V to 2.0V
Output Load .... 1 TTL Gate and C_L = 100 pF

LOAD FOR T_{OTD} AND T_{OTW}

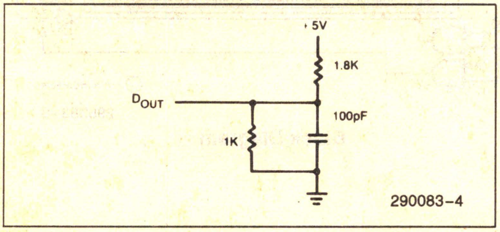


Figure 1

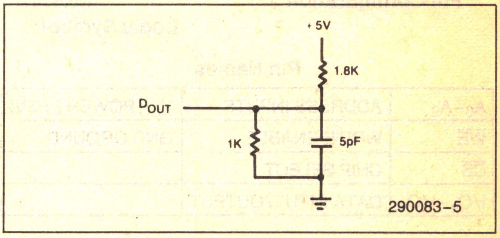


Figure 2

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted.

READ CYCLE(1)

Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		200		250		ns
t_A	Access Time		100		120		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		70		70		85	ns
t_{CX}(3)	Chip Selection to Output Active	10		10		10		10		10		ns
t_{OTD}(3)	Output 3-state from Deselection		30		35		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		15		15		ns

WRITE CYCLE(2)

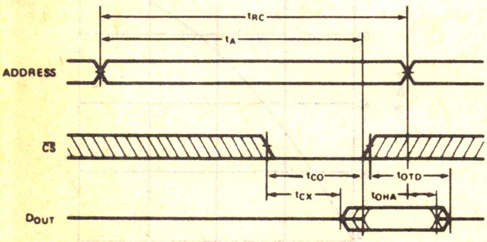
Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		200		250		ns
t_W	Write Time	75		75		90		120		135		ns
t_{WR}	Write Release Time	0		0		0		0		0		ns
t_{OTW}(3)	Output 3-state from Write		30		35		40		50		60	ns
t_{DW}	Data to Write Time Overlap	70		70		90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns

NOTES:

1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
3. Measured at ±500 mV with 1 TTL Gate and C_L = 5.00 pF.

WAVEFORMS

READ CYCLE(3)

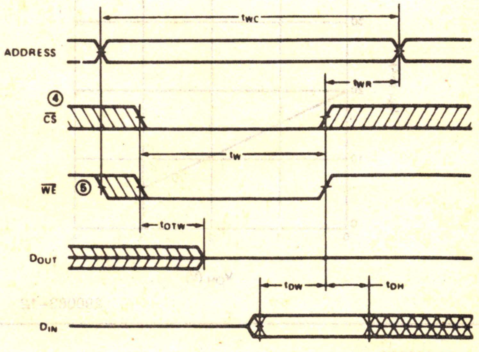


290083-6

NOTES:

3. $\overline{WE}$ is high for a Read Cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
5. $\overline{WE}$ must be high during all address transitions.

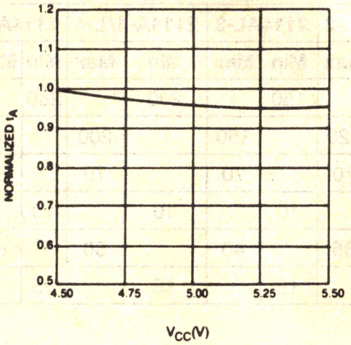
WRITE CYCLE



290083-7

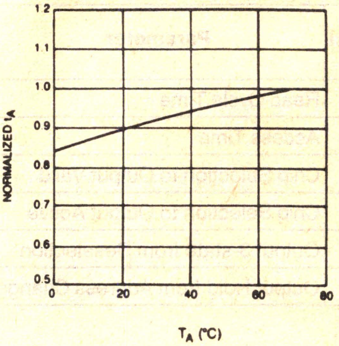
TYPICAL D.C. AND A.C. CHARACTERISTICS

Normalized Access Time vs Supply Voltage



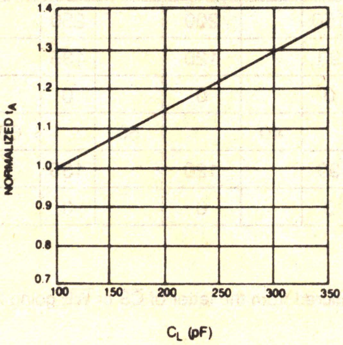
290083-8

Normalized Access Time vs Ambient Temperature



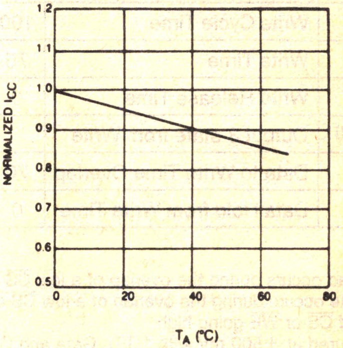
290083-9

Normalized Access Time vs Output Load Capacitance



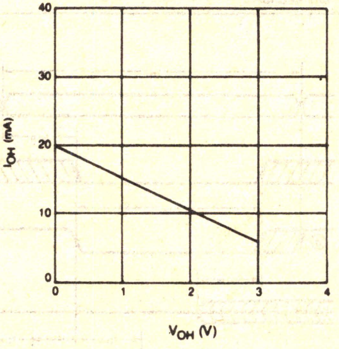
290083-10

Normalized Power Supply Current vs Ambient Temperature



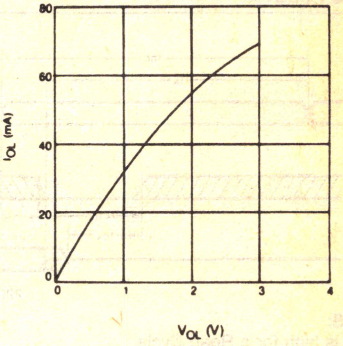
290083-11

Output Source Current vs Output Voltage



290083-12

Output Sink Current vs Output Voltage



290083-13

2115A, 2125A FAMILY
HIGH SPEED 1K x 1 BIT STATIC RAM

	2115AL, 2125AL	2115A, 2125A	2115AL-2, 2125AL-2	2115A-2, 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **Pin Compatible to 93415A (2115A) and 93425A (2125A)**
- **Fan-Out of 10 TTL (2115A Family)**
  — 16 mA Output Sink Current
- **Low Operating Power Dissipation**
  — Max. 0.39 mW/Bit (2115AL, 2125AL)
- **TTL Inputs and Outputs**
- **Available in EXPRESS**
  — Standard Temperature Range
  — Extended Temperature Range
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**
  (See Packaging Spec. Order #231369)

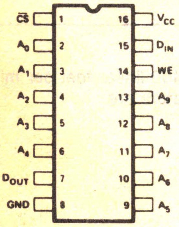
The Intel 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout—in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively offer complete compatibility with a 20% reduction in maximum power dissipation.

The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

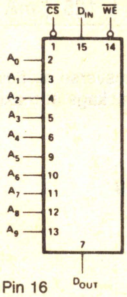
The 2115A and 2125A families are fabricated with Intel's N-channel MOS Silicon Gate Technology.

Pin Configuration


$\overline{CS}$ 1
A0 2
A1 3
A2 4
A3 5
A4 6
DOUT 7
GND 8
16 VCC
15 DIN
14 WE
13 A9
12 A8
11 A7
10 A6
9 A5

290084-1

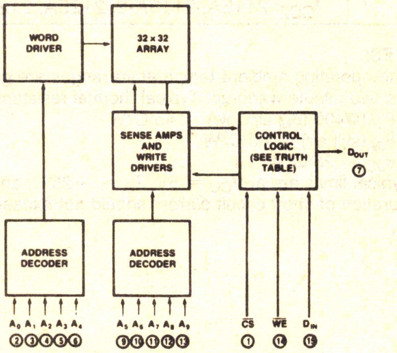
Logic Symbol


$\overline{CS}$
DIN
$\overline{WE}$
1
15
14
A0 2
A1 3
A2 4
A3 5
A4 6
A5 9
A6 10
A7 11
A8 12
A9 13
7
DOUT

V_{CC} = Pin 16
GND = Pin 8

290084-2

Block Diagram


WORD DRIVER
32 x 32 ARRAY
SENSE AMPS AND WRITE DRIVERS
CONTROL LOGIC (SEE TRUTH TABLE)
DOUT ⑦
ADDRESS DECODER
ADDRESS DECODER
A0 A1 A2 A3 A4
②③④⑤⑥
A5 A6 A7 A8 A9
⑨⑩⑪⑫⑬
$\overline{CS}$ ①
$\overline{WE}$ ⑭
DIN ⑮

290084-3

Pin Names

$\overline{CS}$	Chip Select
A_0 to A_9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Truth Table

Inputs			Output 2115A Family	Output 2125A Family	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

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Order Number: 290084-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −10°C to +85°C
Storage Temperature . . . . −65°C to +150°C
All Output or Supply Voltage . . . . −0.5V to +7V
All Input Voltages . . . . −0.5V to +5.5V
D.C. Output Current . . . . 20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS(1,2) $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

Symbol	Test	Min	Typ	Max	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	$I_{OL} = 16$ mA
V_{OL2}	2125A Family Output Low Voltage			0.45	V	$I_{OL} = 7$ mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., $V_{IN} = 0.4V$
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., $V_{IN} = 4.5V$
$\lvert I_{CEX}\rvert$	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., $V_{OUT} = 4.5V$
$\lvert I_{OFF}\rvert$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., $V_{OUT} = 0.5V/2.4V$
I_{OS}(3)	2125A Family Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	$I_{OH} = -3.2$ mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA}(@400 f_{PM} air flow) = 45°C/W
   θ_{JA}(still air) = 60°C/W
   θ_{JC} = 25°C/W
2. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A FAMILY A.C. CHARACTERISTICS(1,2) $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

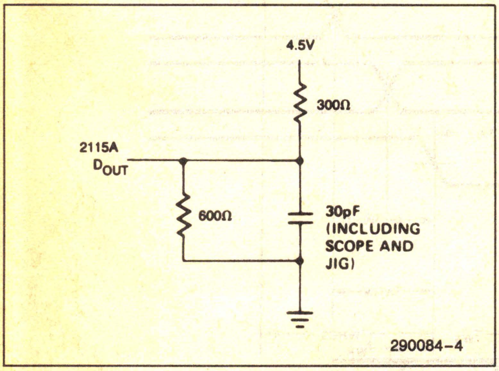
READ CYCLE

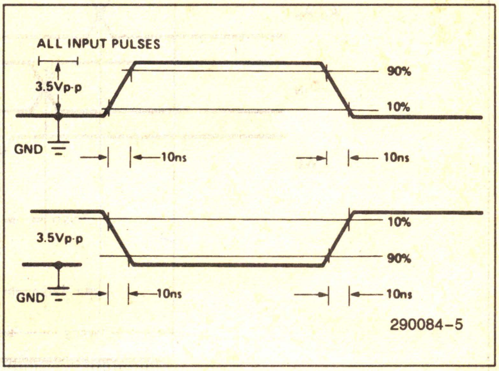
Symbol	Test	2115AL Limits			2115A Limits			2115AL-2 Limits			2115A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	Address Access Time		30	45		30	45		40	70		40	70	ns
t_{OH}	Previous Read Data Valid after Change of Address	10			10			10			10			ns

WRITE CYCLE

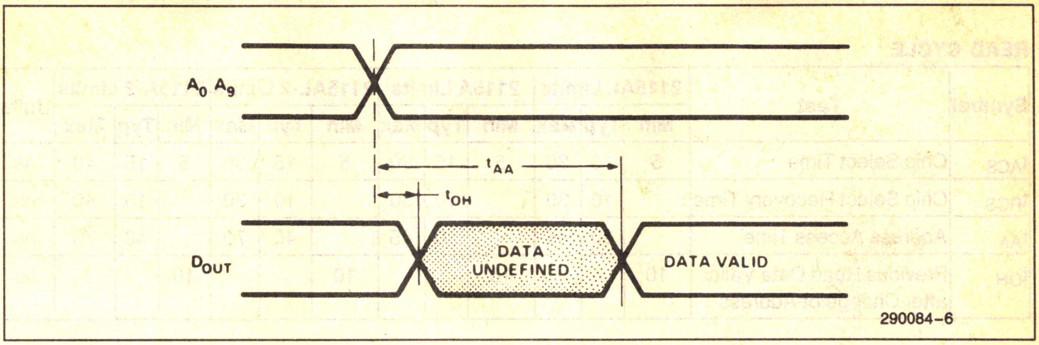
Symbol	Test	2115AL Limits			2115A Limits			2115AL-2 Limits			2115A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time after Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS


4.5V
300Ω
2115A
DOUT
600Ω
30pF (INCLUDING SCOPE AND JIG)
290084-4

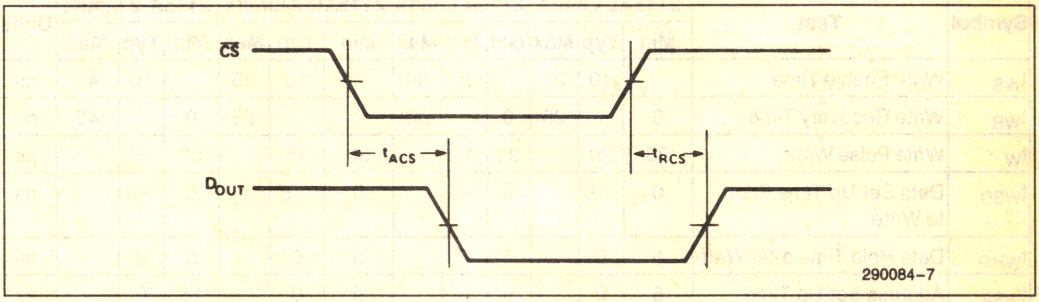

ALL INPUT PULSES
3.5Vp-p
90%
10%
GND
10ns
10ns
3.5Vp-p
10%
90%
GND
10ns
10ns
290084-5

READ CYCLE


A0 A9
tAA
tOH
DOUT
DATA UNDEFINED
DATA VALID

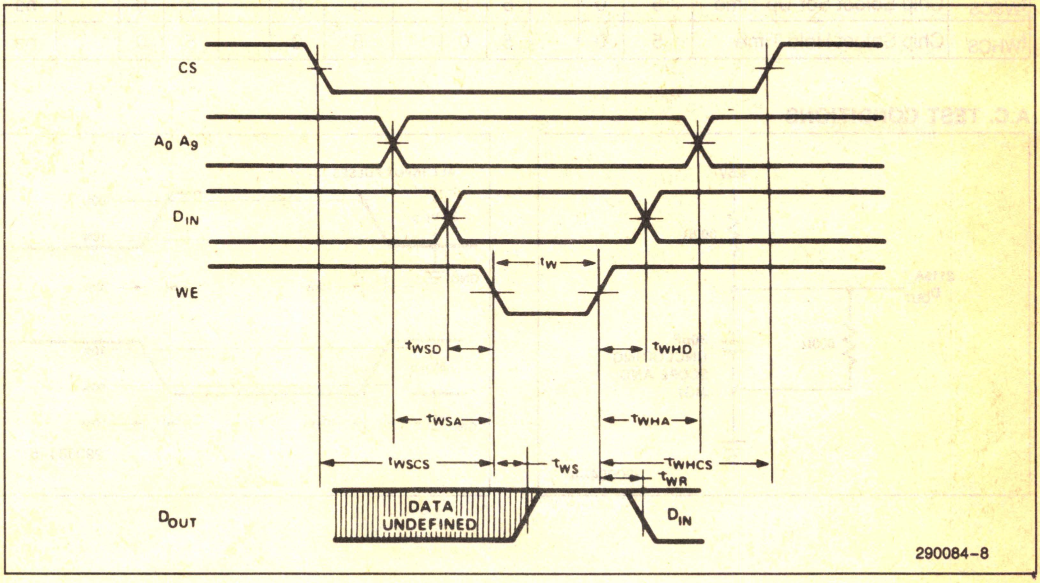
290084-6

PROPAGATION DELAY FROM CHIP SELECT


CS
tACS
tRCS
DOUT

290084-7

WRITE CYCLE


CS
A0 A9
DIN
WE
tW
tWSD
tWHD
tWSA
tWHA
tWSCS
tWS
tWHCS
tWR
DOUT
DATA UNDEFINED
DIN

290084-8

NOTE:
All above measurements referenced to 1.5V.

2125 FAMILY A.C. CHARACTERISTICS(1, 2) V_{CC} = 5V ±5%, T_A = 0°C to 75°C

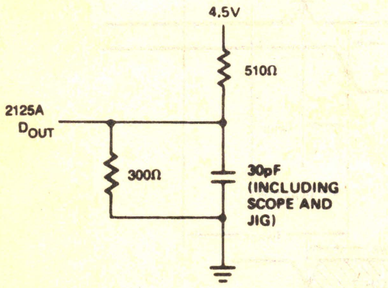
READ CYCLE

Symbol	Test	2125AL Limits			2125A Limits			2125AL-2 Limits			2125A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	Address Access Time		30	45		30	45		40	70		40	70	ns
t_{OH}	Previous Read Data Valid after Change of Address	10			10			10			10			ns

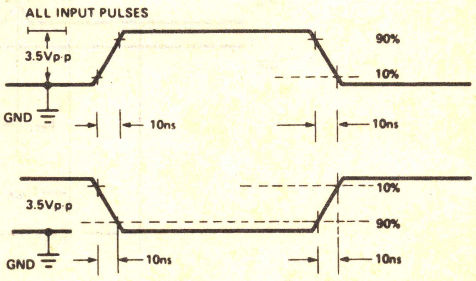
WRITE CYCLE

Symbol	Test	2125AL Limits			2125A Limits			2125AL-2 Limits			2125A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ZWS}	Write Enable Time to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time after Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

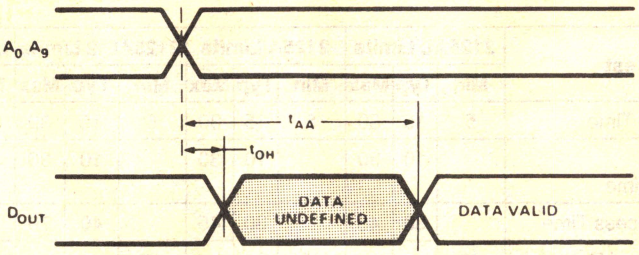

4.5V
510Ω
2125A
D_{OUT}
300Ω
30pF (INCLUDING SCOPE AND JIG)

290084-9


ALL INPUT PULSES
3.5Vp-p
GND
90%
10%
10ns
10ns
3.5Vp-p
GND
10%
90%
10ns
10ns

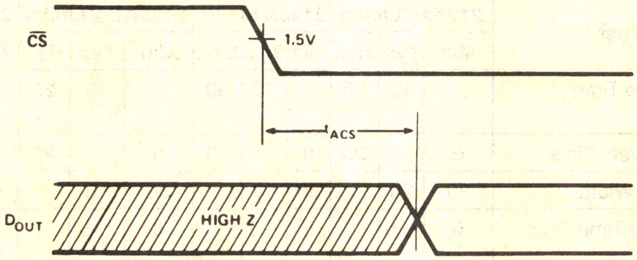
290084-10

READ CYCLE


A_0 A_9
t_{AA}
t_{OH}
D_{OUT}
DATA UNDEFINED
DATA VALID

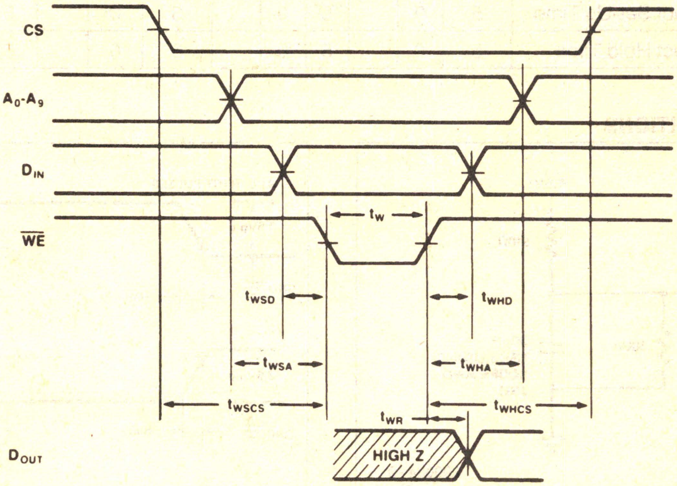
290084-11

PROPAGATION DELAY FROM CHIP SELECT


$\overline{CS}$
1.5V
t_{ACS}
D_{OUT}
HIGH Z

290084-12

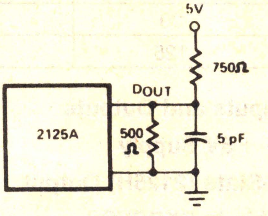
WRITE CYCLE


CS
A_0-A_9
D_{IN}
$\overline{WE}$
t_W
t_{WSD}
t_{WHD}
t_{WSA}
t_{WHA}
t_{WSCS}
t_{WHCS}
t_{WR}
D_{OUT}
HIGH Z

290084-13

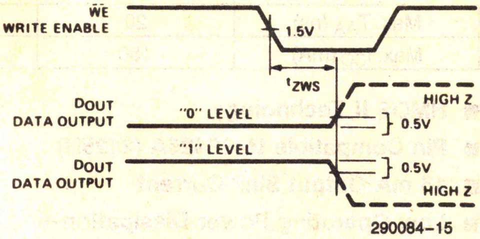
NOTE:
All above measurements referenced to 1.5V.

2125A FAMILY WRITE ENABLE TO HIGH Z DELAY


5V
750Ω
DOUT
2125A
500 Ω
5 pF

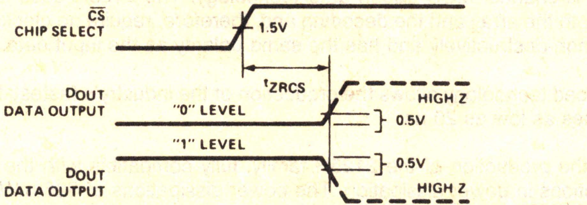
290084-14

Load 1


WE
WRITE ENABLE
1.5V
tZWS
DOUT
DATA OUTPUT
"0" LEVEL
HIGH Z
0.5V
"1" LEVEL
DOUT
DATA OUTPUT
0.5V
HIGH Z

290084-15

2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z


CS
CHIP SELECT
1.5V
tZRCS
DOUT
DATA OUTPUT
"0" LEVEL
HIGH Z
0.5V
"1" LEVEL
DOUT
DATA OUTPUT
0.5V
HIGH Z

290084-16

(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using load 1.)

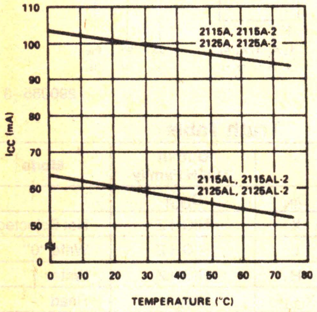
2115A/2125A FAMILY CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	2115A Family Limits		2125A Family Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

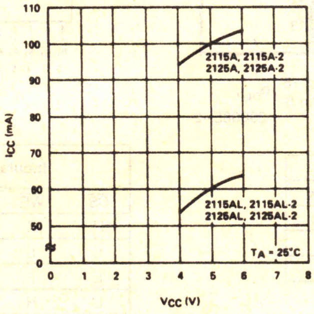
NOTE:
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

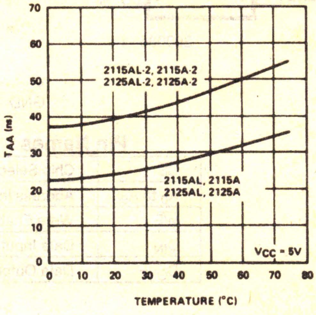
I_{CC} vs Temperature



I_{CC} vs V_{CC}



Access Time vs Temperature



290084-17

2125H
HIGH SPEED 1K × 1 BIT STATIC RAM

	2125H-1	2125H-2	2125H-3	2125H-4
Max. T_{AA} (ns)	20	25	30	35
Max. I_{CC} (mA)	150	125	125	125

- **HMOS II Technology**
- **Pin Compatible to 93425A (2125H)**
- **16 mA Output Sink Current**
- **Low Operating Power Dissipation— Max. 0.53 mW/Bit**
- **Standard 16-Pin Dual In-Line Package**
- **TTL Inputs and Outputs**
- **Single +5V Supply**
- **Three-State (2125H) Output**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**

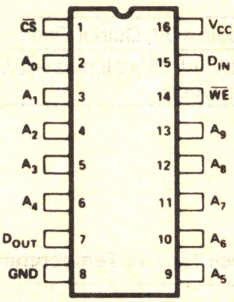
The Intel 2125H has high speed, 1024 words by 1-bit random access memories fabricated with HMOS II, Intel's advanced N-channel MOS silicon gate technology. The 2125H uses fully DC stable (static) circuitry throughout—in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

HMOS II's advanced technology allows the production of the industry's fastest, low power, 1K static RAM—offering access times as low as 20 ns.

HMOS II allows the production of the 2125H family, fully compatible with the 1K Bipolar RAMs yet offering substantial reductions in power dissipation. The power dissipations of 525 mW maximum and 656 mW maximum compared to 814 mW maximum offer reductions of 19% and 36% respectively.

The device is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

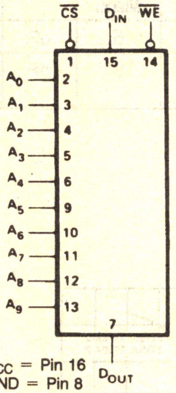
Pin Configuration



CS 1
A0 2
A1 3
A2 4
A3 5
A4 6
DOUT 7
GND 8
16 VCC
15 DIN
14 WE
13 A9
12 A8
11 A7
10 A6
9 A5

290085-1

Logic Symbol

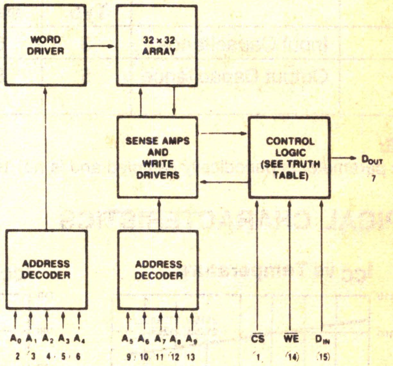


CS
DIN
WE
1
15
14
A0 2
A1 3
A2 4
A3 5
A4 6
A5 9
A6 10
A7 11
A8 12
A9 13
7
DOUT

V_{CC} = Pin 16
GND = Pin 8

290085-2

Block Diagram



WORD DRIVER
32 × 32 ARRAY
SENSE AMPS AND WRITE DRIVERS
CONTROL LOGIC (SEE TRUTH TABLE)
DOUT 7
ADDRESS DECODER
ADDRESS DECODER
A0 A1 A2 A3 A4
2 3 4 5 6
A5 A6 A7 A8 A9
9 10 11 12 13
CS 1
WE 14
DIN 15

290085-3

Pin Names

$\overline{CS}$	Chip Select
A_0 to A_9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Truth Table

Inputs			Output 2125H Family	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X_{OUT}	D_{OUT}	Read

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Order Number: 290085-003

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +85°C
Storage Temperature .... −65°C to +150°C
All Output or Supply Voltages .... −0.5V to +7V
All Input Voltages .... −1.5V to +7V
D.C. Output Current ....20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS(1,2) $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to 75°C

Symbol	Test	Min	Typ	Max	Unit	Conditions
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 16$ mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max, $V_{IN} = 0.4V$
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max, $V_{IN} = 4.5V$
$\lvert I_{OFF} \rvert$	Output Current (High Z)		0.1	50	μA	V_{CC} = Max, $V_{OUT} = 0.5V/2.4V$
I_{OS}	Current Short Circuit to Ground		125	200	mA	V_{CC} = Max.
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5.2$ mA
I_{CC}	Power Supply Current: 2125H-1	80	150		mA	All Inputs Grounded, Output Open
	I_{CC2}: 2125H-2, 2125H-4		80	125	mA	
	I_{CC3}: 2125H-3		80	125	mA	

NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$, and maximum loading.

A.C. CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

READ CYCLE

Symbol	Test	2125H-1 Limits		2125H-2 Limits		2125H-3 Limits		2125H-4 Limits		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACS}	Chip Select Time		15		15		20		20	ns
t_{ZRCS}(1)	Chip Select to HIGH Z		20		20		20		20	ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{OH}(1)	Previous Read Data Valid After Change of Address	0		0		0		0		ns

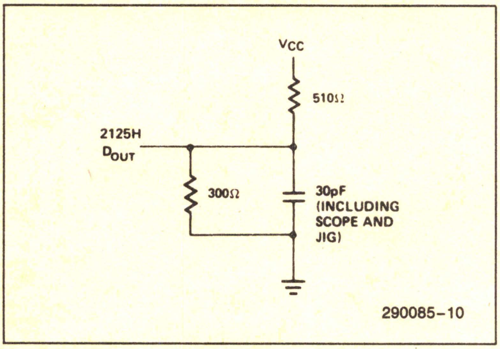
WRITE CYCLE

Symbol	Test	2125H-1 Limits		2125H-2 Limits		2125H-3 Limits		2125H-4 Limits		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZWS}(1)	Write Enable to HIGH Z		15		15		20		20	ns
t_{WR}	Write Recovery Time	0	15	0	15	0	20	0	20	ns
t_W	Write Pulse Width	20		20		20		25		ns
t_{WSD}	Data Set-Up Time Prior to Write	0		0		0		0		ns
t_{WHD}	Data Hold Time After Write	0		0		0		0		ns
t_{WSA}	Address Set-Up Time	5		5		5		5		ns
t_{WHA}(1)	Address Hold Time	0		0		0		0		ns
t_{WSCS}	Chip Select Set-Up Time	5		5		5		5		ns
t_{WHCS}	Chip Select Hold Time	5		5		5		5		ns

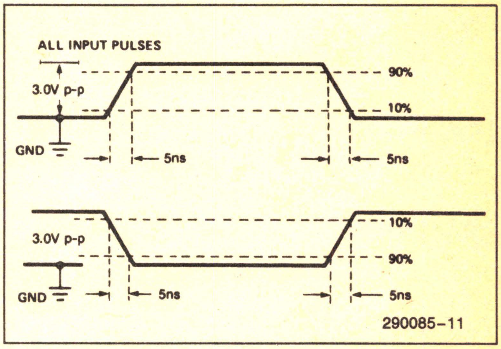
NOTE:

1. These specifications are guaranteed by design and not production tested.

A.C. TEST CONDITIONS

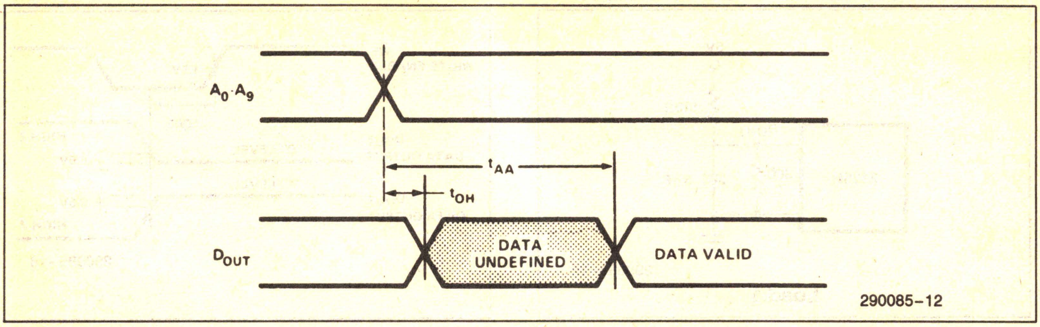

VCC
510Ω
2125H
DOUT
300Ω
30pF (INCLUDING SCOPE AND JIG)

290085-10


ALL INPUT PULSES
3.0V p-p
GND
90%
10%
5ns
5ns
3.0V p-p
GND
10%
90%
5ns
5ns

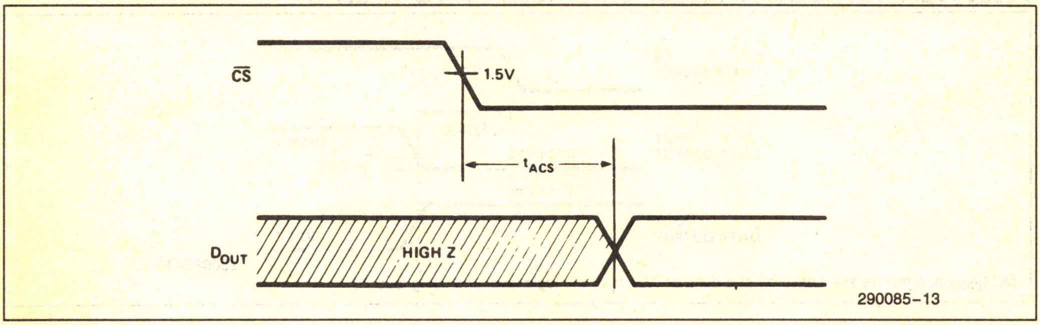
290085-11

READ CYCLE


A_0-A_9
t_{AA}
t_{OH}
D_{OUT}
DATA UNDEFINED
DATA VALID

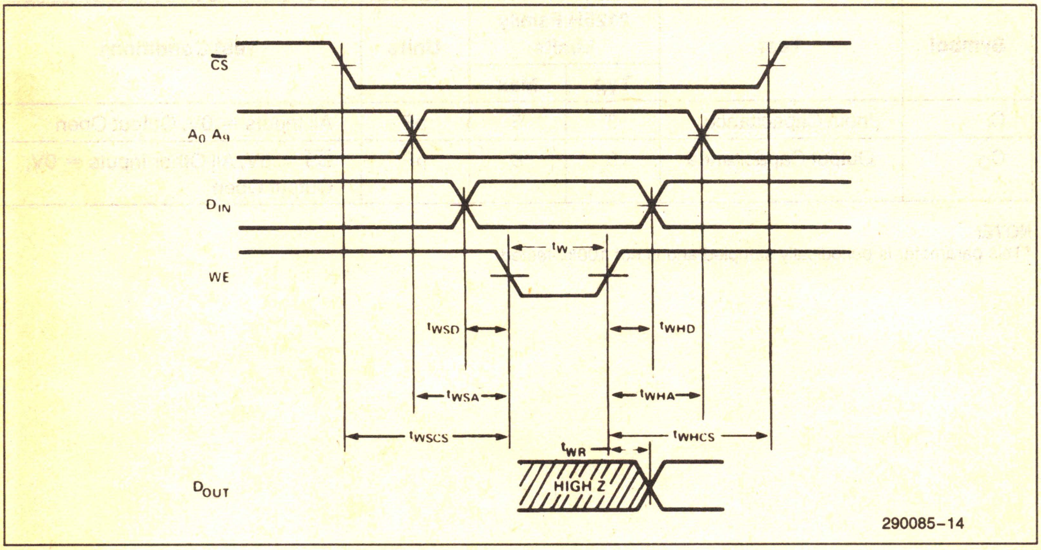
290085-12

PROPAGATION DELAY FROM CHIP SELECT


$\overline{CS}$
1.5V
t_{ACS}
D_{OUT}
HIGH Z

290085-13

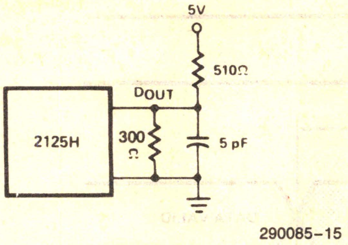
WRITE CYCLE


$\overline{CS}$
A_0 A_9
D_{IN}
WE
t_W
t_{WSD}
t_{WHD}
t_{WSA}
t_{WHA}
t_{WSCS}
t_{WHCS}
t_{WR}
D_{OUT}
HIGH Z

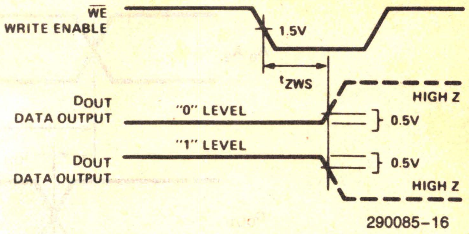
290085-14

(All above measurements referenced to 1.5V.)

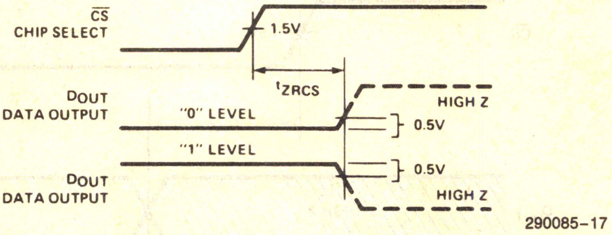
WRITE ENABLE TO HIGH Z DELAY


5V
510Ω
DOUT
2125H
300 Ω
5 pF
290085–15

Load 1


WE
WRITE ENABLE
1.5V
tZWS
DOUT
DATA OUTPUT
"0" LEVEL
HIGH Z
0.5V
"1" LEVEL
0.5V
DOUT
DATA OUTPUT
HIGH Z
290085–16

PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z


CS
CHIP SELECT
1.5V
tZRCS
DOUT
DATA OUTPUT
"0" LEVEL
HIGH Z
0.5V
"1" LEVEL
0.5V
DOUT
DATA OUTPUT
HIGH Z
290085–17

(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using load 1.)

CAPACITANCE* $V_{CC} = 5V$, f = 1 MHz, $T_A = 25°C$

Symbol	Test	2125H Family Limits		Units	Test Conditions
		Typ	Max		
C_I	Input Capacitance	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

NOTE:
*This parameter is periodically sampled and is not 100% tested.

2147H
HIGH SPEED 4096 x 1 BIT STATIC RAM

	2147H-1	2147H-2	2147H-3	2147H
Max. Access Time (ns)	35	45	55	70
Max. Active Current (mA)	180	180	180	160
Max. Standby Current (mA)	30	30	30	20

- **Pinout, Function, and Power Compatible to Industry Standard 2147**
- **HMOS* III Technology**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **0.8–2.0V Output Timing Reference Levels**
- **Direct Performance Upgrade for 2147**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**
- **Separate Data Input and Output**
- **High Reliability Plastic or Cerdip**
- **Three-State Output**

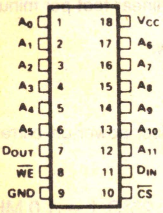
The Intel 2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS III, an ultra high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—deselecting the 2147H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2147H is assembled in an 18-pin package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

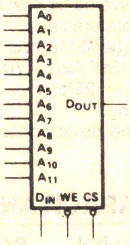
*HMOS is a patent process of Intel.

Pin Configuration


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DOUT 7
WE 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DIN
10 CS

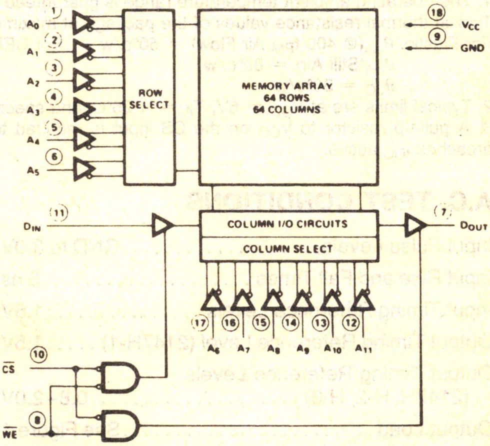
290086-1

Logic Symbol


A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DOUT
DIN
WE
CS

290086-2

Block Diagram


A0
A1
A2
A3
A4
A5
1
2
3
4
5
6
ROW SELECT
MEMORY ARRAY
64 ROWS
64 COLUMNS
18
VCC
9
GND
11
DIN
COLUMN I/O CIRCUITS
COLUMN SELECT
7
DOUT
17
16
15
14
13
12
A6
A7
A8
A9
A10
A11
10
CS
8
WE

290086-3

Pin Names

A_0–A_{11}	Address Inputs	V_{CC} Power (+5V)
$\overline{WE}$	Write Enable	GND Ground
$\overline{CS}$	Chip Select	
D_{IN}	Data Input	
D_{OUT}	Data Output	

Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986
Order Number: 290086-003

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −10°C to 85°C
Storage Temperature . . . . −65°C to +150°C
Voltage on Any Pin
  with Respect to Ground . . . . −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current . . . . 20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted

Symbol	Parameter	2147H-1, 2, 3			2147H			Unit	Test Conditions	
		Min	Typ	Max	Min	Typ(2)	Max			
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	μA	V_{CC} = Max., V_{IN} = GND to V_{CC}	
$\lvert I_{LO} \rvert$	Output Leakage Current		0.1	10		0.1	10	μA	$\overline{CS} = V_{IH}$, V_{CC} = 5.5V V_{OUT} = GND to 4.5V	
I_{CC}	Operating Current		120	170		100	150	mA	T_A = 25°C	V_{CC} = Max., $\overline{CS} = V_{IL}$, Outputs Open
				180			160	mA	T_A = 0°C	
I_{SB}	Standby Current		18	30		12	20	mA	V_{CC} = Min. to Max. $\overline{CS} = V_{IH}$	
I_{PO}(3)	Peak Power-On Current		35	70		25	50	mA	V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V		
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V		
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA	

NOTES:

1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:

For Plastic: θ_{JA}(@ 400 f_{PM} Air Flow) = 50°c/w
θ_{JA}(Still Air) = 80°c/w
θ_{JC} = 30°c/w

For CERDIP: θ_{JA}(@400 f_{PM} Air Flow) = 40°c/w
θ_{JA}(Still Air) = 70°c/w
θ_{JC} = 25°c/w

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels . . . . GND to 3.0V
Input Rise and Fall Times . . . . 5 ns
Input Timing Reference Levels 1.5V
Output Timing Reference Level (2147H-1) 1.5V
Output Timing Reference Levels
  (2147H, H-2, H-3) 0.8–2.0V
Output Load . . . . See Figure 1

CAPACITANCE(4) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

NOTE:
4. This parameter is sampled and not 100% tested.

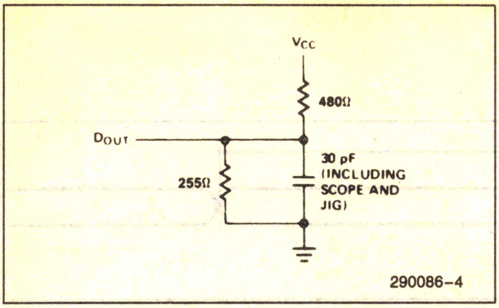

VCC
480Ω
DOUT
255Ω
30 pF (INCLUDING SCOPE AND JIG)
290086-4

Figure 1. Output Load

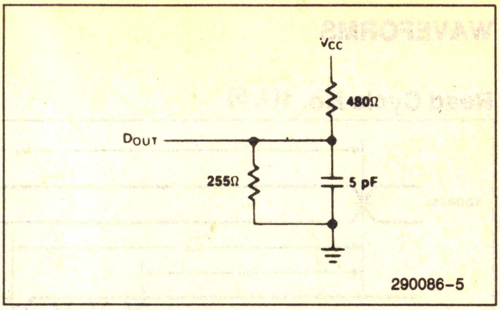

VCC
480Ω
DOUT
255Ω
5 pF
290086-5

Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CHARACTERISTICS

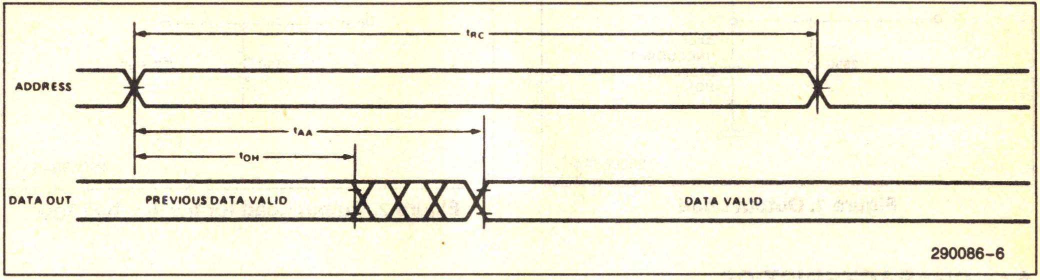
T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted

Read Cycle

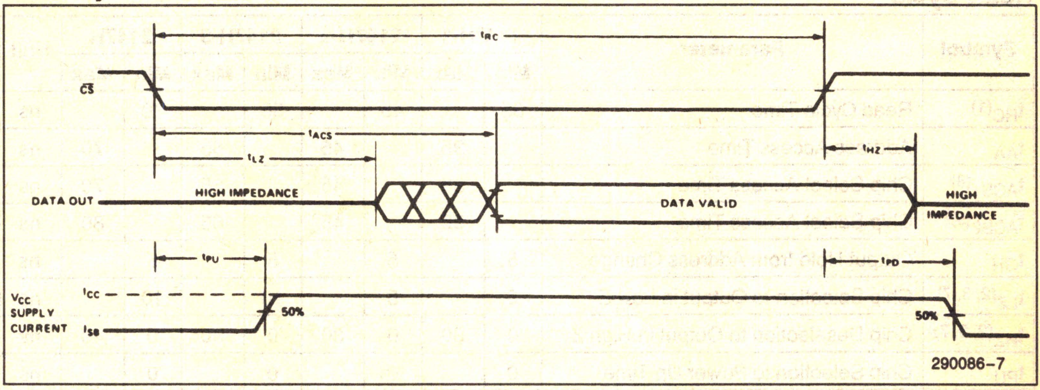
Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RC}^{(1)}$	Read Cycle Time	35		45		55		70		ns
t_{AA}	Address Access Time		35		45		55		70	ns
$t_{ACS1}^{(8)}$	Chip Select Access Time		35		45		55		70	ns
$t_{ACS2}^{(9)}$	Chip Select Access Time		35		45		65		80	ns
t_{OH}	Output Hold from Address Change	5		5		5		5		ns
$t_{LZ}^{(2, 3, 7)}$	Chip Selection to Output in Low Z	5		5		10		10		ns
$t_{HZ}^{(2, 3, 7)}$	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		20		20		30	ns

WAVEFORMS

Read Cycle No. 1(4, 5)


tRC
ADDRESS
tAA
tOH
DATA OUT
PREVIOUS DATA VALID
DATA VALID
290086-6

Read Cycle No. 2(4, 6)


tRC
CS
tACS
tLZ
tHZ
DATA OUT
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
tPU
tPD
VCC SUPPLY CURRENT
ICC
ISB
50%
50%
290086-7

NOTES:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1. Applies to 2147H, 2147H-3.

A.C. CHARACTERISTICS (Continued)

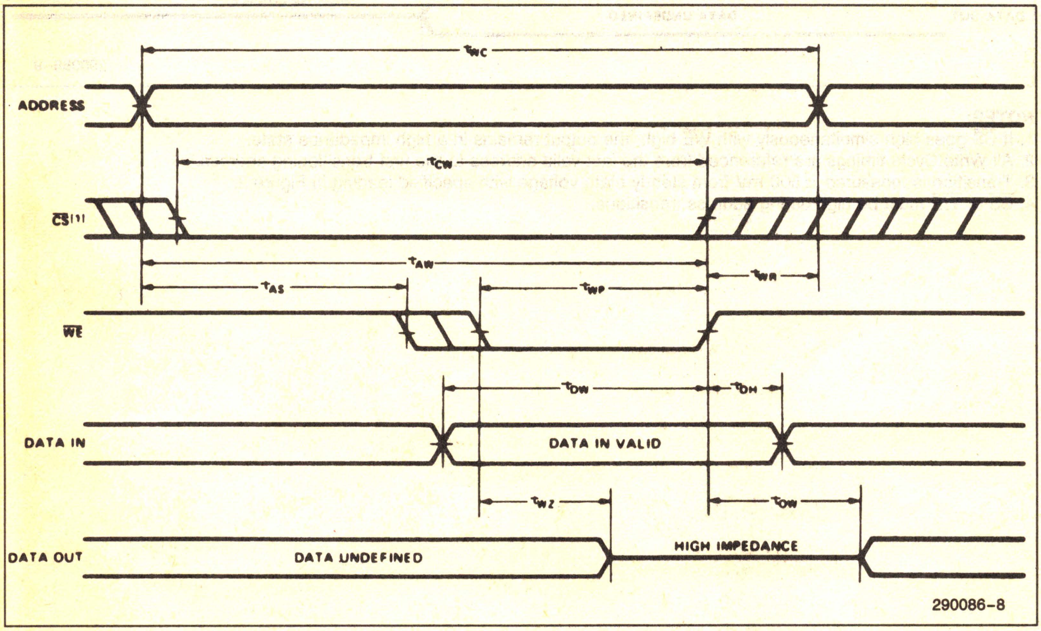
Write Cycle

Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}(2)	Write Cycle Time	35		45		55		70		ns
t_{CW}	Chip Selection to End of Write	35		45		45		55		ns
t_{AW}	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	20		25		25		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	20		25		25		30		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}(3)	Write Enabled to Output in High Z	0	20	0	25	0	25	0	35	ns
t_{OW}(3)	Output Active from End of Write	0		0		0		0		ns

WAVEFORMS

Write Cycle No. 1

($\overline{WE}$ CONTROLLED)(4)



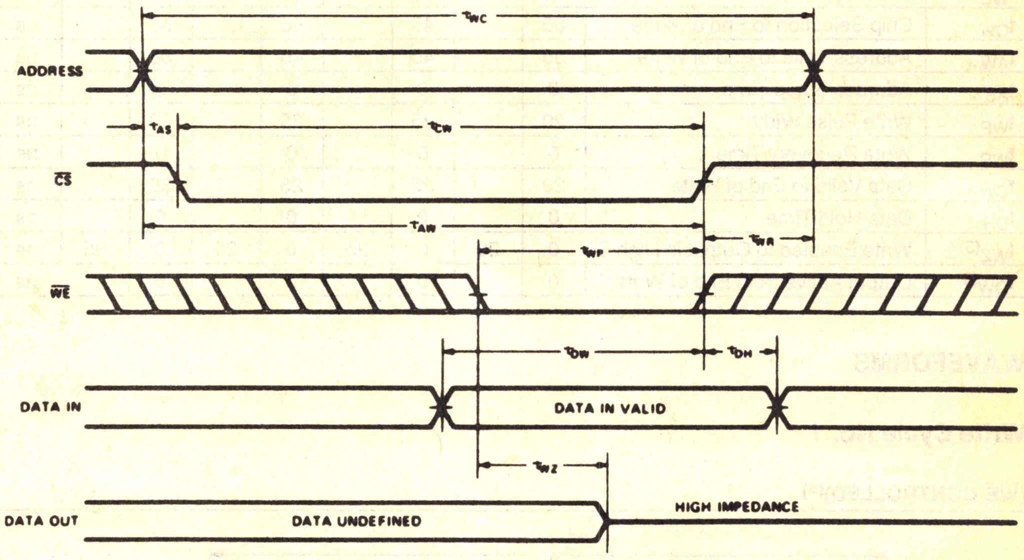
t_WC
ADDRESS
t_CW
$\overline{CS}$(1)
t_AW
t_AS
t_WP
t_WR
$\overline{WE}$
t_DW
t_DH
DATA IN
DATA IN VALID
t_WZ
t_OW
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

290086-8

WAVEFORMS (Continued)

Write Cycle No. 2

($\overline{CS}$ CONTROLLED)(4)


t_{WC}
ADDRESS
t_{AS}
t_{CW}
$\overline{CS}$
t_{AW}
t_{WR}
t_{WP}
$\overline{WE}$
t_{DW}
t_{DH}
DATA IN
DATA IN VALID
t_{WZ}
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE

290086-9

NOTES:

1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

2148H FAMILY
1024 x 4 BIT STATIC RAM

	**2148H-2	2148H-3	2148H	**2148HL-3	2148HL
Max Access Time (ns)	45	55	70	55	70
Max Active Current (mA)	150	**150	**150	125	125
Max Standby Current (mA)	30	30	30	20	20

- **Improved Performance Margins**
- **Automatic Power-Down**
- **Single +5V Supply**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **HMOS* III Technology**
- **Common Data Input and Output**
- **Three-State Output**
- **High Reliability Plastic or CERDIP Package**

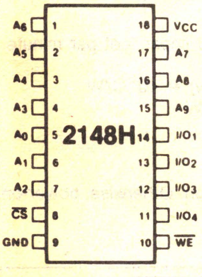
The Intel 2148H is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, an ultra high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{\text{CS}}$ controls the power-down feature. In less than a cycle time after $\overline{\text{CS}}$ goes high—disabling the 2148H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{\text{CS}}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled. A non-power-down companion, the 2149H, is available to provide a fast chip select access time for speed critical applications.

The 2148H is assembled in an 18-pin plastic package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

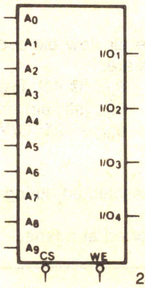
*HMOS is a patent process of Intel Corporation. **Improved performance margins.

Pin Configuration


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 WE
2148H

230781-1

Logic Symbol


A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
CS
WE
I/O1
I/O2
I/O3
I/O4

230781-2

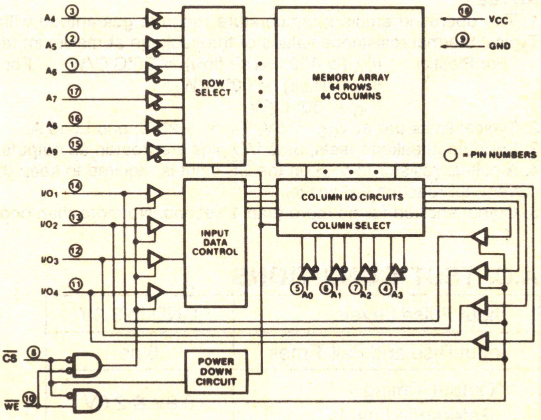
Pin Names

A_0–A_9	Address Inputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
VO_1–V_4	Data Input Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	VO	Power
H	X	Not Selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

Figure 1. Pin Configuration, Logic Symbol, Pin Names and Truth Table


A4 3
A5 2
A6 1
A7 17
A8 16
A9 15
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
18 VCC
9 GND
○ = PIN NUMBERS
I/O1 14
I/O2 13
I/O3 12
I/O4 11
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
5 A0
6 A1
7 A2
4 A3
CS 8
WE 10
POWER DOWN CIRCUIT

230781-3

Figure 2. 2148H Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. November 1986

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Order Number: 230781-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +85°C
Storage Temperature CERDIT ... −65°C to +150°C
Storage Temperature Plastic .... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground .... −3.5V to +7V
D.C. Continuous Output Current .... 20 mA
Power Dissipation 1.2W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to +70°C, V_{CC} = +5V ± 10% unless otherwise noted.

Symbol	Parameter	2148H/H-3/H-2			2148HL/HL-3			Unit	Test Conditions
		Min	Typ[2]	Max	Min	Typ[2]	Max		
*$\lvert I_{LI}\rvert$	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	μA	V_{CC} = max, V_{IN} = GND to V_{CC}
*$\lvert I_{LO}\rvert$(3)	Output Leakage Current		0.1	10		0.1	10	μA	CS = V_{IH}, V_{CC} = max, V_{OUT} = GND to 4.5V
*I_{CC}	Operating Current		100	150		70	125	mA	V_{CC} = max, $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		20	30		10	20	mA	V_{CC} = min to max, $\overline{CS}$ = V_{IH}
I_{PO}(4)	Peak Power-On Current		25	50		15	30	mA	V_{CC} = GND to V_{CC} min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} min
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
*V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA
I_{OS}(5)	Output Short Circuit Current		±250	±275		±250	±275	mA	V_{OUT} = GND to V_{CC}

NOTES:

1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:

For Plastic θ_{JA} (@ 400 f_{PM} air flow) = 50°C C/W
θ_{JA} (still air) = 80° C/W
θ_{JC} = 30° C/W

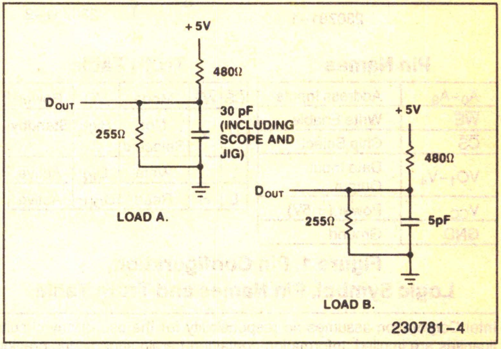
For CERDIP θ_{JA} (@ 400 f_{PM} air flow) = 40° C/W
θ_{JA} (still air) = 70° C/W
θ_{JC} = 25° C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. For output leakage tests, data I/O pins are treated as outputs.
4. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-on. Otherwise, power-on current approaches I_{CC} active.
5. Output shorted for no more than 1 second. No more than one output shorted at a time.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
*Output Timing Reference Levels	0.8V & 2.0V
Output Load	See Load A

*Improved perfomance margins.



230781-4

CAPACITANCE(1) $T_A = 25°C, f = 1.0\ MHz$

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	$V_{IN} = 0V$
C_{IO}	Input/Output Capacitance	7	pF	$V_{OUT} = 0V$

NOTE:
1. This parameter is sampled and not 100% tested.

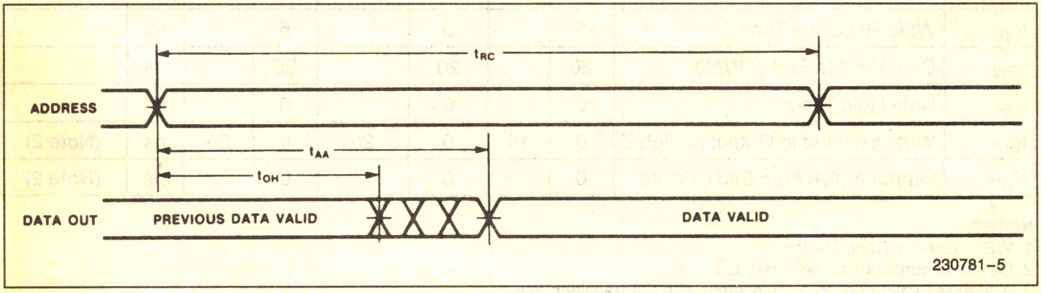
A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

Symbol	Parameter	2148H-2		2148H-3/HL-3		2148H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS}	Chip Select Access Time		45		55		70	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	20		20		20		ns	(Note 4)
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	(Note 4)
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

WAVEFORMS

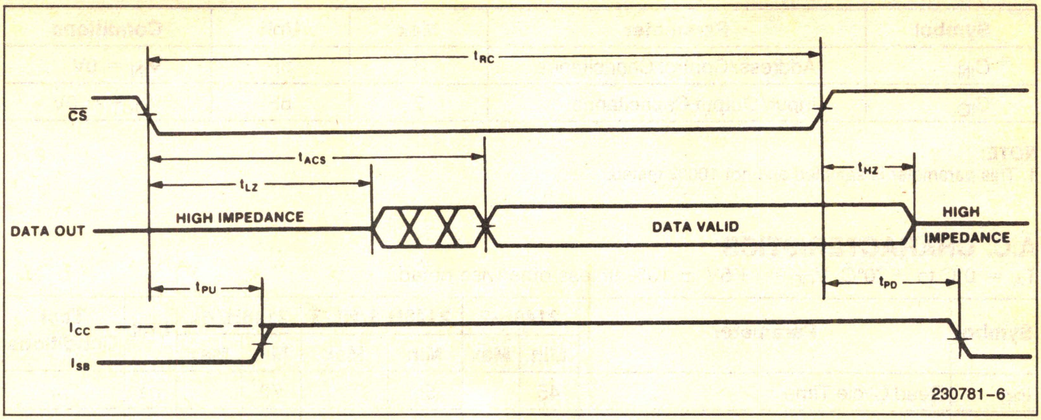
READ CYCLE NO. 1(1,2)



230781–5

NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

READ CYCLE NO. 2(1,3)


t_{RC}
$\overline{CS}$
t_{ACS}
t_{LZ}
t_{HZ}
DATA OUT
HIGH IMPEDANCE
DATA VALID
HIGH IMPEDANCE
t_{PU}
t_{PD}
I_{CC}
I_{SB}
230781-6

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

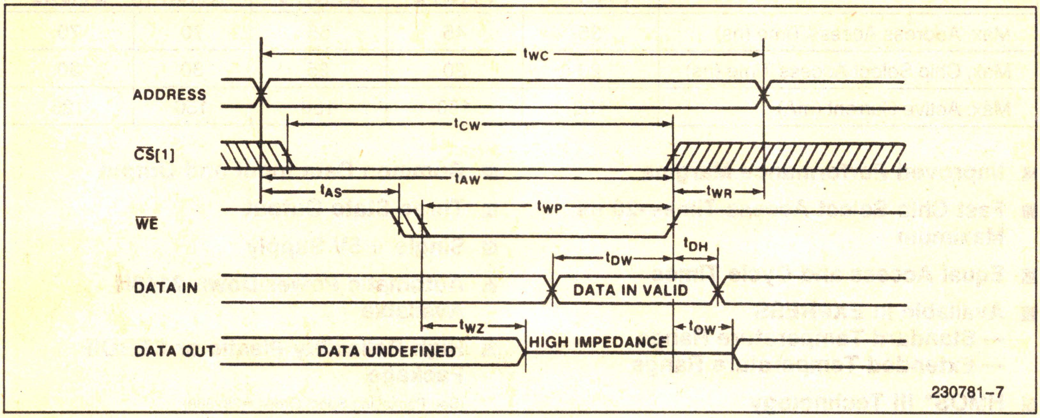
Symbol	Parameter	2148H-2		2148H-3/HL-3		2148/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	(Note 2)
t_{OW}	Output Active from End of Write	0		0		0		ns	(Note 2)

NOTES:

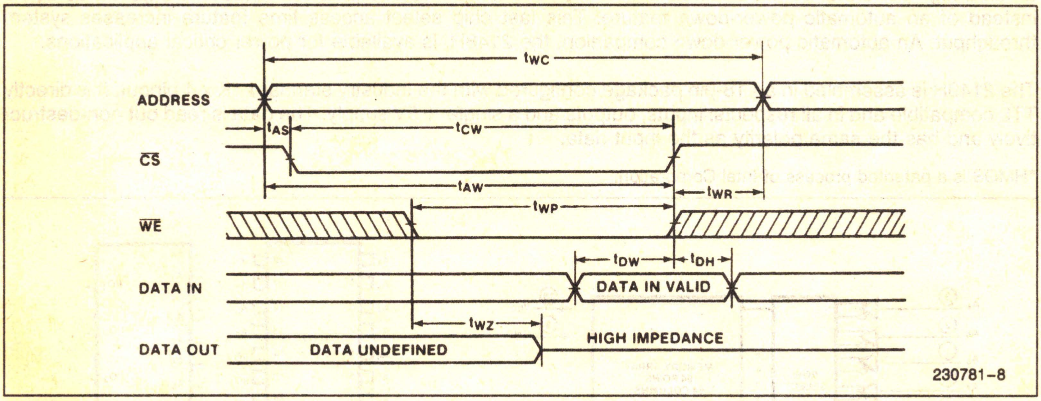
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)


tWC
ADDRESS
tCW
$\overline{CS}$[1]
tAW
tAS
tWR
tWP
$\overline{WE}$
tDH
tDW
DATA IN
DATA IN VALID
tWZ
tOW
HIGH IMPEDANCE
DATA OUT
DATA UNDEFINED
230781-7

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)


tWC
ADDRESS
tAS
tCW
$\overline{CS}$
tAW
tWR
tWP
$\overline{WE}$
tDW
tDH
DATA IN
DATA IN VALID
tWZ
DATA OUT
DATA UNDEFINED
HIGH IMPEDANCE
230781-8

NOTES:

1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B.

2149H
1024 x 4-BIT STATIC RAM

	2149H-1	2149H-2	2149H-3	2149H	2149HL
Max. Address Access Time (ns)	35	45	55	70	70
Max. Chip Select Access Time (ns)	20	20	25	30	30
Max. Active Current (mA)	150	150	150	150	125

- **Improved Performance Margins**
- **Fast Chip Select Access Time—20 ns Maximum**
- **Equal Access and Cycle Times**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**
- **HMOS* III Technology**
- **Common Data Input and Output**
- **Three-State Output**
- **Single +5V Supply**
- **Automatic Power-Down 2148H Available**
- **High Reliability Plastic or CERDIP Package**

  (See Packaging Spec. Order #231369)

The Intel 2149H is 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, an ultra high-performance MOS technology. It provides a maximum chip select access time as low as 20 ns instead of an automatic power-down feature. This fast chip select access time feature increases system throughput. An automatic power-down companion, the 2148H, is available for power critical applications.

The 2149H is assembled in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible and in all respects: inputs, outputs and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

*HMOS is a patented process of Intel Corporation.

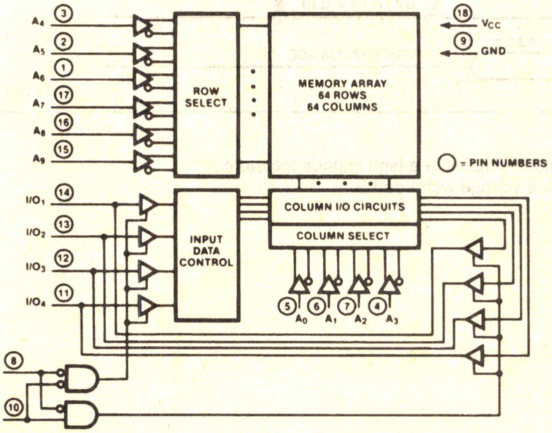

A4 ③
A5 ②
A6 ①
A7 ⑰
A8 ⑯
A9 ⑮
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
⑱ VCC
⑨ GND
○ = PIN NUMBERS
I/O1 ⑭
I/O2 ⑬
I/O3 ⑫
I/O4 ⑪
INPUT DATA CONTROL
COLUMN I/O CIRCUITS
COLUMN SELECT
⑤ A0
⑥ A1
⑦ A2
④ A3
CS ⑧
WE ⑩
230919–1

Figure 1. 2149 Block Diagram

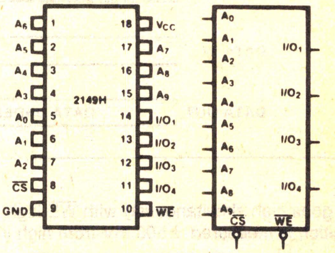

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 WE
2149H
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
I/O1
I/O2
I/O3
I/O4
CS
WE
230919–2

Figure 2. 2149 Pin Diagram

Pin Names

A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1–I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O
H	X	Not Selected	HIGH-Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.
November 1986
Order Number: 230919-003
© Intel Corporation, 1986

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −10°C to +85°C
Storage Temperature CERDIP . . . −65°C to +150°C
Storage Temperature Plastic . . . . −65°C to +125°C
Voltage on Any Pin with Respect to Ground . . . . −3.5V to +7V
D.C. Continuous Output Current . . . . 20 mA
Power Dissipation 1.2W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to + 70°C, V_{CC} = +5V ±10% unless otherwise noted.

Symbol	Parameter	2149H/H-1/H-2/H-3			2149HL			Unit	Test Conditions
		Min	Typ(2)	Max	Min	Typ(2)	Max		
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	μA	V_{CC} = max, V_{IN} = GND to 5.5V
I_{LO}	Output Leakage Current		0.1	10		0.1	10	μA	$\overline{CS} = V_{IH}$, V_{CC} = 5.5V V_{OUT} = GND to 5.5V
I_{CC}	Operating Current		100	150		70	125	mA	V_{CC} = max, $\overline{CS} = V_{IL}$ Outputs Open
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA
I_{OS}(4)	Output Short Circuit Current		±200	±275		±200	±275	mA	V_{OUT} = GND to V_{CC}

A.C. Test Conditions

Input pulse levels . . . . GND to 3.0V
Input rise and fall times . . . . 5 ns
*Output timing reference levels . . . . . . 0.8V and 2.0V
Output load . . . . See Load A.

CAPACITANCE(5)

T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	V_{IN} = 0V
C_{IO}	Input/Output Capacitance	7	pF	V_{OUT} = 0V

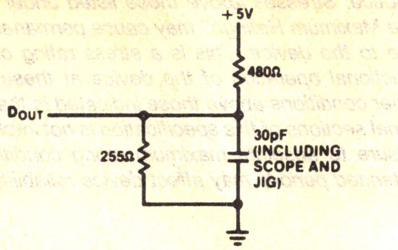
NOTES:

1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:

For CERDIP	θ_{JA}(@400 f_{PM} air flow) = 40°C/W	For Plastic	θ_{JA}(@400 f_{PM} air flow) = 50°C/W
	θ_{JA}(still air) = 70°C/W		θ_{JA}(still air) = 80°C/W
	θ_{JC} = 25°C/W		θ_{JC} = 30°C/W

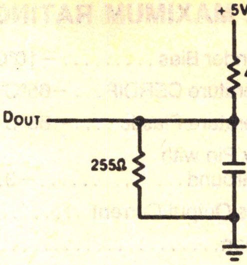
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. For Output Leakage tests, Data I/O pins are treated as outputs.
4. Outputs shorted for no more than 1 second. No more than one output shorted at a time.
5. This parameter is sampled and not 100% tested.

*improved performance margins


+5V
480Ω
DOUT
255Ω
30pF (INCLUDING SCOPE AND JIG)

230919-3

Load A


+5V
480Ω
DOUT
255Ω
5pF

230919-4

Load B

A.C. CHARACTERISTICS

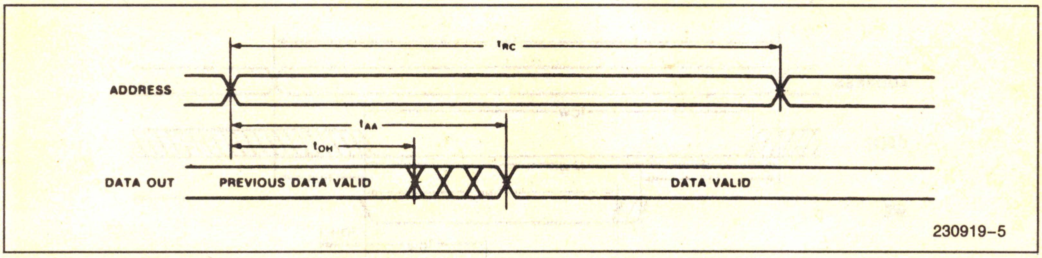
T_A = 0°C to 70°C, V_{CC} = +5V ± 10% unless otherwise noted.

READ CYCLE

Symbol	Parameter	2149H-1		2149H-2		2149H-3		2149H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	35		45		55		70		ns	
t_{AA}	Address Access Time		35		45		55		70	ns	
t_{ACS}	Chip Select Access Time		20		20		25		30	ns	
t_{OH}	Output Hold from Address Change	5		5		5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	5		5		5		5		ns	(Notes 3, 4)
t_{HZ}	Chip Deselection to Output in High Z	0	15	0	15	0	15	0	15	ns	(Notes 3, 4)

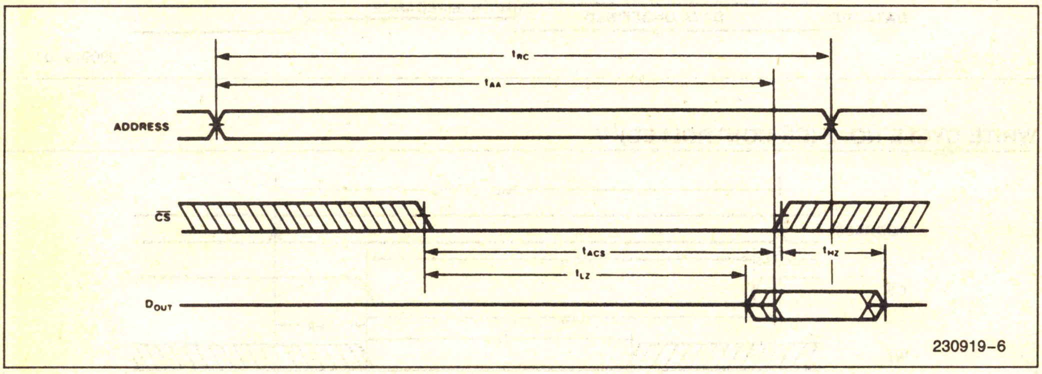
WAVEFORMS

READ CYCLE NO. 1[1, 2]


t_{RC}
ADDRESS
t_{AA}
t_{OH}
DATA OUT
PREVIOUS DATA VALID
DATA VALID

230919-5

READ CYCLE NO. 2[3]


t_{RC}
t_{AA}
ADDRESS
$\overline{CS}$
t_{ACS}
t_{HZ}
t_{LZ}
D_{OUT}

230919-6

NOTES:

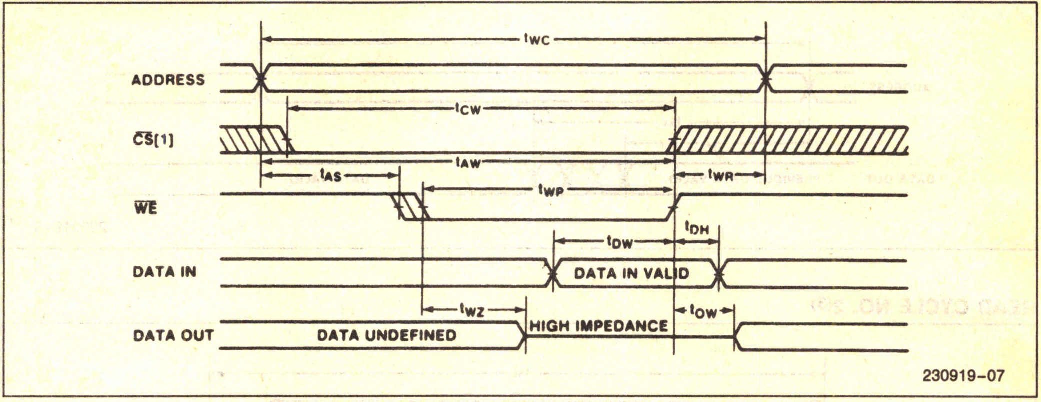
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

WRITE CYCLE

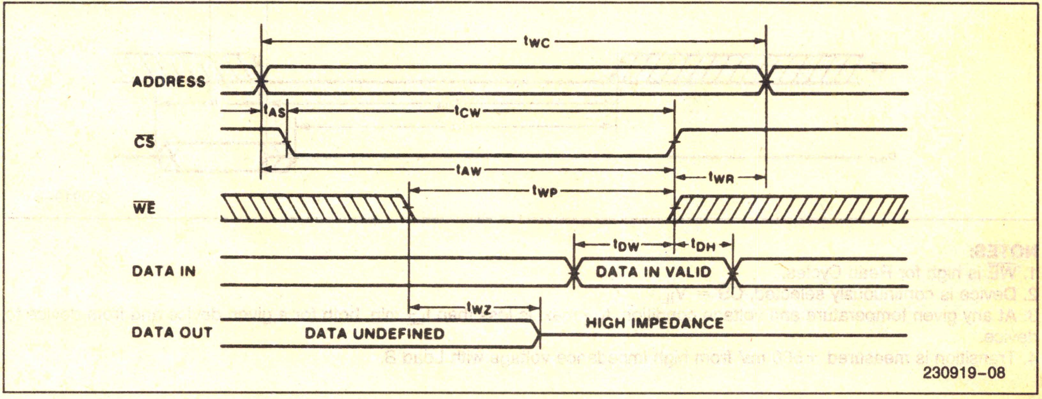
Symbol	Parameter	2149H-1		2149H-2		2149H-3		2149H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	35		45		55		70		ns	
t_{CW}	Chip-Selection to End of Write	30		40		50		65		ns	
t_{AW}	Address Valid to End of Write	30		40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{WP}	Write Pulse Width	30		35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	15	0	20	0	25	ns	(Note 2)
t_{OW}	Output Active from End of Write	0		0		0		0		ns	(Note 2)

WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(3)


ADDRESS
$\overline{CS}$[1]
$\overline{WE}$
DATA IN
DATA OUT
t_{WC}
t_{CW}
t_{AW}
t_{AS}
t_{WP}
t_{WR}
t_{DW}
t_{DH}
DATA IN VALID
t_{WZ}
t_{OW}
HIGH IMPEDANCE
DATA UNDEFINED
230919-07

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(3)


ADDRESS
$\overline{CS}$
$\overline{WE}$
DATA IN
DATA OUT
t_{WC}
t_{AS}
t_{CW}
t_{AW}
t_{WP}
t_{WR}
t_{DW}
t_{DH}
DATA IN VALID
t_{WZ}
HIGH IMPEDANCE
DATA UNDEFINED
230919-08

NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B.
3. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

RAM FAMILY

EXPRESS

- **Standard Temperature Range**
- **Extended Temperature Range −40°C−+85°C Available**
- **168 (±8) Hour Burn-In Available**
- **Inspected to 0.1% AQL**

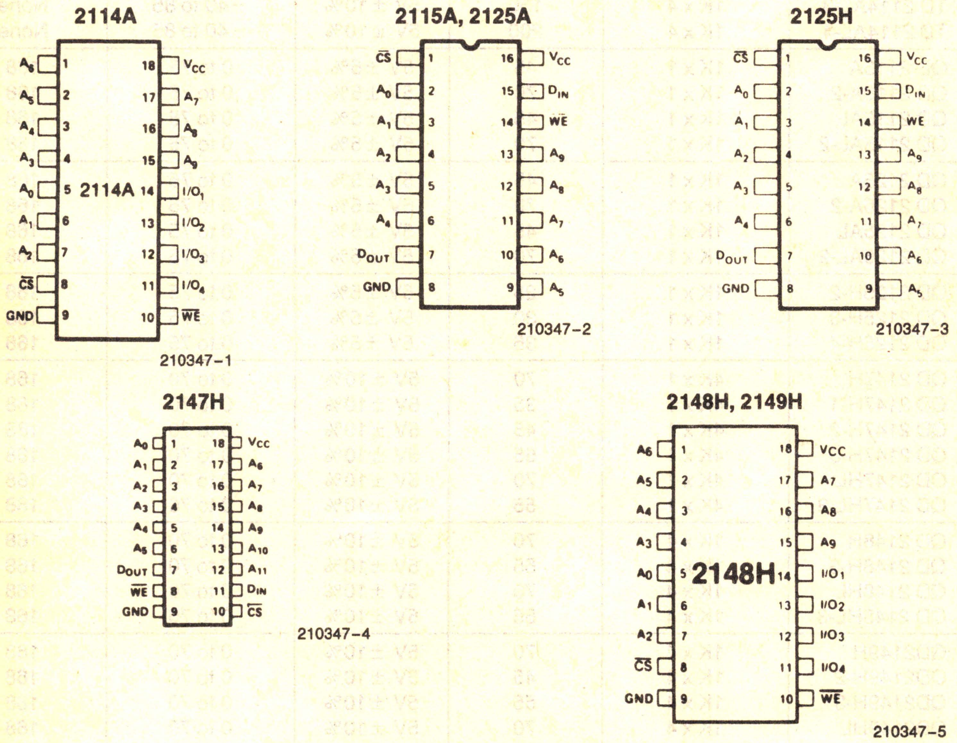
The Intel EXPRESS RAM family is a series of random-access memories which have received additional processing to enhance product operating temperature range and infant mortality. EXPRESS processing is available for several densities of RAM, allowing the choice of appropriate memory size to match system applications.

EXPRESS RAM product is available with 168 (±8) hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in.

The standard EXPRESS RAM operating temperature range is 0°C to 70 or 75°C. Extended operating temperature range (−40°C to +85°) EXPRESS product is available. EXPRESS products plus military grade RAMs (−55°C to +125°C) provide the most complete choice of standard and extended temperature range RAMs available.

Like all Intel RAMs, the EXPRESS RAM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

Detailed individual product electrical specifications are available separately in Intel's respective commercial and industrial grade product data sheets.



2114A

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 Vcc
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 WE
2114A

210347-1

2115A, 2125A

CS 1
A0 2
A1 3
A2 4
A3 5
A4 6
DOUT 7
GND 8
16 Vcc
15 DIN
14 WE
13 A9
12 A8
11 A7
10 A6
9 A5

210347-2

2125H

CS 1
A0 2
A1 3
A2 4
A3 5
A4 6
DOUT 7
GND 8
16 Vcc
15 DIN
14 WE
13 A9
12 A8
11 A7
10 A6
9 A5

210347-3

2147H

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DOUT 7
WE 8
GND 9
18 Vcc
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 DIN
10 CS

210347-4

2148H, 2149H

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CS 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 I/O1
13 I/O2
12 I/O3
11 I/O4
10 WE
2148H

210347-5

Pin Configuration

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986
Order Number: 210347-001

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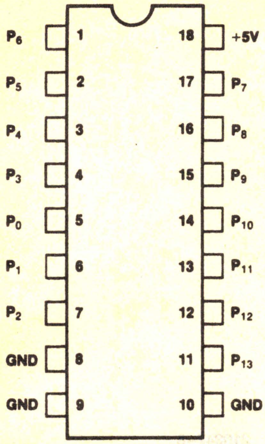
Table 1. RAM Product Family

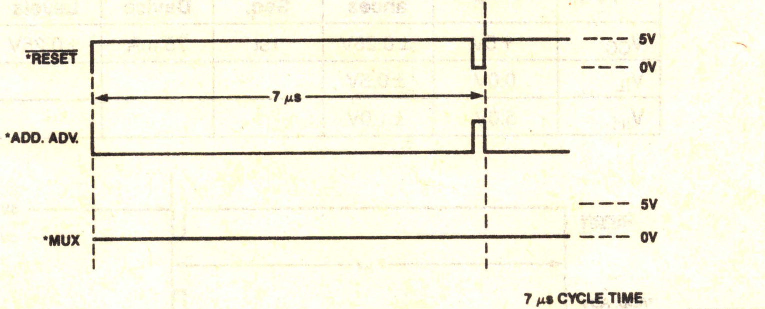
EXPRESS

Type	Organization	Maximum Access (ns)	Power Supply	Operating Temperature (°C)	Burn-In 125°C (±8 hours)
QD 2114A-4	1K x 4	200	5V ±10%	0 to 70	168
QP 2114A-4	1K x 4	200	5V ±10%	0 to 70	168
QD 2114A-5	1K x 4	250	5V ±10%	0 to 70	168
QP 2114A-5	1K x 4	250	5V ±10%	0 to 70	168
QP 2114A-6	1K x 4	300	5V ±10%	0 to 70	168
QD 2114AL-1	1K x 4	100	5V ±10%	0 to 70	168
QP 2114AL-1	1K x 4	100	5V ±10%	0 to 70	168
QD 2114AL-2	1K x 4	120	5V ±10%	0 to 70	168
QP 2114AL-2	1K x 4	120	5V ±10%	0 to 70	168
QD 2114AL-3	1K x 4	150	5V ±10%	0 to 70	168
QP 2114AL-3	1K x 4	150	5V ±10%	0 to 70	168
QD 2114AL-4	1K x 4	200	5V ±10%	0 to 70	168
QP 2114AL-4	1K x 4	200	5V ±10%	0 to 70	168
LD 2114A-4	1K x 4	200	5V ±10%	−40 to 85	168
LD 2114A-5	1K x 4	250	5V ±10%	−40 to 85	168
LD 2114AL-3	1K x 4	150	5V ±10%	−40 to 85	168
LD 2114AL-4	1K x 4	200	5V ±10%	−40 to 85	168
TD 2114A-4	1K x 4	200	5V ±10%	−40 to 85	None
TD 2114A-5	1K x 4	250	5V ±10%	−40 to 85	None
TD 2114AL-3	1K x 4	150	5V ±10%	−40 to 85	None
TD 2114AL-4	1K x 4	200	5V ±10%	−40 to 85	None
QD 2115A	1K x 1	45	5V ±5%	0 to 75	168
QD 2115A-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2115AL	1K x 1	45	5V ±5%	0 to 75	168
QD 2115AL-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125A	1K x 1	45	5V ±5%	0 to 75	168
QD 2125A-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125AL	1K x 1	45	5V ±5%	0 to 75	168
QD 2125AL-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125H-2	1K x 1	25	5V ±5%	0 to 75	168
QD 2125H-3	1K x 1	30	5V ±5%	0 to 75	168
QD 2125H-4	1K x 1	35	5V ±5%	0 to 75	168
QD 2147H	4K x 1	70	5V ±10%	0 to 70	168
QD 2147H-1	4K x 1	35	5V ±10%	0 to 70	168
QD 2147H-2	4K x 1	45	5V ±10%	0 to 70	168
QD 2147H-3	4K x 1	55	5V ±10%	0 to 70	168
QD 2147HL	4K x 1	70	5V ±10%	0 to 70	168
QD 2147HL-3	4K x 1	55	5V ±10%	0 to 70	168
QD 2148H	1K x 4	70	5V ±10%	0 to 70	168
QD 2148H-3	1K x 4	55	5V ±10%	0 to 70	168
QD 2148HL	1K x 4	70	5V ±10%	0 to 70	168
QD 2148HL-3	1K x 4	55	5V ±10%	0 to 70	168
QD2149H	1K x 4	70	5V ±10%	0 to 70	168
QD2149H-2	1K x 4	45	5V ±10%	0 to 70	168
QD2149H-3	1K x 4	55	5V ±10%	0 to 70	168
QD2149HL	1K x 4	70	5V ±10%	0 to 70	168
QD2149HL-3	1K x 4	55	5V ±10%	0 to 70	168


P_6
1
18
+5V
P_5
2
17
P_7
P_4
3
16
P_8
P_3
4
15
P_9
P_0
5
14
P_{10}
P_1
6
13
P_{11}
P_2
7
12
P_{12}
GND
8
11
P_{13}
GND
9
10
GND

210347-6

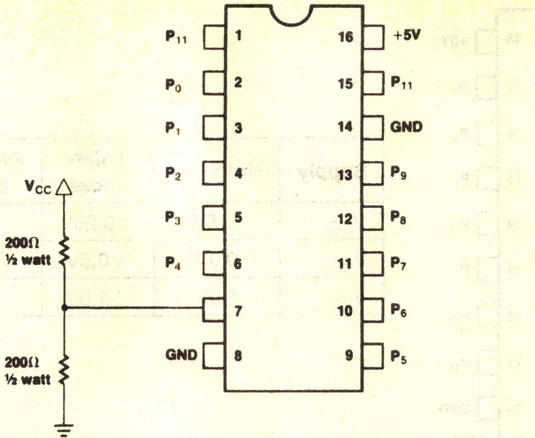
Supply	Voltages	Toler-ances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1	70 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			


*$\overline{\text{RESET}}$
7 µs
5V
0V
*ADD. ADV.
5V
*MUX
0V
7 µs CYCLE TIME

210347-7

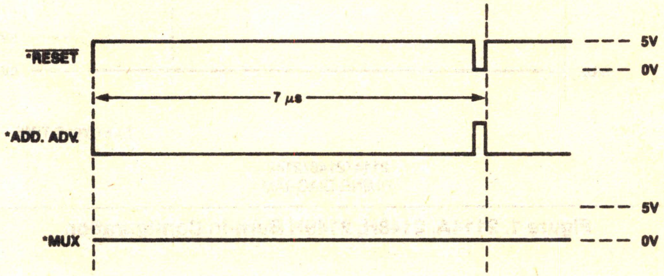
2114/2148/2149
TIMING DIAGRAM

Figure 1. 2114A, 2148H, 2149H Burn-In Configuration


P11
P0
P1
P2
P3
P4
GND
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
+5V
P11
GND
P9
P8
P7
P6
P5
VCC
200Ω ½ watt
200Ω ½ watt

210347-8

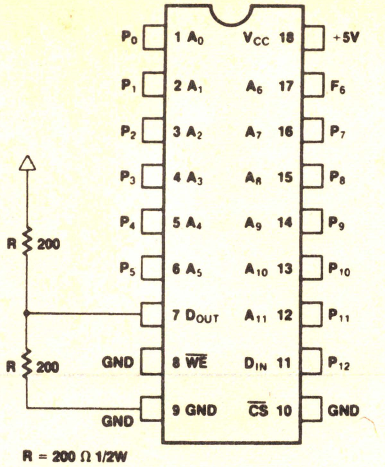
Supply	Voltages	Toler-ances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1st	75 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			


*RESET
7 µs
*ADD. ADV.
*MUX
5V
0V
5V
0V

210347-9

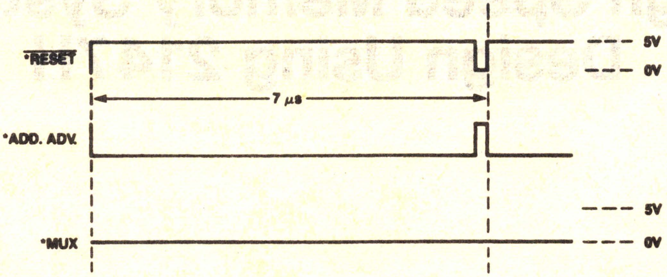
2115/2125 TIMING DIAGRAM
7 µs CYCLE TIME

Figure 2. 2115, 2125 Burn-in Configuration


P0
1 A0
VCC 18
+5V
P1
2 A1
A6 17
F6
P2
3 A2
A7 16
P7
P3
4 A3
A8 15
P8
P4
5 A4
A9 14
P9
P5
6 A5
A10 13
P10
7 DOUT
A11 12
P11
GND
8 WE
DIN 11
P12
9 GND
CS 10
GND
GND
R 200
R 200
R = 200 Ω 1/2W

210347-10

Supply	Voltages	Toler-ances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1	125 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			


*RESET
7 µs
*ADD. ADV.
*MUX
5V
0V
5V
0V

210347-11

2147H
TIMING DIAGRAM
7 µs CYCLE TIME

Figure 3. 2147H Burn-In Configuration

March 1980

High Speed Memory System Design Using 2147H

JOE ALTNETHER
APPLICATIONS ENGINEERING
INTEL CORPORATION

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Order Number: 290080-001

INTRODUCTION

The Intel 2147H is a 4096-word by 1-bit Random Access Memory, fabricated using Intel's reliable HMOS II technology. HMOS II, the second generation HMOS, is Intel's high performance n-channel silicon gate technology, making simple, high speed memory systems a reality. The purpose of this application note is to describe the 2147H operation and discuss design criteria for high speed memory systems.

TECHNOLOGY

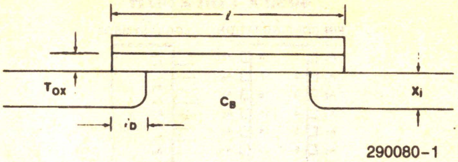
When Intel introduced the HMOS 2147, MOS static RAM performance took a quantum leap by combining scaling, internal substrate bias generation, and automatic powerdown. As a result, the 2147 has an access time of 55 ns, density of 4096 bits, and power consumption of 0.99W active and 0.165W standby.

The high performance of the 2147 is further enhanced by the 2147H using HMOS II, a scaled HMOS process increasing the speed at the same power level which involves more than scaling dimensions.

Figure 1 shows the cross section of an HMOS device and lists the parameters of scaling, one of which is high device gain. The slew rate of an amplifier or device is proportional to the gain. Because faster switching speeds occur with high gain, the gain is maximized for high speed. Device gain is inversely proportional to the oxide thickness (T_{OX}) and device length (ℓ), consequently, scaling these dimensions increases the gain.

Another factor which influences performance is unwanted capacitance which appears in two forms—diffusion and Miller. Diffusion capacitance is directly proportional to the diffusion depth (X_j) into the silicon, thus X_j must be reduced. Miller capacitance, the same phenomenon that occurs in the macro world of discrete devices, is proportional to the overlap length of the gate and the source (ℓ_D). Capacitance on the input shunts the high frequency portion of the input signal so that the device can only respond to low frequencies. Secondly, capacitance from the drain to the gate forms a feedback path creating an integrator or low pass filter which degrades the high frequency performance. This effect is minimized by reducing ℓ_D.

One of the limits on scaling is punch through voltage, which occurs when the field strength is too high, causing current to flow when the device is "turned off." Punch through voltage is a function of channel length (ℓ) and doping concentration (C_B), thus channel shortening can be compensated by increasing the doping concentration. This has the additional advantage of balancing the threshold voltage which was decreased by scaling the oxide thickness for gain.



PERFORMANCE FACTORS

- High Device Gain — Gain $\alpha\, 1/(T_{OX}\ell)$
- Low Diffusion Capacitance — $C_P\ \alpha\ X_j$
- Low Miller Capacitance — $C_m\ \alpha\ \ell_D$
- Low Body Effect — $\Delta V_T\ \alpha\ \sqrt{C_B}\,T_{OX}$

LIMITS

- Punch Through Voltage — $V_{PT}\ \alpha\ C_B\ \ell^2$
- Threshold Voltage — $V_T\ \alpha\ \sqrt{C_B}\,T_{OX}$

RESULT

- Decrease ℓ, T_{OX}, X_j, ℓ_D
- Increase C_B

ℓ = Channel Length
T_{OX} = Oxide Thickness
X_j = Diffusion Depth
ℓ_D = Gate Overlap
C_B = Concentration

Figure 1. HMOS Scaling

Comparison

Comparing scaling theory to HMOS II scaling in Table 1, note that HMOS II agrees with scaling theory except for the supply voltage. It is left constant at +5V to maintain TTL compatibility. Had the voltage been scaled, the power would have been reduced by $1/K^3$ rather than $1/K$, but the device would not have been TTL compatible.

Table 1. Scaling

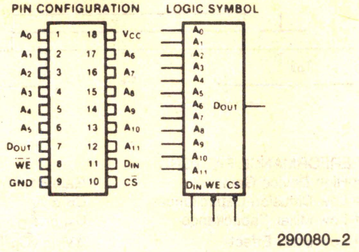
	Theory	HMOS II
Dimensions	1/K	1/K
Substrate Doping	K	K
Voltage	1/K	1
Device Current	1/K	1
Capacitance A/T	1/K	1/K
Time Delay VC/I	1/K	1/K
Power Dissipation VI	$1/K^2$	1
Power Delay Product	$1/K^3$	1/K

THE DEVICE

The 2147H is TTL compatible, operates from a single +5V supply, and is easy to use.

Figure 2 shows the pin configuration and the logic symbol. The 2147H is compatible with the 2147 allowing easy system upgrade. Contained in an industry standard 18-pin dual-in-line package the 2147H is organized as 4096 words of 1 bit. To access each of these

4096 x 1 Bit 2147H


PIN CONFIGURATION
LOGIC SYMBOL
A0 1 18 Vcc
A1 2 17 A6
A2 3 16 A7
A3 4 15 A8
A4 5 14 A9
A5 6 13 A10
DOUT 7 12 A11
WE 8 11 DIN
GND 9 10 CS
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
DOUT
DIN WE CS
290080-2

Pin Names

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

Figure 2. 2147H Logic Diagram

words, twelve address lines are required. In addition, there are two control signals: $\overline{CS}$, which activates the RAM; and $\overline{WE}$, which controls the write function. Separate data input and output are available. Logical operation of the 2147H is shown in the truth table. The output is in the high impedance or three-state mode unless the RAM is being read. Power consumption switches from standby to active under control of $\overline{CS}$.

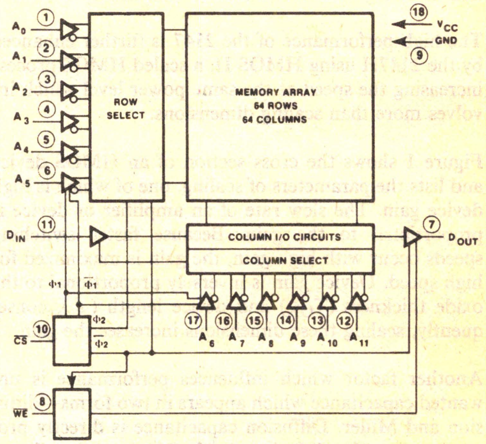
Internal structure of the 2147H is shown in the block diagram of Figure 3. The major portions of the device are: addresses, control ($\overline{CS}$ and $\overline{WE}$), the memory array and a substrate bias generator, which is not shown.

The memory is organized into a two-dimensional array of 64 rows and 64 columns of memory cells. The lower-order six addresses decode one of 64 to select the row while the upper-order six addresses decode to select one column. The intersection of the selected row and the selected column locate the desired memory cell. Additional logic in the column selection circuit controls the flow of data to the array and as stated in the truth table, $\overline{WE}$ controls the output buffer.

As shown in Figure 4, the first three stages of the address buffer are designed with an additional transistor. In each stage, the lowest transistors are the active devices, the middle transistors are load devices, while the upper transistors, controlled by Φ_1, are the key to low standby power. Forming an AND function with the active devices, the upper transistors are turned off when the 2147H is not active, minimizing power consumption. Without them, at least one stage of these cascaded amplifiers would always be consuming power.

The signal Φ_1, and its inverse $\overline{\Phi}_1$, are generated from CS. They are part of an innovative design not found in the earlier 2147. Their function is to minimize the effects at short deselect times on the Chip Select access time, t_{ACS}.

For both the 2147 and the 2147H, access is delayed until the address buffers are activated by chip selection. In the standard 2147, priming during deselection compensates for this delay by speeding up the access elsewhere in the circuitry. For short deselect times, however, full compensation does not occur because priming is incomplete. The result is a pushout in t_{ACS} for short deselect times.


A0 A1 A2 A3 A4 A5
1 2 3 4 5 6
ROW SELECT
MEMORY ARRAY 64 ROWS 64 COLUMNS
18 VCC
9 GND
11 DIN
COLUMN I/O CIRCUITS
COLUMN SELECT
7 DOUT
Φ1 Φ̄1
Φ2 Φ̄2
10 CS
8 WE
17 16 15 14 13 12
A6 A7 A8 A9 A10 A11

Φ_1 Slow deselect, fast select
$\overline{\Phi}_1$ Slow deselect, fast select
Φ_2 Fast deselect, fast select
$\overline{\Phi}_2$ Fast deselect, fast select

290080-3

Figure 3. 2147H Block Diagram

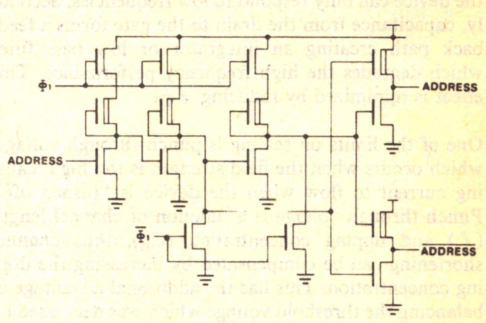
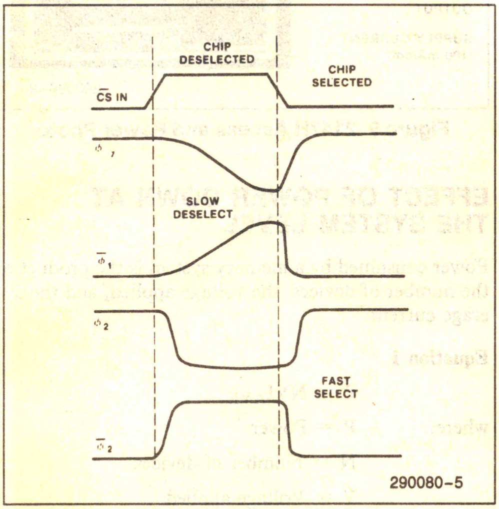

Φ1
ADDRESS
ADDRESS
Φ̄1
ADDRESS
290080-4

Figure 4. Address Buffer

In the 2147H, the address buffers are controlled by Φ_1, which is shaped as shown in Figure 5. Φ_1 activates rapidly for fast select time. However, Φ_1 deactivates slowly, keeping the address buffers active during short deselect times to speed access. As shown in Figure 6, this design innovation keeps t_{ACS} pushout to less than 1 ns.

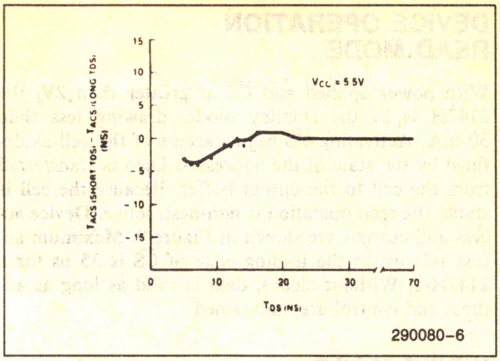

CHIP DESELECTED
CHIP SELECTED
$\overline{CS}$ IN
$\overline{\Phi}_1$
SLOW DESELECT
Φ_1
Φ_2
FAST SELECT
$\overline{\Phi}_2$

290080-5

Figure 5. CS Buffer Signals

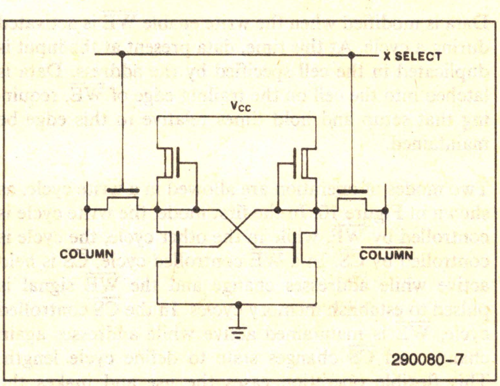
Figure 7 shows the standard six-transistor cell. Configured as a bi-stable flip-flop, the memory cell uses two transistors for loads and two for active devices so that the data is stored twice as true and compliment. The two remaining transistors enable data onto the internal I/O bus. Unlike the periphery, the cell is not powered down during deselect time to sustain data indefinitely.

The 2147H has an internal bias generator. Bias voltage allows the use of high resistivity substrate by adjusting the threshold voltages. In addition, it reduces the effect of bulk silicon capacitance. As a result, performance is enhanced. Bias voltage is generated by capacitively coupling the output of a ring oscillator to a charge pump connected to the substrate. Internally generated bias permits the 2147H to operate from a single +5V supply, maintaining TTL compatibility.



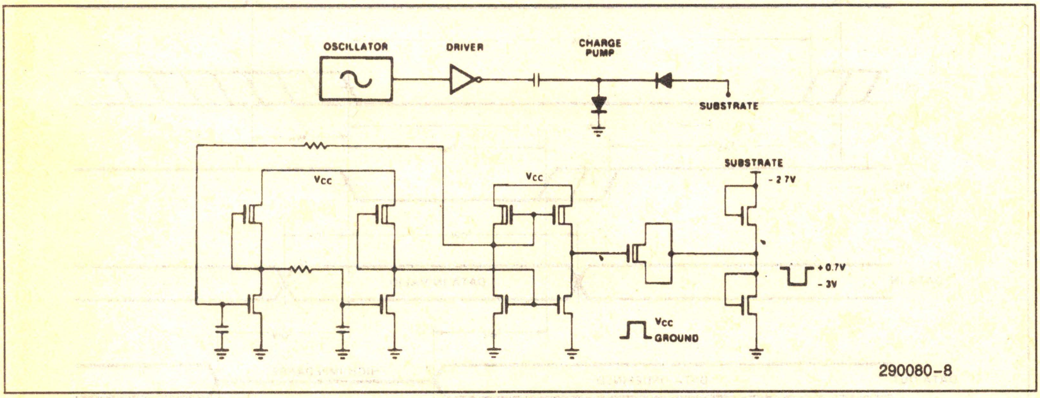
290080-6

Figure 6. CS Access vs. Deselect Time


X SELECT
V_{CC}
COLUMN
$\overline{COLUMN}$

290080-7

Figure 7. 2147H Memory Cell


OSCILLATOR
DRIVER
CHARGE PUMP
SUBSTRATE
V_{CC}
V_{CC}
SUBSTRATE
− 2.7V
+0.7V
− 3V
V_{CC}
GROUND

290080-8

Figure 8. 2147H Substrate Bias Generator

DEVICE OPERATION READ MODE

With power applied and $\overline{\text{CS}}$ at greater than 2V, the 2147H is in the standby mode, drawing less than 30 mA. Activating $\overline{\text{CS}}$ begins access of the cell as defined by the state of the addresses. Data is transferred from the cell to the output buffer. Because the cell is static, the read operation is non-destructive. Device access and current are shown in Figure 9. Maximum access relative to the leading edge of $\overline{\text{CS}}$ is 35 ns for a 2147H-1. Without clocks, data is valid as long as address and control are maintained.

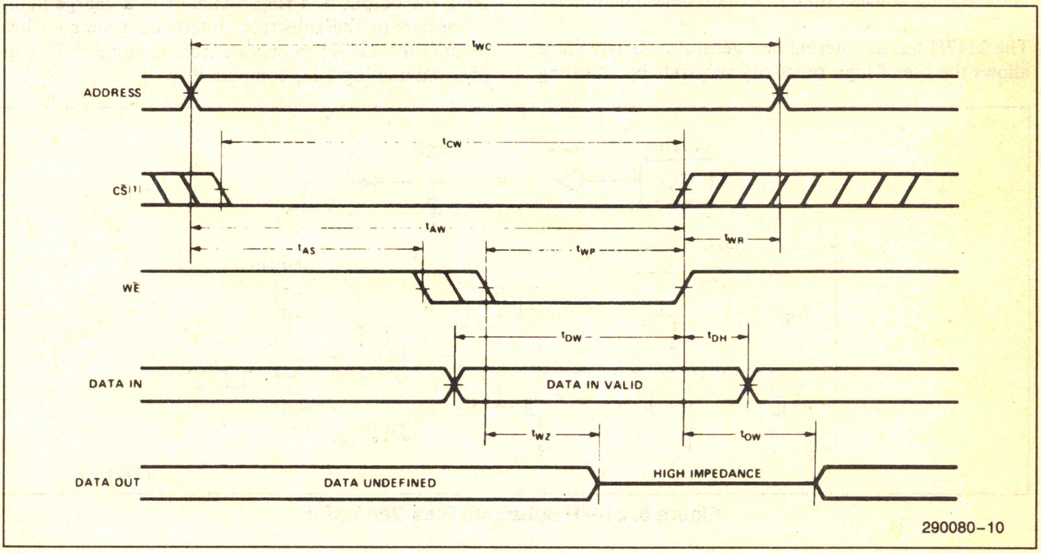
WRITE MODE

Data is modified when the write enable $\overline{\text{WE}}$ is activated during a cycle. At this time, data present at the input is duplicated in the cell specified by the address. Data is latched into the cell on the trailing edge of $\overline{\text{WE}}$, requiring that setup and hold times relative to this edge be maintained.

Two modes of operation are allowed in a write cycle, as shown in Figure 10. In the first mode, the write cycle is controlled by $\overline{\text{WE}}$, while in the other cycle, the cycle is controlled by $\overline{\text{CS}}$. In a $\overline{\text{WE}}$ controlled cycle, $\overline{\text{CS}}$ is held active while addresses change and the $\overline{\text{WE}}$ signal is pulsed to establish memory cycles. In the $\overline{\text{CS}}$ controlled cycle, $\overline{\text{WE}}$ is maintained active while addresses again change and $\overline{\text{CS}}$ changes state to define cycle length. This flexible operation eases the use and makes the 2147H applicable to a wide variety of system designs.

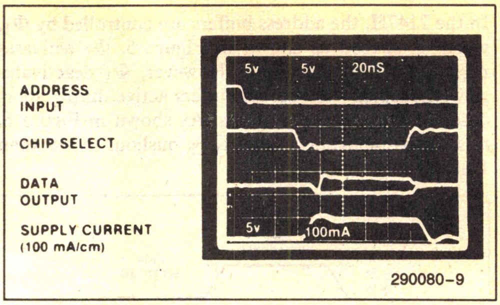
WAVEFORMS

WRITE CYCLE #1 ($\overline{\text{WE}}$ CONTROLLED)



290080-10

Figure 10. Write Cycle Modes of Operation



290080-9

Figure 9. 2147H Access and Power Photo

EFFECT OF POWER DOWN AT THE SYSTEM LEVEL

Power consumed by a memory system is the product of the number of devices, the voltage applied, and the average current:

Equation 1

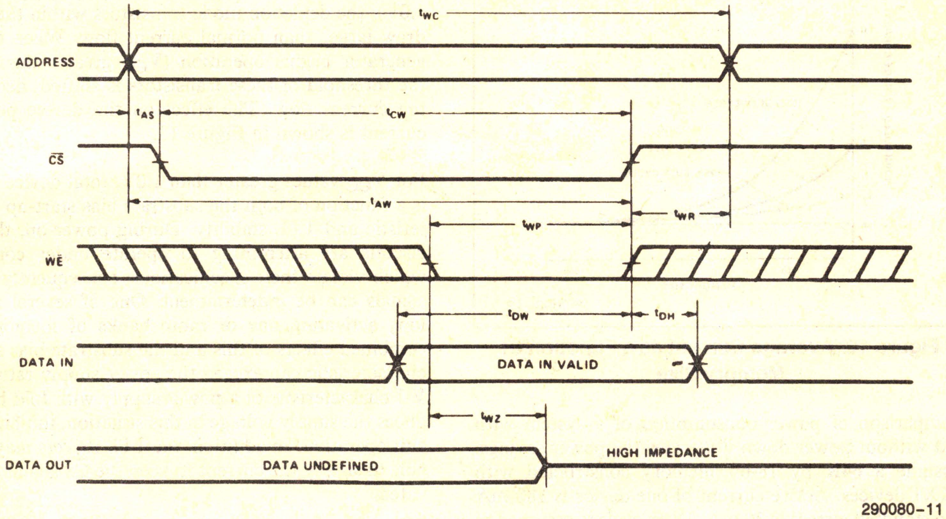
$$P = NVI_{AVE}$$

where:
P = Power
N = Number of devices
V = Voltage applied
I_{AVE} = Average current/device

Without power down, the average current is approximately the operating current. System power increases

WAVEFORMS (Continued)

WRITE CYCLE #2 ($\overline{\text{CS}}$ CONTROLLED)



NOTE:
1. If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance state.

Figure 10. Write Cycle Modes of Operation (Continued)

linearily with the number of devices. With power down, power consumption increases in proportion to the standby current with increasing number of memory devices. Curves in Figure 11 illustrate the difference which results from the majority of devices being in standby with a very small portion of the devices active or being accessed. For a system with power down, the average current of a device in the system is the sum of total active current and the total standby current divided by the number of devices in the system. For an X1 memory such as the 2147H, the number of active devices in most systems will be equal to the number of bits/word, m. Therefore, the number of devices in standby is the difference between N and M. I_{AVE} is expressed mathematically:

Equation 2

$$I_{AVE} = \frac{mI_{ACT} + (N - m)\, I_{SB}}{N}$$

where: m = Number of active devices

I_{ACT} = Active current

I_{SB} = Standby current

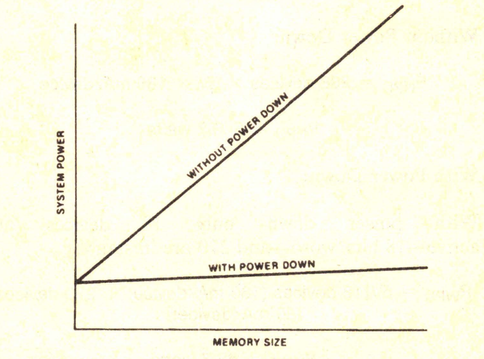
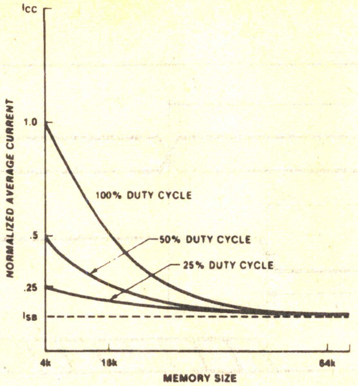


Figure 11. Effect of Power Down at the System

The graph of Figure 12 shows the relation between average device current and memory size for automatic power down. For large memories the average device current approaches the standby current. Total system power usage, P, is calculated by substituting Equation 2 into Equation 1.

$$P = V[mI_{ACT} + (N - m)\, I_{SB}]$$



290080-13

Figure 12. Average Current as a Function of Memory Size

Comparison of power consumption of a system with and without power down illustrates the power savings. Assume a 64K by 18-bit memory constructed with 4KX1 devices. Active current of one device is 180 mA and standby current is 30 mA. Duty cycle is assumed to be 100% and voltage is 5V. The number of devices in the system is:

$$N = \frac{64\text{K words} \times 18 \text{ bits/word}}{4\text{K bit/device}}$$

$$N = 288 \text{ devices}$$

Without Power Down:

$$P_{NPD} = 288 \text{ devices} \times 5\text{V} \times 180 \text{ mA/device}$$

$$P_{NPD} = 259.2 \text{ watts}$$

With Power Down:

With power down only 18 devices are active—18 bits/word—and 270 are in standby.

$$P_{WPD} = 5\text{V}[18 \text{ devices } (180 \text{ mA/device}) + 270 \text{ devices } (30 \text{ mA/device})]$$

$$P_{WPD} = 56.7 \text{ watts}$$

The system with power down devices uses only 22% of the power required by a non-powerdown memory system.

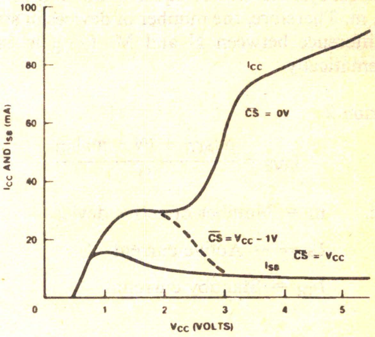
POWER-ON

When power is applied, two events occur that must be considered: substrate bias start up and TTL instability. Without the bias generator functioning (V_{CC} less than 1.0V), the depletion mode transistors within the device draw larger than normal current flow. When the bias generator begins operation (V_{CC} greater than 1.0V), the threshold of these transistors is shifted, decreasing the current flow. The effect on the device power-on current is shown in Figure 13.

For V_{CC} values greater than 1.0V, total device current is a function of both the substrate bias start-up characteristic and TTL stability. During power-on, the TTL circuits are attempting to operate under conditions which violate their specifications; consequently the $\overline{CS}$ signals can be indeterminent. One of several may be low, activating one or more banks of memory. The combined effects of this and the substrate bias start-up characteristic can exceed the power supply rating. The V-I characteristic of a power supply with fold back reduces the supply voltage in this situation, inhibiting circuit operation. In addition, the TTL drivers may not be able to supply the current to keep the $\overline{CS}$ signals deactivated.

One of several design techniques available to eliminate the power-on problem is power supply sequencing. Memory supply voltage and TTL supply voltage are separated, allowing the TTL supply to be activated first. When all the $\overline{CS}$ signals have stabilized at 2.0V or greater, the memory supply is activated. In this mode the memory power-on current follows the curve marked $\overline{CS} = V_{CC}$ in Figure 13.

If power sequencing is not practical, an equally effective method is to connect the $\overline{CS}$ signal to V_{CC} through a 1 KΩ resistor. Although this does not guarantee a 2.0V $\overline{CS}$ input; empirical studies indicate that the effect is the same.



290080-14

Figure 13. 2147H Power Up Characteristic

ARRAY CHARACTERISTICS

When two or more RAMs are combined, an array is formed. Arrays and their characteristics are controlled by the printed circuit card which is the next most important component after the memory device itself. In addition to physically locating the RAMs, the PC board must route power and signals to and from the RAMs.

GRIDDING

A power distribution network must provide required voltage, which from the 2147H data sheet is 5.0V ±10% to all the RAMs. A printed circuit trace, being an extremely low DC resistance, should easily route ±5V DC to all devices. But as the RAMs are operating, micro circuits within the RAMs are switching micro currents on and off, creating high frequency current transients on the distribution network. Because the transients are high frequency, the network no longer appears as a "pure" low resistance element but as a transmission line. The RAMs and the lumped equivalent circuits of the transmission line are drawn in Figure 14. Each RAM is separated by a small section of transmission line both on the +voltage and the −voltage. Associated with the transmission lines is a voltage attenuation factor. In terms of AC circuits, the voltage across the inductor is the change in current—switching transient—multiplied by the inductance.

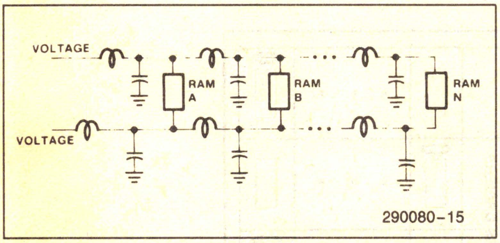


Figure 14. Equivalent Circuit for Distribution

Assuming all RAMs act similarly, the first inductor will see N current transients and the inductor at RAM B sees N-1 transients. The total differential is:

$$\Delta V = \sum_{n=1}^{N} n L \frac{di_n}{dt}$$

That voltage tolerance of ±10% could easily be exceeded with excursions of ±1V not uncommon. Measures must be taken to prevent this. The characteristic impedance of a transmission line is shown in Figure 15A.

Connecting two transmission lines in parallel will halve the characteristic impedance. The result is shown in Figure 15B.

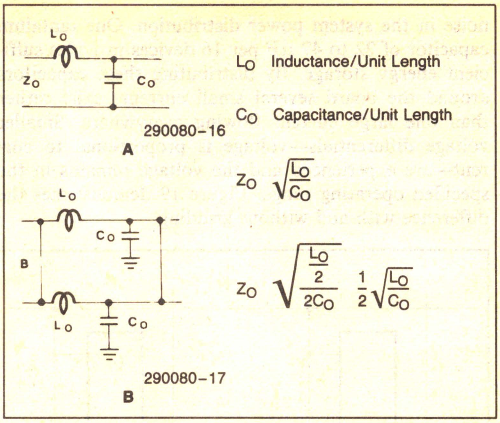

Lo
Zo
Co
Lo Inductance/Unit Length
Co Capacitance/Unit Length
290080-16
A
Zo √(Lo/Co)
Lo
Co
B
Lo
Co
Zo √((Lo/2)/(2Co)) ½√(Lo/Co)
290080-17
B

Figure 15. Transmission Line Characteristic Impedance

Paralleling N traces will reduce the impedance to Z_O/N. Extrapolation of this concept to its limit will result in an infinite number of parallel traces such that they are physically touching, forming an extremely wide, low impedance trace, called a plane. Distribution of power (+ voltage) and ground (− voltage) via separate planes provides the best distribution.

PC boards with planes are manufactured as multilayer boards sandwiching the power and ground planes internally. Characteristics of a multilayer board can be cost effectively approximated by gridding the power and ground distribution. Gridding surrounds each device with a ring of power and ground distribution forming many parallel paths with a corresponding reduction of impedance. Gridding is easily accomplished by placing horizontal traces of power (and ground) on one side of the PC board and vertical traces on the other, connected by plated through holes to form a grid.

Viewed from the top of the PC board, the gridding as in Figure 16 surrounds each device. Pseudo-gridding techniques such as serpentine or interdigitated distribution, as in Figure 17, are not effective because there are no parallel paths to minimize the impedance.

DECOUPLING

One final aspect of power/ground distribution must be considered—decoupling.

Decoupling provides localized charge to minimize instantaneous voltage changes on the power grid due to current changes. These transient current changes are local and high frequency as devices are selected and deselected. Adequate decoupling for the 2147H is accomplished by placing a 0.1 μf ceramic capacitor at every other device as shown in Figure 18. Bulk decoupling is included on the board to filter low frequency noise in the system power distribution. One tantalum capacitor of 22 to 47 μF per 16 devices provides sufficient energy storage. By distributing these capacitors around the board several small currents exist rather than one large current flowing everywhere. Smaller voltage differentials—voltage is proportional to current—are experienced and the voltage remains in the specified operating range. Figure 19 demonstrates the difference with and without gridding.

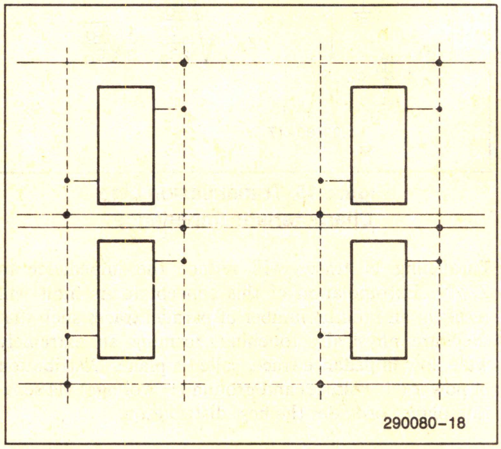


Figure 16. Gridding Plan

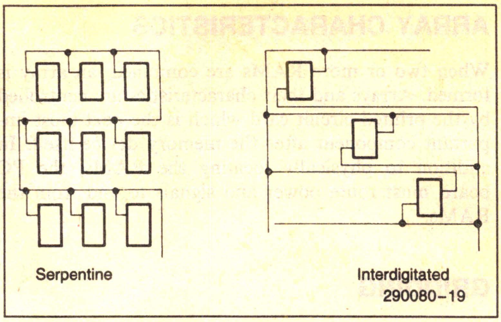


Figure 17. Pseudo-Gridding Techniques

TERMINATION

Similar reasoning is applied to the AC signals: address, control, and data. While they are not gridded or decoupled, they must be kept short and terminated. Similar to the power trace, the signal trace will have transmission line characteristics. A simplified circuit is shown in Figure 20.

MOS RAM input is essentially capacitive. Simplifying the capacitance and writing the differential equation.

$$\partial = \frac{Ldi}{dt} + \frac{1}{C}\int idt$$

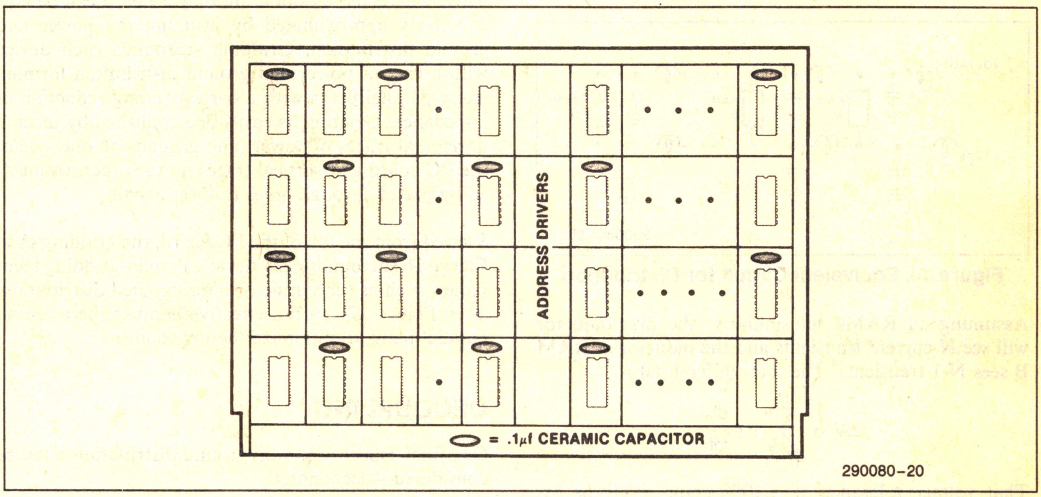
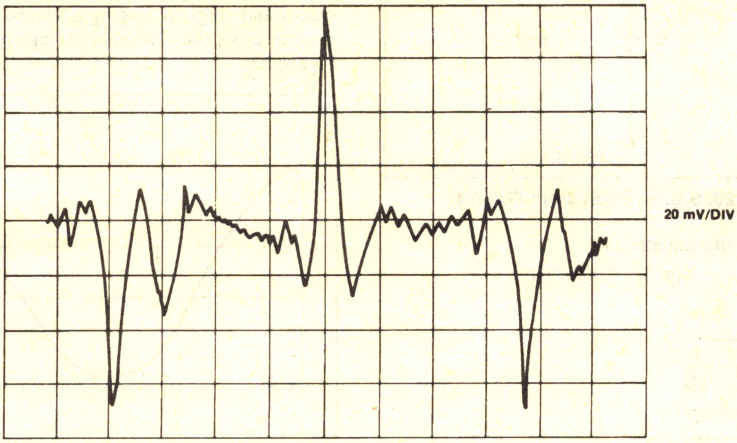


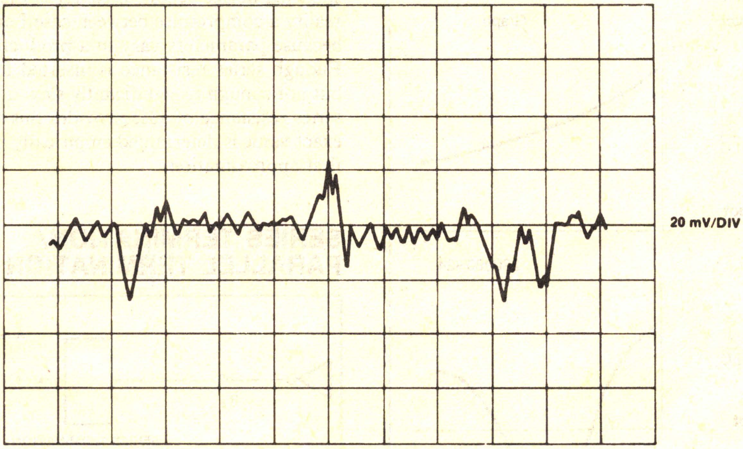
Figure 18. Decoupling

V_{CC} Noise Without Gridding and One Decoupling Capacitor Per 4 RAMs



290080-21

V_{CC} Noise With Gridding and One Decoupling Capacitor Per 2 RAMs



290080-22

Figure 19. V_{CC} Noise With and Without Gridding

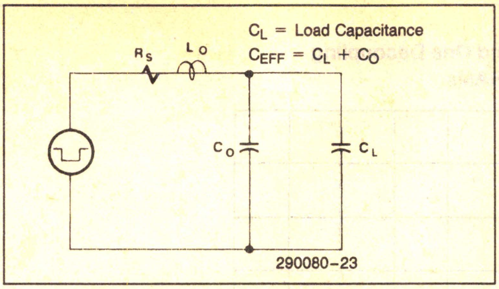


Figure 20. Signal Equivalent Circuit

The solution of this equation is:

$$i = K_1e^{-r_1t} + K_2e^{-r_2t}$$

where:

$$r_1 = \frac{R}{2L} + \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$$

$$r_2 = \frac{R}{2L} - \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$$

K_1 = constant
K_2 = constant

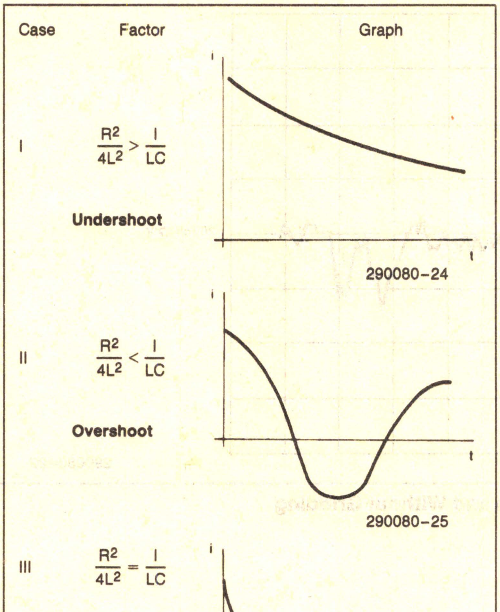


Figure 21. Three Cases of Equation Solution

Dependent on the values of R, L and C, there are three cases shown in Figure 21. In case I, rise and fall times are excessively long. In case III, the current smoothly and clearly changes, while in case II, the current overshoots and rings. If ringing is severe enough, the voltage can cross the threshold voltage of the device as in Figure 22.

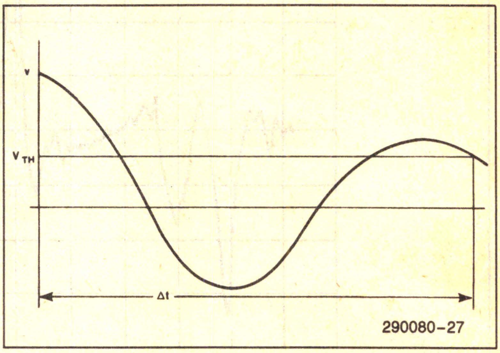


Figure 22. Access Push-Out Due to Ringing

Effective access is stretched out until the wave form settles. System access is the settling time (Δt) plus the specified device access. Case III is the ideal case but in reality a compromise between case I and case II is used because parameters vary in a production environment. Enough series resistance is inserted to prevent ringing but not enough to significantly slow down the access. A series resistance of 33Ω provides this compromise. The exact value is determined empirically but 33Ω is a good first approximation.

SERIES TERMINATION/ PARALLEL TERMINATION

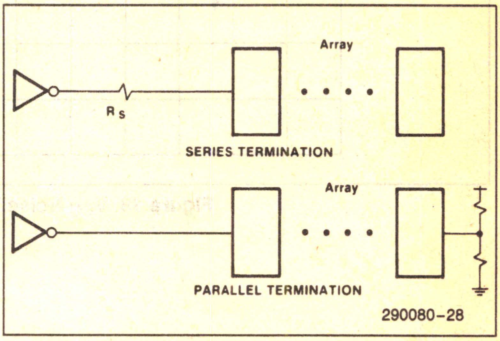


Figure 23. Series and Parallel Termination

Series termination uses one resistor and consumes little power. Current through the resistor creates a voltage differential shifting the levels of input voltage to the devices slightly. This shift is usually insignificant because the 2147H has an extremely high input impedance.

Termination could also be accomplished by a parallel termination as shown in Figure 23. Parallel termination has the advantage of faster rise and fall times but the disadvantage of higher power consumption and increased board space usage.

SYSTEM DELAYS

RAMs are connected to the system through an interface, comprised of address, data and control signals. Inherent in the interface is propagation delay. Added to the RAM access time, propagation delay lengthens system access time and hence system cycle time. Expressed as an equation:

$$t_{sa} = t_{da} + t_{pd}$$

where: t_{sa} = system access time

t_{da} = device access time

t_{pd} = propagation delay

Device access is a fixed value, guaranteed by the data sheet. System efficiency then, is a function of system access and can be expressed as:

$$\mathrm{Eff} = t_{da}/t_{sa}$$

where: Eff = System Efficiency

This can be reduced by substitution for t_{sa} to:

$$\mathrm{Eff} = 1/(1 + t_{pd}/t_{da})$$

System efficiency is maximized when propagation delay is minimized. With sub 100 ns access RAMs, efficiency can be reduced to 40–60% because delay through the signal paths is significant when compared to RAM access. Three factors contribute to the delay: logic delay, capacitive loading, and transit time.

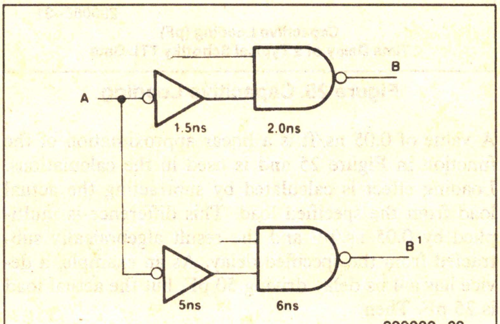
LOGIC DELAY

The delay through a logic element is the time required for the output to switch with respect to the input. Actual delay times vary. Maximum TTL delays are specified in catalogs, while minimum delays are calculated as one-half of the typical specification. As an example, a gate with a typical delay of 6 ns has a minimum delay of 3 ns.

A signal propagating through two logically identical paths but constructed from different integrated circuits will have two different propagation times. For example, in Figure 24A one path has minimum delays while the other has maximum delays. Path A-B has a delay of 3.5 ns while A-B^1 has a delay of 11 ns. The time difference between these two signals is skew, which will be important later in the system design. Figure 24B shows skew values for several TTL devices.

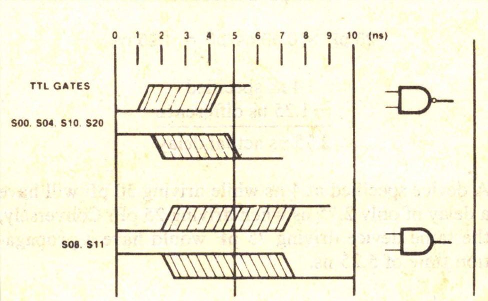
CAPACITIVE LOADING

Delay time is also affected by the capacitive load on the device. Typical delay as a function of capacitive load is shown in Figure 25. TTL data sheets specify the delay for a particular capacitive load (typically 15 pF or 50 pF). Loads greater than specified will slow the device; similarly, loads less than specified will speed up the device.



290080-29

Figure 24A



290080-30

Figure 24B. Skew

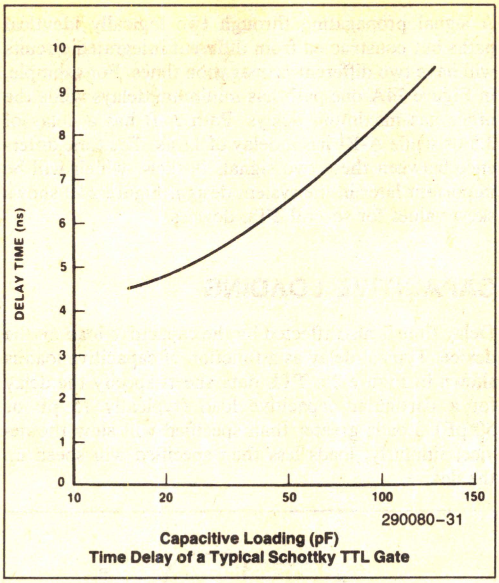


Figure 25. Capacitive Loading

A value of 0.05 ns/ft is a linear approximation of the function in Figure 25 and is used in the calculations. Loading effect is calculated by subtracting the actual load from the specified load. This difference is multiplied by 0.05 ns/pF and the result algebraically subtracted from the specified delay. As an example, a device has a 4 ns delay driving 50 pF, but the actual load is 25 pF. Then,

$$\begin{array}{r} 50\text{ pF specified} \\ -25\text{ pF actual} \\ \hline 25\text{ pF difference} \end{array}$$

$$25\text{ pF} \times 0.05\text{ ns/pF} = 1.25\text{ ns}$$

$$\begin{array}{r} 4\text{ ns specified} \\ -1.25\text{ ns difference} \\ \hline 2.75\text{ ns actual delay} \end{array}$$

A device specified at 4 ns while driving 50 pF will have a delay of only 2.75 ns when driving 25 pF. Conversely, the same device driving 75 pF would have a propagation time of 5.25 ns.

TRANSIT TIME

Signal transit time, the time required for the signal to travel down the PC trace, must also be considered. As was shown in Figure 19, these traces are transmission lines. Classical transmission line theory can be used to calculate the delay:

$$t_p = \sqrt{LC}$$

where: t_p = Travel Time
L = Inductance/unit length of trace
C = Capacitance/unit length of trace

The capacitance term in the equation is modified to include the sum of the trace capacitance and the device capacitance. This equation approximates in the worst case direction; a signal will never "see" all the load capacitance simultaneously, it is distributed along the trace at the devices.

Substituting into the equation:

$$tp^1 = \sqrt{L(C + C_L)}$$

where: tp^1 = Modified delay
C_L = Load capacitance

Algebraically:

$$tp^1 = \sqrt{LC(1 + C_L/C)}$$

$$tp^1 = \sqrt{LC}\sqrt{1 + CL/C}$$

and

$$tp^1 = tp\sqrt{1 + CL/C}$$

Empirically, tp is 1.8 ns/ft for G-10 epoxy and C is 1.5 pF/in. For a 5-in. trace and a 40 pF load, the delay is calculated to be 4.5 ns. Because this is worst case, an approximated 2 ns/ft can be used. In the following sections, however, the equation will be used. Total delay is the summation of all the delays. Adding the device access, TTL delays and the trace delays result in the system access.

BOARD LAYOUT

The preceding section discussed the effects of trace length and capacitive loading. Proper board layout minimizes these effects.

As shown in Figure 26, address and control lines are split into a right and left hand configuration with these signals driving horizontally. This configuration minimizes propagation delay. Splitting the data lines is not necessary, as the data loads are not as great nor are their traces as long as address and control lines. Control and timing fills the remaining space.

Two benefits are derived from this layout. First, the address and control lines are perpendicular to the data lines which minimizes crosstalk. Second, troubleshooting is simplified. A failing row of devices indicates a defective address or control driver; whereas a failing column indicates a faulty data driver.

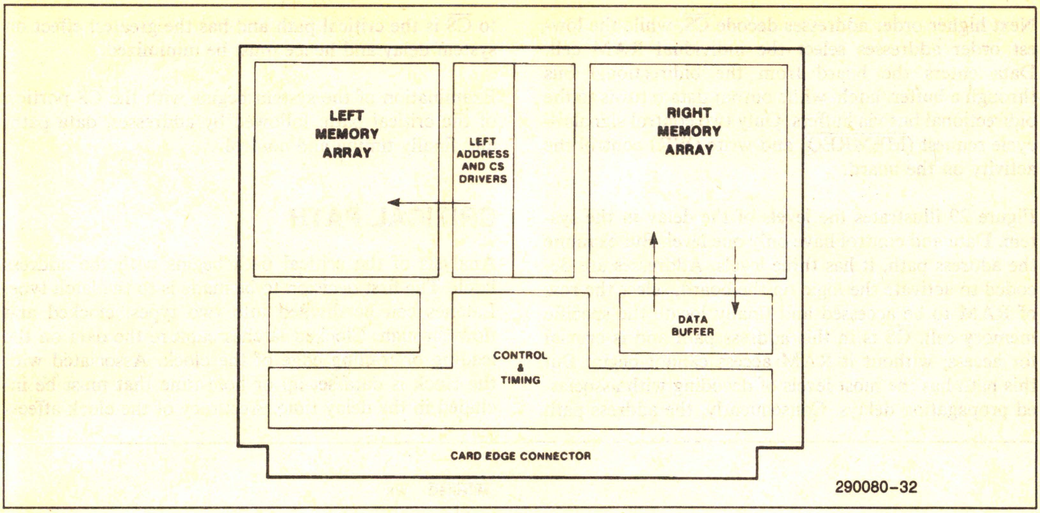

LEFT MEMORY ARRAY
LEFT ADDRESS AND CS DRIVERS
RIGHT MEMORY ARRAY
DATA BUFFER
CONTROL & TIMING
CARD EDGE CONNECTOR
290080-32

Figure 26. Board Layout

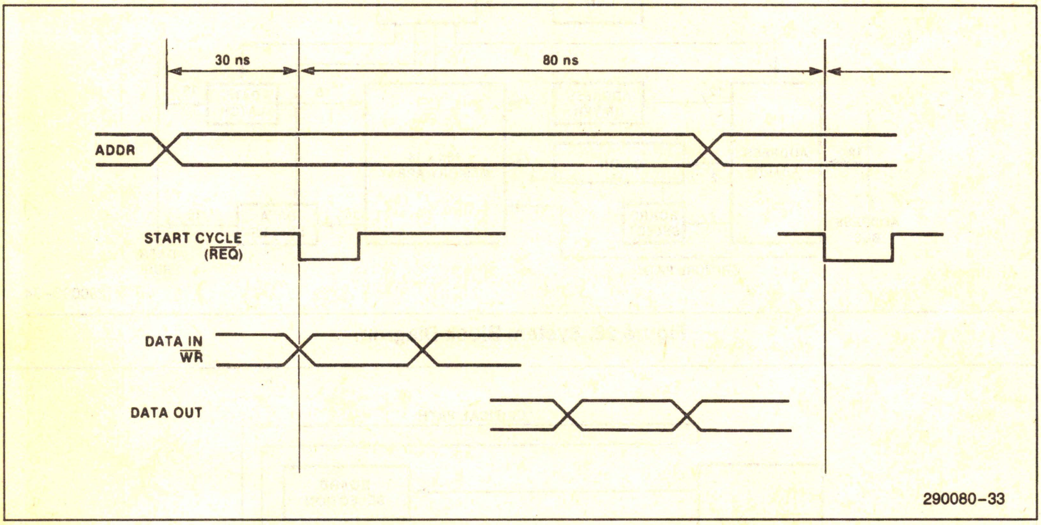

30 ns
80 ns
ADDR
START CYCLE (REQ)
DATA IN WR
DATA OUT
290080-33

Figure 27. System Timing

SYSTEM DESIGN

Using previously discussed rules and guidelines, the design of a typical high speed memory will be reviewed to illustrate these techniques. Configuration of the system is a series of identical memory cards containing 16K words of 16 bits. Timing and control logic is contained on each board. System timing requires an 80 ns cycle as shown in Figure 27. Cycle operation begins when data and control signals arrive at the board. In this design, addresses are shifted 30 ns to be valid before the start of the cycle so that address, data, and control arrive at the memory device at the same time for maximum performance. Data and control signals are coincident with the start of the cycle. Access is not yet specified because it is affected by device access and the unknown propagation delay. Access will be determined in the design.

Figure 28 illustrates the elements of the system in block diagram form. Addresses are buffered and latched at the input to the printed circuit card. Once through the latch, the addresses split to perform three functions: board selection, chip select (CS) generation, and RAM addressing. Highest order addresses decode the board select, which enables all of the board logic including CS.

Next higher order addresses decode $\overline{CS}$, while the lowest order addresses select the individual RAM cell. Data enters the board from the bidirectional bus through a buffer/latch, while output data returns to the bidirectional bus via buffers. Only two control signals—cycle request ($\overline{MEMREQ}$) and write ($\overline{WR}$) control the activity on the board.

Figure 29 illustrates the levels of the delay in the system. Data and control have only one level. But examine the address path, it has three levels. Addresses are decoded to activate the logic on the board, select the row of RAM to be accessed and finally locate the specific memory cell. $\overline{CS}$ is in this address path and is crucial for access; without it RAM access cannot begin. But this path has the most levels of decoding with associated propagation delays. Consequently, the address path to $\overline{CS}$ is the critical path and has the greatest effect on system delay and hence must be minimized.

Examination of the system begins with the $\overline{CS}$ portion of the critical path, followed by addresses, data path, and finally timing and control.

CRITICAL PATH

Analysis of the critical path begins with the address latch. The first decision to be made is to the latch type. Latches can be divided into two types: clocked and flow-through. Clocked latches capture the data on the leading or trailing edge of the clock. Associated with the clock is data set-up or hold-time that must be included in the delay time. Accuracy of the clock affects

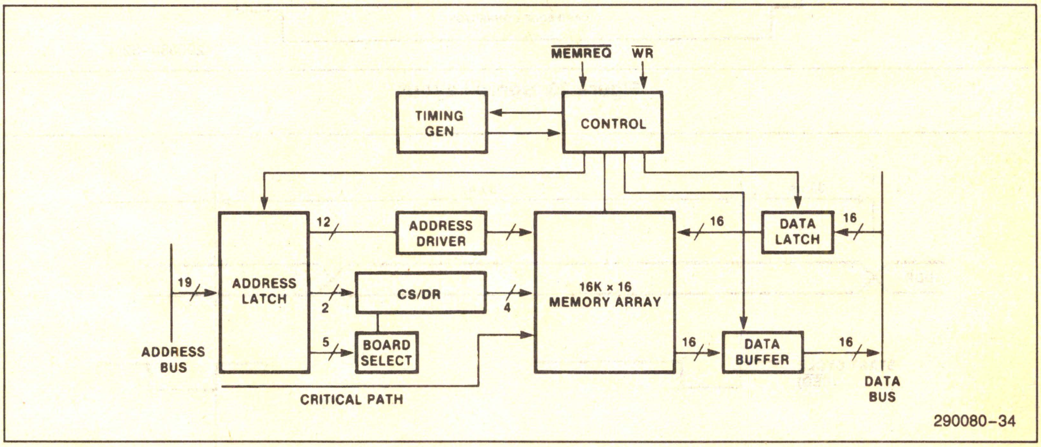

MEMREQ
WR
TIMING GEN
CONTROL
ADDRESS LATCH
12
ADDRESS DRIVER
19
ADDRESS BUS
2
CS/DR
4
5
BOARD SELECT
16K × 16 MEMORY ARRAY
16
DATA LATCH
16
16
DATA BUFFER
16
DATA BUS
CRITICAL PATH
290080-34

Figure 28. System Block Diagram

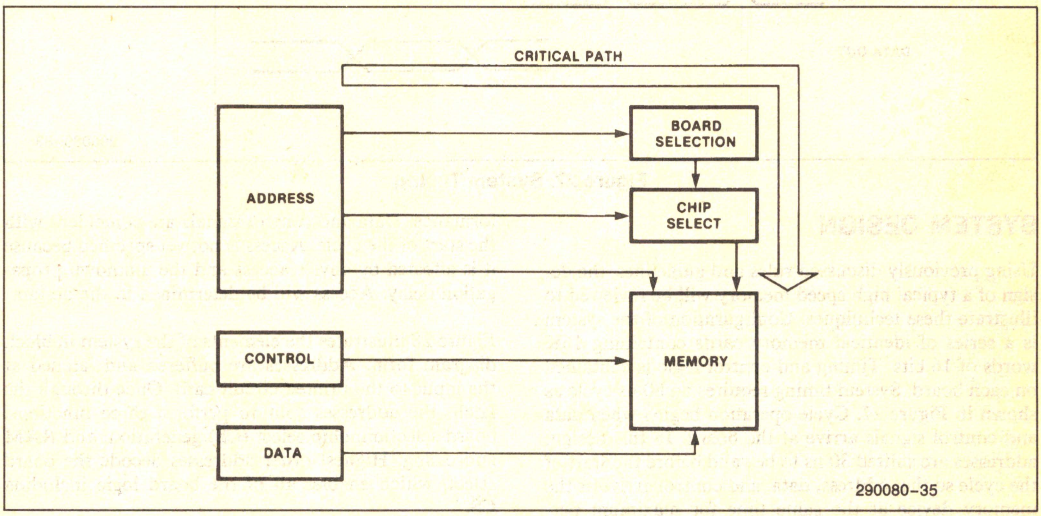

CRITICAL PATH
ADDRESS
BOARD SELECTION
CHIP SELECT
CONTROL
MEMORY
DATA
290080-35

Figure 29. Worst Case Delay Path

the transit time of the signal because any skew in the clock adds to the delay time. As an example, a typical 74S173 latch has a data set-up time of 5 ns and a maximum propagation delay time from the clock of 17 ns. Total delay time is 22 ns, excluding any clock skew.

Flow-through latches have an enable rather than clock. The enable opens the address window and allows addresses to pass independent of any clock. Delay time is measured from the signal rather than a clock. The Intel 3404 is a high speed, 6-bit latch operating in a flow-through mode with 12 ns delay. This is acceptable but a faster latch can be fashioned using a 2-to-1 line multiplexer, either a 74S157 or a 74S158. The slower of the two is the 74S157 with 7.5 ns delay. Although the 74S158 is faster with 6 ns delay, it requires an extra inverter in the feedback path as shown in Figure 30. Between the 74S157 and the 74S158 latches, the trade off is speed against board space and power. Individual designers will choose to optimize their designs.

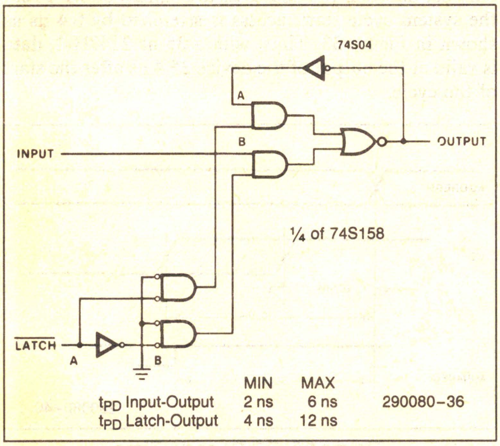


Figure 30. Fast Latch

In either case, care must be exercised in constructing the latch. Output data must be fed back to the input having the shortest internal path—the A input. If the latch is constructed with the output strapped to the B input, the input could be deselected and the feedback loop not yet selected because of the delay through the internal inverter. In this situation data would be lost. Additional delay through the external inverter (74S04) aids in preventing data loss. Inverting addresses has no system effect—except that it's faster than the non-inverting latch. During a write cycle, data will be stored at the compliment of the system address. When this data is to be retrieved, the same address will be complimented, fetching the correct word.

The remaining elements in the critical path to be designed are board selection and $\overline{\text{CS}}$ decoding. To minimize the $\overline{\text{CS}}$, decode path, the easiest method is to work backwards from $\overline{\text{CS}}$. In this manner input signals to a stage are determined and the output from the preceding stage is defined. This saves inserting an inverter at the cost of 5 ns to generate the proper input to a stage.

Starting with the $\overline{\text{CS}}$ driver, the design analyzes several approaches to select the fastest one. With four rows of devices, there are four $\overline{\text{CS}}$ signals to be generated. A 2-to-4 line decoder like the 74S138 is a possible solution. It is compact, but has two detriments: long propagation delay and insufficient drive capability. Propagation delay from enable is 11 ns. Enable is driven by board selection which arrives later than the binary inputs. Splitting the RAMs into two 4 x 8 arrays eases the drive requirement but the demultiplexer must still drive eight devices at 5 pF each—or 40 pF total—which adds 1.75 ns to the delay. More importantly, signal drive is required to switch cleanly and maintain levels in spite of crosstalk and reflections. A 74S240 buffer will solve this but in the process consumes an additional 9 ns.

A second and preferred approach is to use a discrete decoder to decode and Drive the $\overline{\text{CS}}$ signals. Four input NAND buffers—74S40—fulfill this function. Addresses A_{12} and A_{13} are inverted via 74S04, providing true and compliment signals to the buffer for decoding. As shown in Figure 31, the delay is 11.5 ns. Propagation delay for the 74S40 is specified into a 50 pF load, eliminating the additional loading delay. Left and right drivers—CSXL and CSXR—are in the same package to minimize skew between left and right bytes of data. All of the decoders are enabled by Board Select to prevent rows of devices on several boards from being simultaneously active. Board Select is a true input, defining the output from the Board Select decoder.

In the Board Select decoder, the high order addresses are matched to hard-wired logic levels generated with switches for flexibility. Changing a switch setting shifts the 16K range of the board. Comparison of the switch setting and the address can be accomplished with an exclusive-OR, a 74S86. NANDing all the exclusive-OR outputs will generate a Board Select signal. Unfortunately, this signal is active-low, requiring an additional inverter as in Figure 32A, and it also consumes 22.5 ns to decode. An MSI solution to board selection is a 4-bit comparator—74S85—which consumes less board area and propagation delay is improved at 16.5 ns.

The best solution is attained by inverting the high order addresses to generate true and compliment signals. The appropriate signal is connected into a 74S260, 5-input NOR. With an active-high output, maximum delay is 11 ns as in Figure 32B.

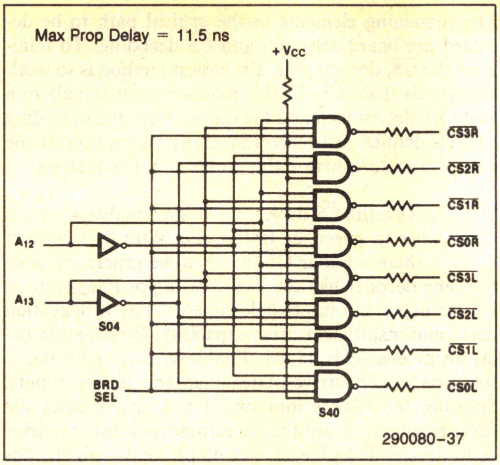
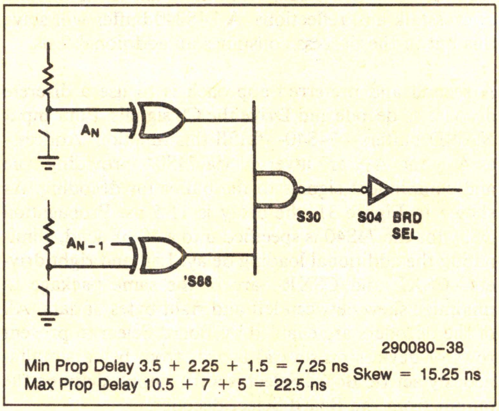
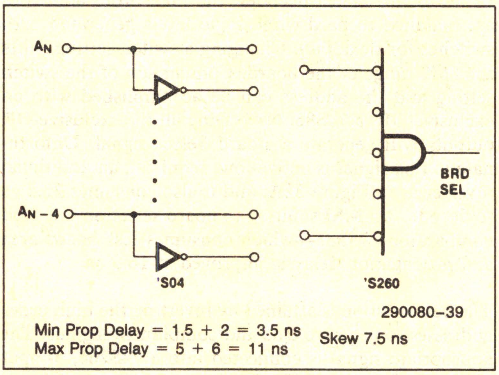


Figure 31. $\overline{\text{CS}}$ Decode



Min Prop Delay 3.5 + 2.25 + 1.5 = 7.25 ns
Max Prop Delay 10.5 + 7 + 5 = 22.5 ns
Skew = 15.25 ns

Figure 32A



Min Prop Delay = 1.5 + 2 = 3.5 ns
Max Prop Delay = 5 + 6 = 11 ns
Skew 7.5 ns

Figure 32B. Board Select

Critical path timing is the sum of the latch, Board Select, and $\overline{\text{CS}}$ delay times. In this example, latch delay is 6 ns, Board Select is 11 ns and $\overline{\text{CS}}$ decode is 11.5 ns for a total of 28.5 ns. One additional delay—trace delay—must be included for a complete solution. Each 74S40 drives eight MOS inputs having 5 pF/device for a load of 40 pF. Trace capacitance is calculated on 5 in. of trace. At 1.5 pF/in., trace capacitance is 7.5 pF. Trace delay calculated from equation 3 is 1.9 ns.

$$tp^1 = \frac{1.8 \text{ ns}}{\text{ft}} \times \frac{5 \text{ in.}}{12 \text{ in./ft}} \sqrt{1 + \frac{40 \text{ pF}}{7.5 \text{ pF}}}$$

$$tp^1 = 1.9 \text{ ns}$$

Total worst case maximum critical path delay has been calculated to be 30.4 ns (28.5 ns + 1.9 ns). With the addresses shifted in time by an amount equal to the worst case delay, device and system cycle start are coincident. Start of system access and device access differ only 0.4 ns when the addresses are shifted 30 ns. From the system cycle start, access is stretched by 0.4 ns as shown in Figure 33. Thus, with a 35 ns 2147H-1, data is valid at the output of the device 35.4 ns after the start of the cycle.

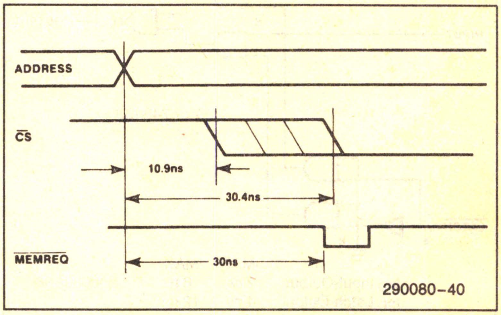


Figure 33. $\overline{\text{CS}}$ Decode Time

The minimum delay also must be calculated. With addresses valid prior to the start of the cycle, $\overline{\text{CS}}$ decoding can start in the previous cycle. If it occurs too soon, the previous cycle will not be properly completed. Minimum delay time is the sum of the minimum propagation delays plus capacitive loading delay plus trace delay. Capacitive loading delay is less than 0.4 ns and ignored. Minimum delay through the TTL is 9 ns, and added to trace delay results in a total of 10.9 ns.

From address change, the maximum delay in the critical path is 30.4 ns while the minimum is 10.9 ns. The difference between these two times is skew and will be important in later calculations.

ADDRESSES

Lower order addresses (A_0-A_{11}) arrive at the devices earlier than $\overline{CS}$ because they are not decoded. Consequently, the address drivers do not have a critical speed requirement. Once through the 6 ns latch, addresses have 24 ns to arrive at the devices.

While speed is not the primary prerequisite, drive capability is. Address drivers are located in the center of the board, dividing the array into two sections of 32 devices each. For the moment, assume one driver drives 32 devices as in Figure 34A. Each device is rated at 5 pF/input, resulting in a load of 160 pF. In addition, there are four 5-in. traces—one for each row. Twenty inches of trace equates to 30 pF. Total capacitive load is 190 pF. A 74S04 is specified at 5 ns delay into 15 pF. The increased capacitive load is 175 pF, which at 0.05 ns/pF increases the delay by 8.75 ns. Under these conditions the worst case driver relay is 5 ns plus 8.75 ns, totaling 13.75 ns. It is 10 ns earlier than the 24 ns available.

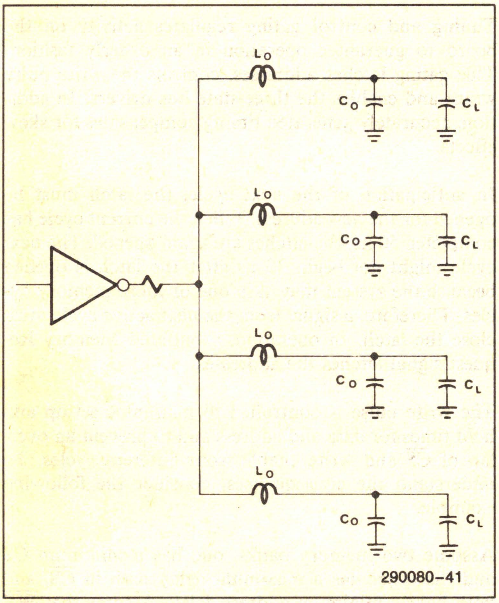


Figure 34A. Address Driver

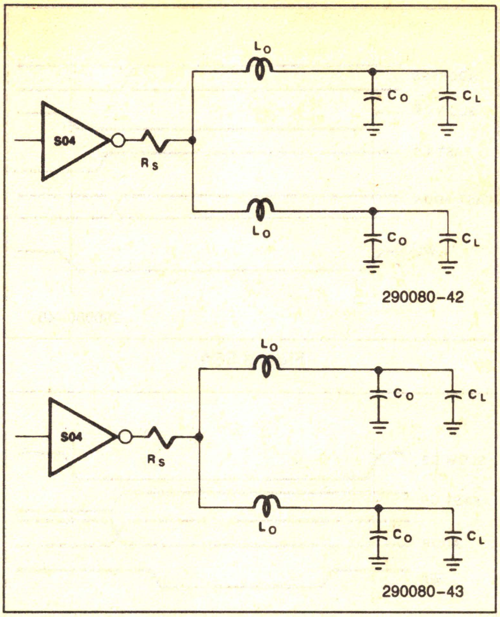


Figure 34B. Address Drivers

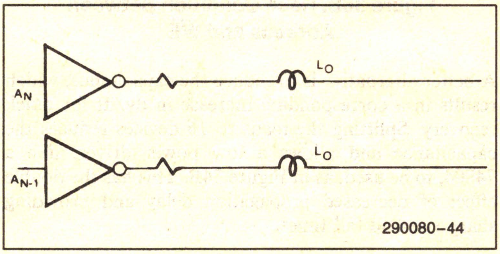


Figure 35. Cross Talk

The first impression is that this is sufficient, but the effect of crosstalk must be considered. For example, as shown in Figure 35, each trace has inductance, and parallel traces take on the characteristics of transformers. When a signal switches from a one level to a zero level, its driver can sink 20 mA, inducing a transient in an adjacent trace. If the adjacent signal is switching to a one level, only 400 μA of a source current from the driver is available. The induced current will generate a negative spike, driving the signal at a one level negative. Additional time of 10 ns to 15 ns is required to recover and re-establish a stable one level. This may prevent stable address at the start of the cycle. Recall:

$$i = C\frac{dv}{dt} \text{ or } dt = C\frac{dv}{i}$$

where: i = instantaneous current

C = capacitance

$\frac{dv}{dt}$ = voltage time rate of change

The term dv/dt can be maximized by increasing i or decreasing C. Current can be doubled by using a driver like a 74S240, but it draws 150 mA supply current. In a large system the increased power is a disadvantage because it requires a larger power supply and additional cooling.

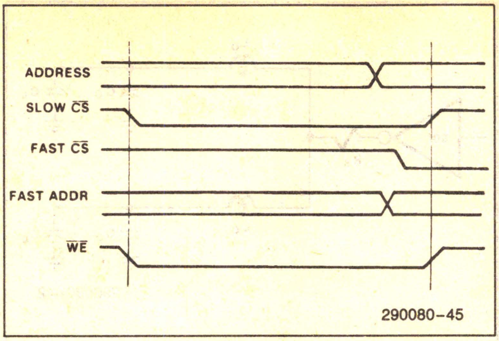


Figure 36A

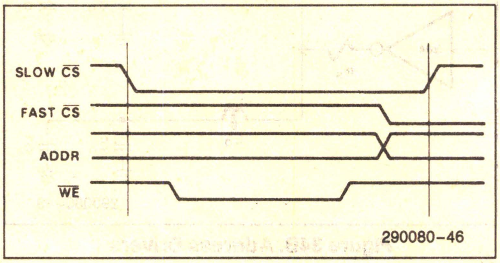


Figure 36B. Race Condition Between Address and $\overline{WE}$

A better alternative is to reduce the capacitance, which results in a corresponding increase in dv/dt for quick recovery. Splitting the loads to 16 devices reduces the capacitance and allows a low power driver, like a 74S04, to be used, as in Figure 34B. This has the double effect of decreased propagation delay and providing sharp rise and fall times.

Now, there are only 10 in. of trace or 15 pF load and 16 devices, representing 80 pF for a total of 95 pF. Again, the S04 delay is 5 ns into 15 pF, but the stretched delay due to 80 pF is only 4.0 ns for a total of 9.0 ns. Stable addresses are guaranteed at the start of the cycle.

DATA PATH

Next in line for analysis is the data path. Reference to the system block diagram shows that the data is latched into the board on a write cycle and buffered out during a read cycle. Data latches are constructed from 74S158 quad two-input multiplexers. Because the data bus is bidirectional, 74S240 three-state drivers are used for output buffers.

All that remains to complete the board access computation is the calculation of the output propagation delay. Output delay of the active RAM is caused by the capacitance loading of its own output plus the three idle RAMs, the input capacitance of the 74S240 bus driver and trace capacitance. Output capacitance of the 2147Hs is 6 pF/device for a subtotal of 24 pF; input capacitance of the 74S240 is 3 pF and trace capacitance of a 5-in. trace is 7.5 pF. Total load capacitance is 34.5 pF, and access time of the 2147H is specified driving a 30 pF load. Calculated loading is close enough to the specified loading to eliminate any significant effect on the access calculations. Had there been a difference, the effect would have been included in the calculation. As previously calculated, transit time of the trace is 1.6 ns. Adding this to the 7 ns delay through the 74S240 bus driver results in an 8.6 ns output propagation delay from the RAM output to the bus.

Total access is 35.4 ns plus 8.6 ns output delay for a total access of 44 ns. The efficiency of this system is:

$$\text{Eff} = \frac{35}{44} \text{ or } 80\%$$

TIMING AND CONTROL

Timing and control gating regulates activity on the board to guarantee operation in an orderly fashion. This gating latches addresses, controls the write pulse width and enables the three-state bus drivers. In addition, accurately generated timing compensates for skew effects.

In anticipation of the next cycle, the latch must be opened for the new address. When the current cycle has completed 50 ns, the latches are again opened. The next cycle might not begin 30 ns after the latch is opened because the system may skip one or more memory cycles. Therefore, a signal from the next active cycle must close the latch. In operation, a buffered Memory Request signal latches the addresses.

The write pulse is controlled to guarantee set-up and hold times for data and address and to prevent an overlap of $\overline{CS}$ and write enable from different cycles. To understand the consequences, consider the following example.

Assume two memory banks, one has a minimum $\overline{CS}$ and the other has a maximum delay path in $\overline{CS}$, and both have a minimum address delay. Assume that $\overline{WE}$ is a level generated from a write command as shown in Figure 36A. The operation under examination is a write cycle into the bank with fast $\overline{CS}$ followed by a read cycle into the bank with slow $\overline{CS}$.

Both the write cycle and the read cycle have device specification violations. In the write cycle, the addresses change prior to $\overline{CS}$ and $\overline{WE}$ becoming inactive; that new address location may be written into. In the read cycle, the address change is correct but $\overline{WE}$ is still active and the fast $\overline{CS}$ begins too soon, performing a nonexistent write cycle. Clearly, controlling the width of $\overline{WE}$ will solve the problems.

Figure 36B shows the proper operation controlled with timing.

Finally, the data output buffers, controlled by timing signals are enabled only during a read cycle while the board is selected preventing bus contention with two or more boards in the system. More importantly, timing disables the output prior to the start of the next cycle, allowing input data to be stabilized on the bidirectional data bus in preparation for a write cycle.

TIMING GENERATION

Having discussed the philosophy of timing and control, we can now focus on the specifics of address latching, write pulse generation and output-enable timing. To perform these functions timing can be generated from one of three sources: clock and shift register, monostable multivibrator, or delay line.

CLOCKED SHIFT REGISTER

A clocked shift register circuit is shown in Figure 37 consisting of a D-type flip-flop and an 8-bit shift register.

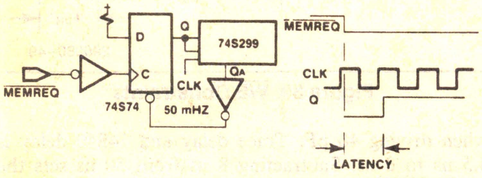


Figure 37. Flip-Flop and Shift Register

On the leading edge of $\overline{MEMREQ}$, the Q output of the D flip-flop is clocked to a one state, enabling a "one" to be propagated through the shift register. The one is clocked into the first stage of the shift register on the first clock edge after the A and B inputs are "ones." After the clock, the output Q_A goes true which subsequently clears the D flip-flop, clocking zeroes into the register to create a pulse one clock period wide.

The accuracy and repeatability depends primarily on the accuracy and stability of the clock. Crystal clocks can be built with +0.005% tolerance and less than 1% variation due to temperature.

An inherent difficulty is the synchronization of Memory Request and the clock. At times there will be a latency of one clock cycle between Memory Request and the actual start of the cycle when Memory Request becomes active just after the clock edge. Assuming an 80 ns cycle and 20 ns clock, the latency can be 20 ns or 25% of a cycle stretching both access and cycle accordingly. A second difficulty of this circuit is caused by the asynchronous nature of the clock and the Memory Request. The request becomes active just prior to the clock and the set-up time of the latch is violated, the output Q_A "hangs" in a quasi-digital state and could double or produce an invalid pulse width; this and the latency hinder effective use in high speed design.

MONOSTABLE MULTIVIBRATOR

The second possible timing generator is a series of monostable multivibrators, using a device such as the AMD Am 26S02 multivibrator. It has a maximum delay from input to output of 20 ns and an approximate minimum of 6 ns. However, with a delay of 20 ns, the monostable multivibrator offers no advantage over the clocked generator. Having a minimum pulse width of 28 ns, the one-shot offers no improvement over the 50 MHz clock, but in fact the performance is worse because it is more temperature and voltage sensitive. The pulse width is dependent on the RC network composed of resistors and capacitors that are temperature sensitive. Consequently, repeatability leaves something to be desired.

DELAY LINE

The third and best choice is a delay line. This design uses STTLDM-406 delay lines from EC^2 with tapped outputs at 5 ns increments. In operation, Memory Request activates an R-S flip-flop fabricated from cross-coupled NAND gates. The output of this circuit starts the memory cycle. Consequently, the cycle starts 5 ns after Memory Request compared to 20 ns for the other two timing generators. The leading edge travels down the delay lines. When the edge reaches the 25 ns tap, the output is inverted and fed back to the R input of the R-S flip-flop, shaping the pulse to width to 25 ns. Twenty-five nanoseconds was chosen to match as close as possible the write pulse width. A 25 ns pulse limits the Memory Request signal width to less than 25 ns to insure proper operation. Otherwise, the R-S flip-flop will not clear until Memory Request returns to a one level. As the pulse travels down the delay lines, it acquires additional skew of ± 1 ns per delay line package for a total of 6 ns overall. Figure 38 shows several timing pulses and the uncertainty of each edge calculated by worst case timing analysis. The remaining problem is selection of timing edges to operate the device. Now that the timing chain is completely defined, specific details of the address latch, write pulse and output enable can be completed.

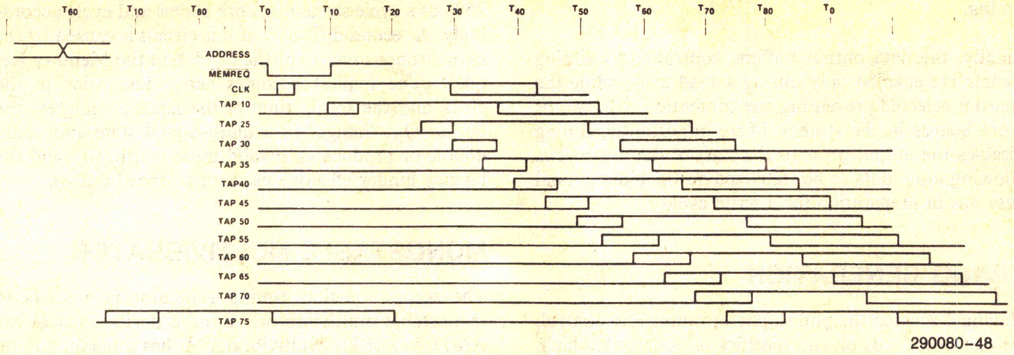


Figure 38. Timing Chain

ADDRESS LATCH TIMING

An R-S flip-flop activated by MEMREQ latches the addresses. A second signal which we will now calculate is used to open the latch. This signal has two boundaries. If the latch opens too late, the access of the cycle will be extended; if it opens too soon, the current cycle will be aborted. Skew through the R-S flip-flop is 1.75 ns to 5.5 ns and skew in the latch from enable to output is 4 ns to 12 ns for a total skew of 6 ns to 17.5 ns. With this skew added to the 30 ns address set-up time, the latch opening signal must be valid at 36 ns best case or 47.5 ns worst case prior to the start of the memory cycle. Each cycle is 80 ns long, therefore, the latch opening signal must begin 44 ns or 32.5 ns, respectively, in the preceding cycle. From the delay line timing diagram, T35 will satisfy the worst case requirements for opening the latch and T25 best case. In production, each board is tuned by selecting T25, T30, or T35 to open the latch, guaranteeing it opens between 35 ns and 30 ns prior to the start of the cycle.

WRITE PULSE TIMING

The next timing to be calculated is the write pulse. Figure 39 shows the three parameters which define the write pulse timing: data set-up time, write pulse width and write recovery time. Data set-up is assured by having data valid through the entire cycle.

Placement of $\overline{\text{WE}}$ in the cycle is controlled by address change to comply with t_{WR}. From previous calculations the earliest addresses can change is 50 ns, which defines the end of the $\overline{\text{WE}}$ signal. Our calculations begin at the device and work back to the timing edge. Eight devices constitute a 40 pF load and a 74S40 is specified for a 50 pF load, reducing delay by 0.5 ns when driving 40 pF. Trace delay and 74S40 delay is 3.5 ns to 8 ns. Subtracting 8 ns from 50 ns sets the termination of the write timing edge at 42 ns. Using the inversion of T25 will end the write pulse at 43 ns with 7 ns to spare.

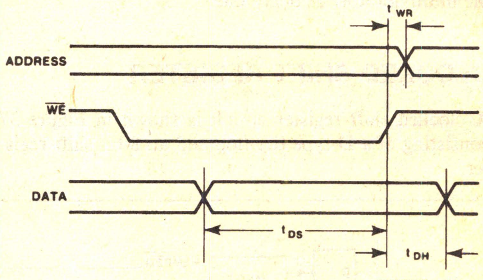


Figure 39. $\overline{\text{WE}}$ Constraints

Data set-up time is guaranteed because data is valid 6 ns (the worst case delay through the latch) after the start of $\overline{\text{MEMREQ}}$.

OUTPUT ENABLE TIMING

There is a 5.5 ns delay through the address driver providing minimum device cycle of 50 ns. As a result the earliest data can disappear from the bus is at 54 ns because of delay through the output circuit. To select the timing tap for the output enable, the skew of the enable circuit is subtracted from the system access time.

Subtracting the 28 ns skew of the buffer enable circuit from the 44 ns access time of the system shows that the latest the timing edge can occur is 16 ns, which is satisfied by edge T10. The trailing edge, however, ends at 37 ns and with minimum propagation delays the bus would become three-stated at 44 ns, coincident with data becoming valid. ORing T20 with T10 will guarantee the output is valid until 54 ns, minimum. Selecting a timing gap between T35 and T50, depending on the propagation delay in the enable circuit, disables the output at 70 ns, allowing input data to be valid for 10 ns prior to start of cycle. The complete schematic is shown in Figure 40.

SUMMARY

The 2147H is an easy-to-use, high speed RAM. The problems in a memory system design are the result of inherent limitations in interfacing. Largest of these is skew, which the designer must strive to minimize. In this example, skew consumed 45 ns of an 80 ns cycle while device access time was extended by only 10 ns, resulting in an 80% efficiency.

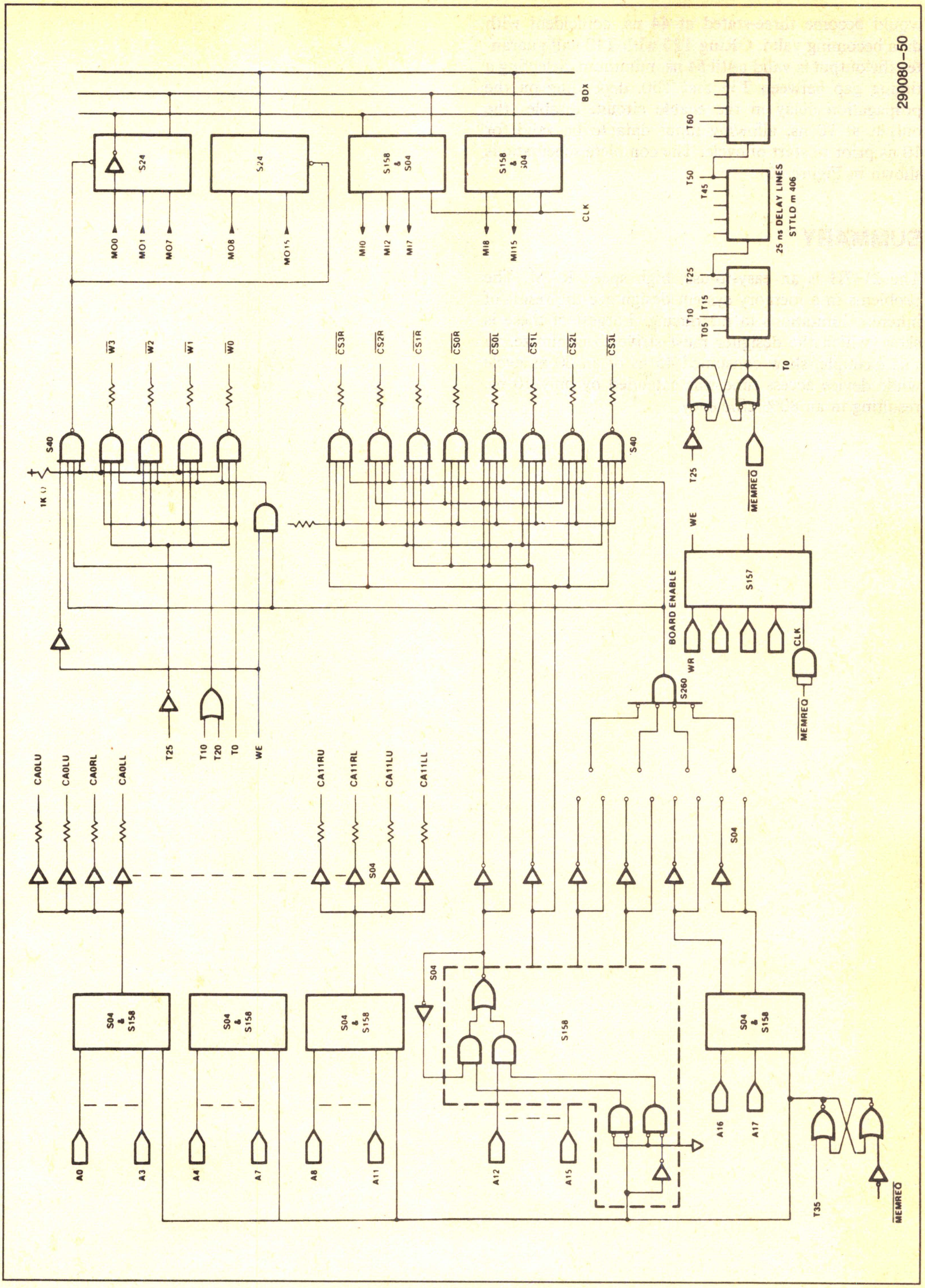

290080-50
BDX
S24
S24
S158 & S04
S158 & S04
CLK
MO0
MO1
MO7
MO8
MO15
MI0
MI2
MI7
MI8
MI15
T60
T50
T45
25 ns DELAY LINES
STTLD m 406
T25
T05
T10
T15
T0
W3
W2
W1
W0
CS3R
CS2R
CS1R
CS0R
CS0L
CS1L
CS2L
CS3L
S40
S40
1K Ω
T25
MEMREQ
WE
S157
BOARD ENABLE
WR
S260
CLK
MEMREQ
T25
T10
T20
T0
WE
CA0LU
CA0LU
CA0RL
CA0LL
CA11RU
CA11RL
CA11LU
CA11LL
S04
S04
S04
S04 & S158
S04 & S158
S04 & S158
S158
S04 & S158
A0
A3
A4
A7
A8
A11
A12
A15
A16
A17
T35
MEMREQ

Figure 40. 16K x 16-Bit High Speed Static Memory

intel®

APPLICATION
NOTE

AP-238

March 1985

Memory Design For The Low Power Microsystem Environment

DENNIS KNUDSON
MEMORY COMPONENTS

© Intel Corporation, 1985

Order Number: 280103-001

1.0 INTRODUCTION

1.1 The Low Power Environment

The low power environment, as discussed in this document, refers to microsystems that have low power as a major feature of the design. The purpose here is to provide some guidelines for designing such systems—particularly the memory subsystems. The topics covered include descriptions and trade-offs of various types of memory components, system design examples and discussions of batteries and power switching circuitry.

1.2 Elements

Generally, the low power environment has two basic elements: active and standby power. With respect to memories, another element—the data retention power—is equally important. As discussed in this document, active power is simply the power required during an access to memory. Standby power is that required while the memory is between accesses. Data retention power is the minimum power required to maintain data in the memory.

1.3 Applications

Low power applications in general are divided into those using AC line power and those using batteries either as primary power or as backup power for memory maintenance and/or memory protection. Active or primary power for systems is fairly simple and can be provided by either the AC line or batteries. Back-up power subsystems consists of circuitry supported by batteries only during the absence of regular power. It includes the system memory, batteries and power switching circuits. When in the backup power mode, the batteries provide power to the memory and the support circuits necessary to maintain the stored information. When power fails, the power switching circuits must shut down all of the system except the memory and its support circuits. In so doing, they must provide a clean, glitch-free and orderly transition from line power to battery power. When line power returns, they must transfer control from the battery powered circuits back to line powered circuits, again in an orderly, glitch-free manner.

In the backup power applications, only those components required to maintain volatile memory data when power is removed, or those required to protect the data when power fails need to be low power devices. Some examples are systems requiring fast, non-volatile storage (RAMs) or power failure protection for on-line memory. They include, but are not limited to battery powered systems. For example, when used for storage such as solid state disks, CHMOS DRAMs allow the user to operate directly out of mass memory but they require battery backup to maintain the data whenever the system is powered down.

In battery powered systems or subsystems, all components are battery supported and as such must consume little power. Such systems must be able to run on each set of batteries for an acceptable period defined by the application. When using re-chargeable batteries, the system should run on each charge for the longest likely continuous use in the specific application and recharge time should be acceptable for the probable frequency of use. Obviously, the more power drawn by the components of the system, the bigger the battery required or the shorter the operating time. Above all, a battery powered system design should avoid components or sub-systems that will require special cooling accommodations (i.e. fans).

1.4 Design Considerations

When designing low power memory systems with standard TTL drivers, standby power can be as little as two percent of the active power. To achieve the low standby power possible with CMOS memories, pull-up resistors must be used on all critical control lines and the TTL must be powered down. This requires special considerations. A more effective method is to use CMOS logic.

Newer CMOS products are ideal for these types of applications because they provide the speed required when the system is operating, and dissipate very little heat in the process when compared to NMOS products. When in backup or data retention mode, they require about two tenths of one percent of their active power to maintain information. CMOS drivers for the memory system reduce standby power to its lowest level—lower, typically by a factor of 40, than TTL standby power consumption. The implications to the system designer are lower cooling requirements and smaller power supplies of batteries(1).

2.0 MEMORY OPTIONS FOR LOW POWER OR NON-VOLATILE STORAGE

In this section we will look at various types of memory suitable for low power applications. Typically, memories used in this type of system are CMOS RAMs for their low power and high speed features. Bubble memories are useful here for mass storage if the application requires long term storage without power. For relatively short term storage, power consumption for the bubble can be reduced by power switching(2). E^2PROMs and CMOS EPROMs, also non-volatile, can be used for small, permanent or semi-permanent software storage such as firmware and operating system kernels.

NVRAMs would be useful for buffer storage on a communications data link or in small, fast local memory requiring data retention without power. In 1972, Signetics introduced the 25120 write only memory (WOM) but no lasting applications have developed so it will not be covered here.

2.1 Magnetic Bubble Memory

The bubble memory is a rugged, non-volatile, serial-in/serial-out storage medium. Both the one megabit (7110) and the four megabit (7114) operate at 50 KHz. Briefly, the MBM operates by rotating an external magnetic field to propel a cylindrical magnetic domain (bubble) through a film or magnetic material. Externally, it handles data in a serial fashion similar to magnetic disc or drum storage systems but, without the noise or moving parts, it is faster, more reliable and uses much less power.

Magnetic bubble memory is smaller than any other memory storage system and cost/bit is second only to the dynamic RAM. It is the slowest and has the highest operating and standby power requirements of all solid state memories but it can retain data indefinitely when power is removed.

A complete bubble memory kit consists of the bubble memory, controller, current pulse generator, formatter, coil pre-driver and drive transistors. The kit requires two voltages and dissipates about 1.5 watts in standby and 3.5 watts active per bubble component. Rugged and truly non-volatile, it has many applications including robotics, oil exploration, aircraft navigation and test equipment.

2.2 EPROMs

Non-volatile read-only-memories, EPROMS are erased under ultraviolet light and then re-programmed electrically. They are programmed by injecting "hot" electrons (typically created by a 12.5 volt Vpp) into the floating (isolated) gate of the transistor. Capacitively coupled to the select gate of the transistor, this charge adds to the select gate charge, altering the threshold voltage of the transistor. They are erased by ultraviolet light which induces enough energy into the floating gate to cause the excess electrons to overcome the energy barrier between the floating gate and the insulator surrounding it. Thus, the electrons are dissipated into the select gate and substrate of the transistor.

EPROMs must be removed from the circuit to be erased and re-programmed. In addition, they must first be completely erased before they can be re-programmed. Typical erasure times are 15 to 20 minutes. Program time is typically 5 minutes (27256 with Int$_e$ligent^{TM} programming) and access times of less than 250 nS are available. Through they do not have the flexibility of reading and writing data in real time, they are close to the dynamic RAM in density and they do not lose data when power is removed.

Some typical applications of EPROMs are firmware, operating system kernels, computer boot programs, communications, portable instruments, office equipment and commercial appliances. CHMOS EPROMs are faster and, with 25% of the active and 0.4% of the standby current of their NMOS counterparts, are well suited for storing initialization programs in low power systems.

2.3 E^{2}PROMs

Electrically erasable (E^2) PROMs use the same "floating gate" technology as EPROMs. The difference is that the charge is added or removed via a tunnel oxide in a phenomenon known as Fowler-Nordheim tunneling. At an energy level referred to as the "forbidden" band, the electrons are able to penetrate the oxide without ever reaching the energy level that standard mechanics would predict as being necessary to overcome the barrier[3]. This allows them to be erased and programmed IN-CIRCUIT and it permits individual byte programmability.

Active power is equivalent to that of static RAM but standby power is much higher, second only to magnetic bubble memory. It has the highest cost/bit and lowest density of the solid state memories except for Non-Volatile RAMs. Non-volatile and in-circuit reprogrammable, it is versatile in control functions and in data acquistion and communication systems requiring frequent system reconfiguration.

2.4 NVRAMs

Each cell of the Non-Volatile RAM consists of two memory cells, one static RAM and the other E^{2}PROM. Consequently, it is the least dense of all solid state memories. It functions as a static RAM during operation but provides non-volatile storage of data when powered off. A signal from the power supply indicating that power is being removed (or lost) causes the NVRAM to move the data from the SRAM cell into the E^{2}PROM cell. Thus, data that can be operated on at microprocessor speeds is automatically saved in non-volatile memory, combining the flexibility of SRAM with the long-term, power free storage of E^{2}PROM. Power and cost/bit are roughly equivalent to E^{2}PROMs.

2.5 SRAMs

Static Random Access Memories latch data into either four transistor (4T, for cost) or six transistor (6T, for low power) memory cells. Consequently, they do not need to be refreshed and access time is, essentially, cycle time. These features have historically contributed to the speed advantage of SRAMs over other memory types as well as to simple interface design. However, they also contribute to the density and power disadvantages of the SRAM. As data are gated out by addresses, they do not require clocks but may use one of two signals to control system interface. A chip enable $(\overline{CE})$ may be used to provide a standby mode with reduced power and an output enable $(\overline{OE})$ may be provided to release the data bus.

SRAMs are always one density generation behind dynamic RAMs because of the number of transistors per cell. The new CMOS SRAMs actually enjoy a power advantage over NMOS dynamic RAMs but the advantage is lost once again to dynamic RAMs on the CMOS process. Like dynamic RAMs, SRAMs are volatile memory, losing data when power is lost.

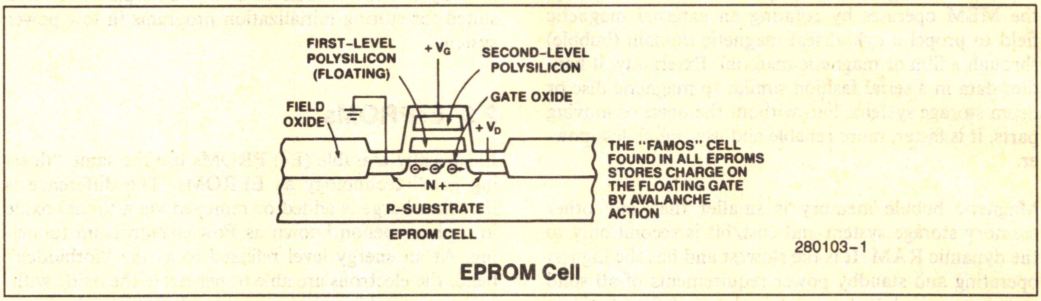

FIRST-LEVEL POLYSILICON (FLOATING)
+VG
SECOND-LEVEL POLYSILICON
GATE OXIDE
FIELD OXIDE
+VD
N+
P-SUBSTRATE
EPROM CELL
THE "FAMOS" CELL FOUND IN ALL EPROMS STORES CHARGE ON THE FLOATING GATE BY AVALANCHE ACTION
280103-1
EPROM Cell

Figure 1. EPROM Cell

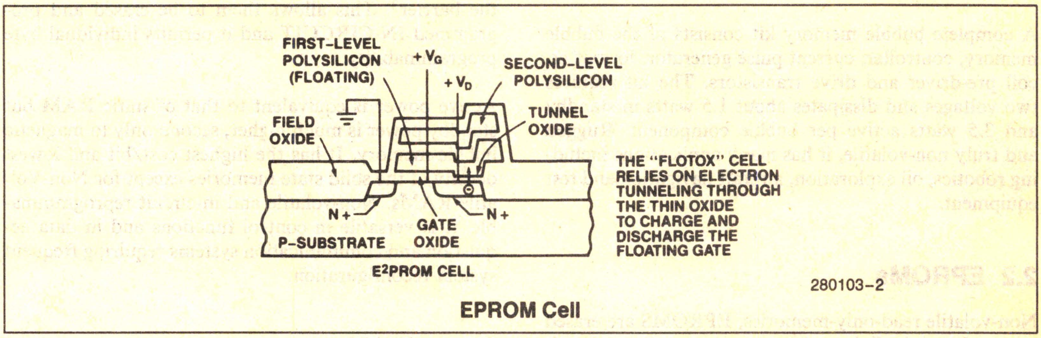

FIRST-LEVEL POLYSILICON (FLOATING)
+VG
+VD
SECOND-LEVEL POLYSILICON
TUNNEL OXIDE
FIELD OXIDE
N+
N+
GATE OXIDE
P-SUBSTRATE
E2PROM CELL
THE "FLOTOX" CELL RELIES ON ELECTRON TUNNELING THROUGH THE THIN OXIDE TO CHARGE AND DISCHARGE THE FLOATING GATE
280103-2
EPROM Cell

Figure 2. E^{2}PROM Cell

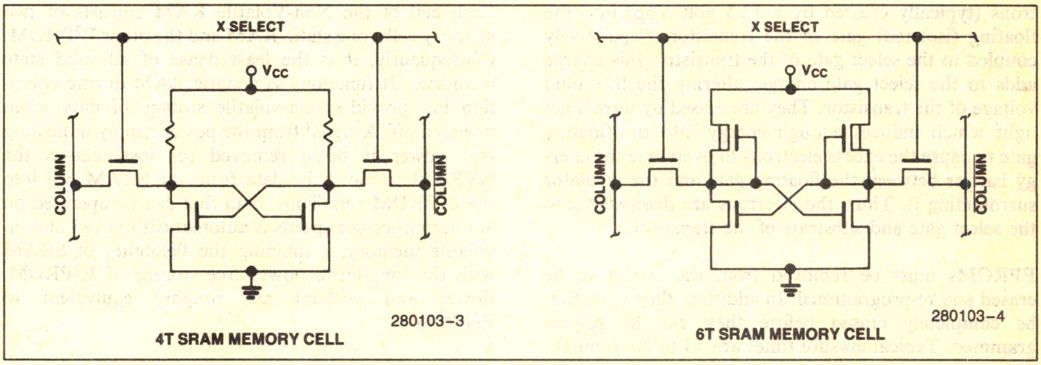
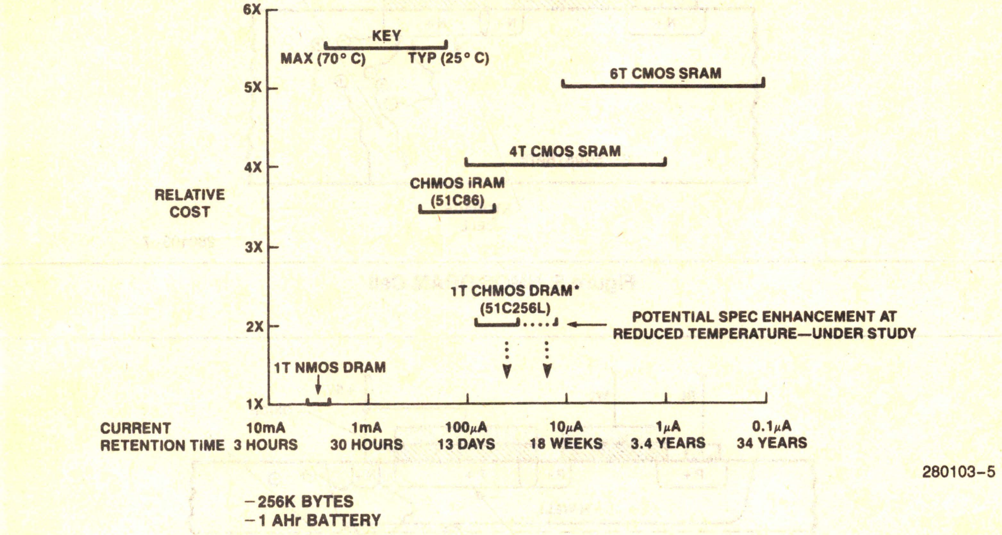

X SELECT
VCC
COLUMN
COLUMN
280103-3
4T SRAM MEMORY CELL
X SELECT
VCC
COLUMN
COLUMN
280103-4
6T SRAM MEMORY CELL

Figure 3. SRAM 4T and 6T Cells

MEMORY COST vs DATA RETENTION CURRENT/TIME (64K BIT EQUIVALENT)



NOTE:
*Includes controller and assumes extended refresh. See bibliography, Item 4

Chart 1

Some typical applications of SRAMs are in cache memories, bit slice processors, local microprocessor memory (less than 64K), video graphics and (with CMOS SRAMs) battery backup and battery powered systems.

2.6 iRAMs

The integrated RAM works like an SRAM but costs less. It is a dynamic RAM with an on-chip refresh circuitry and it is generally available in two versions, synchronously or asynchronously refreshing. The synchronous version has an on-chip refresh address generator and a "Refresh" input that allows the user to control the refresh occurrence.

The asynchronous version has a timer, refresh address generator, access arbiter and a "Ready" output. When a refresh request occurs coincident with an access request the arbiter resolves which will take precedence. Whenever an access request is held up by refresh, "Ready" goes low, causing the processor to insert WAIT states. With these features, the iRAM provides SRAM characteristics at lower cost per bit and lower power requirements (within like technologies). The iRAM is a volatile memory, particularly well suited to microcontroller memory (up to 64K bytes) and local memory (up to 128K bytes) for microprocessors.

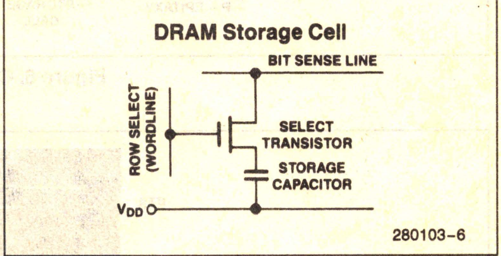
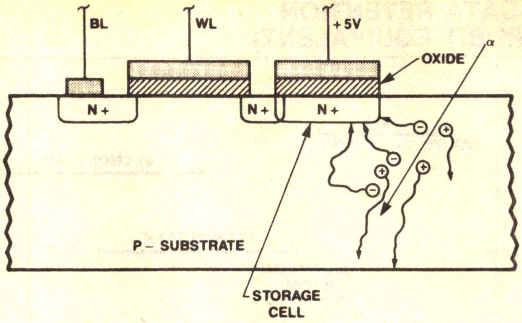


Figure 4. DRAM Storage Cell

2.7 DRAMs

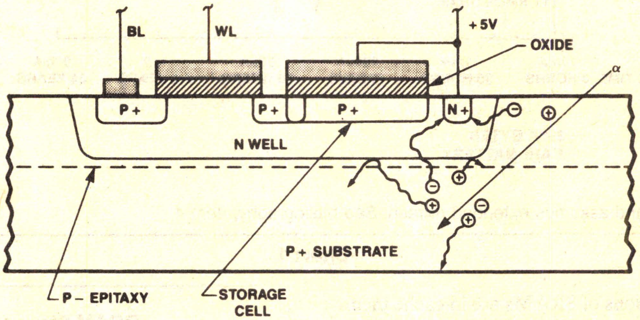
The Dynamic RAM stores data on a capacitor in a single transistor cell. This allows the highest density and lowest power per bit of all random access memories, but, because of charge leakage from the storage capacitor, they have to be refreshed periodically. DRAMs are volatile memory and, as such, lose data whenever power is removed or lost.

The primary DRAM application has been, historically, large main memories (greater than 64K) for mainframe, mini and personal computers. The introduction of CHMOS DRAMs has further reduced the power requirements(4) and added new high bandwidth fea-


BL
WL
+5V
OXIDE
α
N+
N+
N+
P− SUBSTRATE
STORAGE CELL

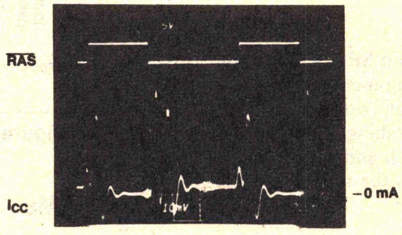
280103-7

Figure 5. NMOS DRAM Cell


BL
WL
+5V
OXIDE
α
P+
P+
P+
N+
N WELL
P+ SUBSTRATE
P− EPITAXY
STORAGE CELL

280103-8

Figure 6. CMOS DRAM Cell



280103-9

51C259L CURRENT
20 mA/DIVISION
I_{CC} DURING $\overline{\text{RAS}}$ LOW TIME BETWEEN
T_{RAC} AND T_{RP} IS 5 mA

Figure 7. 51C259 Current

tures such as Ripplemode^{TM} and Static Column Decode(5). The features of CHMOS allow DRAMs to move into non-volatile solid state disks (which will permit the user to execute directly from mass storage), battery powered (portable) computers, battery back-up systems and traditionsl SRAM speed applications such as video graphics(6).

DRAMs on the CHMOS process reduce the standby current by about a factor of forty. The data retention power requirement of the DRAM is further reduced by the extended refresh feature. When operating in the data retention mode, refresh can be extended to 32 ms for the 51C256L, 64 ms for the 51C64L.

Because a small capacitor is the storage mechanism for DRAMs, they have been susceptible to "soft errors". When an alpha particle strikes the die, it generates ions which collect at the capacitor, changing the stored charge(7). The cell is not damaged but the information it contains can be changed (Figure 5). If it is, a "soft" error has occurred. The CMOS process has changed this by allowing the storage capacitor to be placed in an "n" well which absorbs the ions generated by the stray particle(8) (Figure 6). Consequently, 64K CHMOS DRAMs, at a 1μS cycle rate, have soft error rates of 10 fits*. At the 256K level, the soft error rate will be less than 400 fits, and typically 40 fits. Furthermore, since the soft error rate is directly related to cycle rate , during the low power data retention mode (i.e. 32 ms refresh) the soft error rate goes to:

1 μs = 40 fits, then for the 256K devices the extended refresh soft error rate is:

32 ms/256 refresh rows = 125 μs

1 μs/125 μs −40 fits = **0.32 fits** per device

*failures in time = number of failures in 10(9) device hours (or 114 years).

3.0 SYSTEM DESIGN USING CHMOS DRAMs

3.1 Active Low Power Design Description

CHMOS DRAMs permit the building of larger and lower powered systems than have previously been possible. As an illustration, a low power, general purpose microcomputer system design will be discussed using all CMOS products. An 80C88 operating in max mode has 256K bytes of DRAM (expandable to 960 Kb) with a DMA controller to handle refresh during normal operation. A standby mode of operation is provided to reduce the power usage during periods of no activity. During standby the memory refresh is extended to 32 ms which reduces the data retention power.

To minimize the transient effects of current, it is recommended that a 0.1 μF bypass capacitor be provided for each memory device. High speed (low inductance) capacitors are preferred. Most CMOS devices require less than 0.1 μF. The actual decoupling capacitance required can be calculated for specific devices using the formula:

$$C_{BYPASS} = di^{*}dt/dV$$

where; di = change in current

dt = spike duration or 1 μs*, whichever is faster

dV = allowable voltage droop

For example, Figure 7 shows the current requirement for the 51C259. The peak current is 95.63mA so the decoupling requirement is:

$$C = 96\text{ mA} \times 40\text{ ns}/100\text{ mV} = 0.04\ \mu F$$

In this case 0.1 μF for every other device would be sufficient.

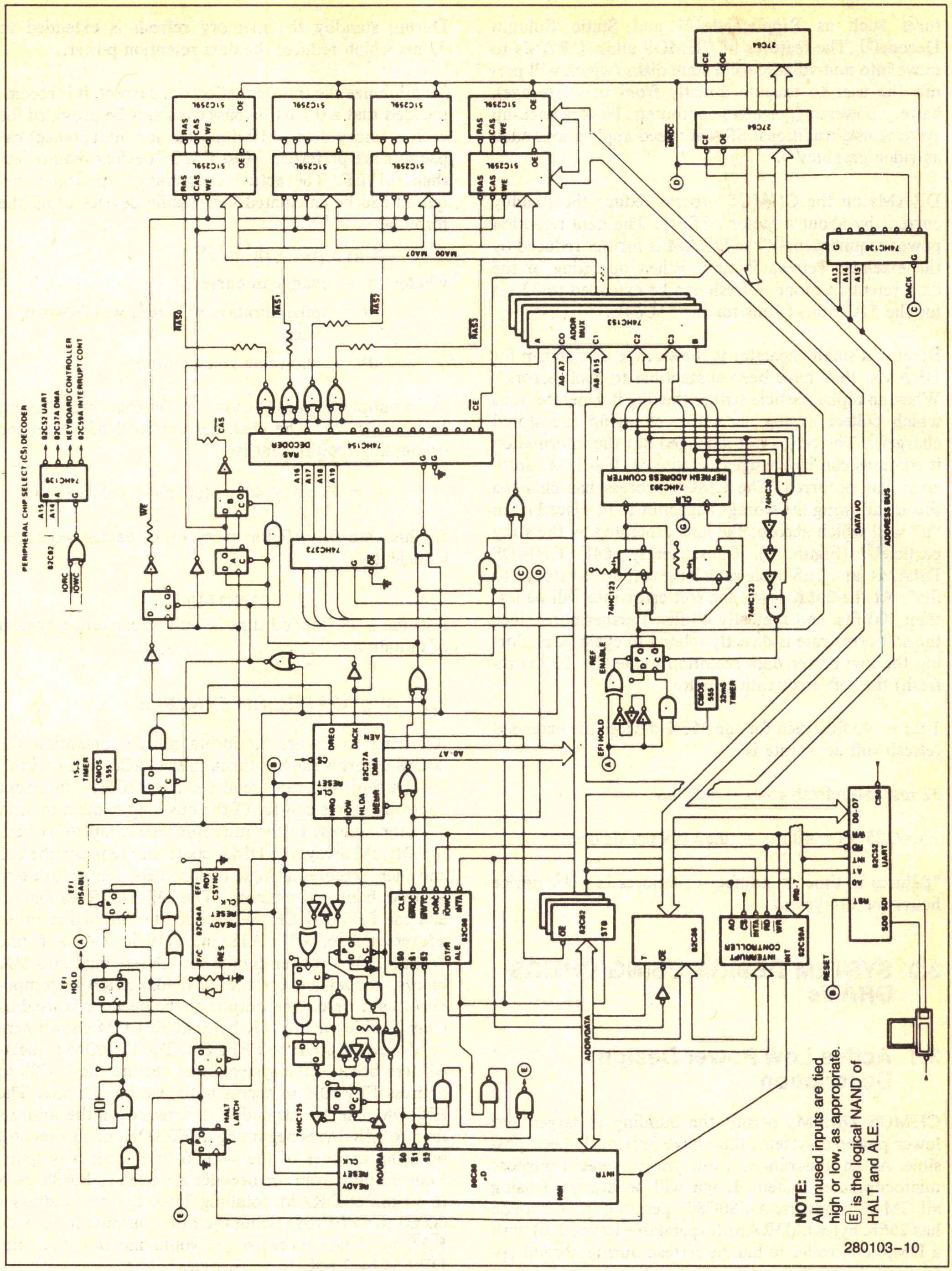
***NOTE:**

Assume 1 μs respond time of bulk capacitance, typical of tantalum.

3.1.1 SYSTEM DESIGN EXAMPLE

Referring to Figure 8, during normal ooeration the 80C88 controls the bus through the 82C88 bus controller. During interrupt requests the 82C59A interrupt controller takes control of the bus long enough to send a vector address to the microprocessor, and to refresh the DRAM array, the DMA controller requests the bus and then executes a single (distributed) refresh cycle to all four banks of memory. The DRAM $\overline{RAS}$ signals and the EPROM $\overline{CE}$ are decoded by the higher order addresses A16, A17, A18 and A19 in a 4-to-16 line decoder. The decoder divides the address field into 64K blocks, convenient for the particular DRAM components used here. One output of the decoder is used as Chip Enable for the 16K bytes of EPROM shown here at address FC000H to FFFFFH. The EPROM is located here because the system reset vectors the 80C88 to address FFFF0H to access initialization routines. The EPROM can be expanded downward in the address field to 64K bytes beginning at F0000H, or further still by using another of the 4-to-16 line decoder outputs. Four outputs from the decoder are used as $\overline{RAS}$'s each to a bank of DRAM, totalling 256K bytes at addresses 00000 to 3FFFFH. Using the other outputs to provide $\overline{RAS}$ to eleven more banks would increase the total DRAM by 704K, to 960K bytes.

The reset initialization routines are located in EPROM and, for this system, will include programming routines


51C259L
27C64
74HC138
74HC153 ADDR MUX
74HC154 RAS DECODER
74HC373
74HC393 REFRESH ADDRESS COUNTER
74HC30
74HC123
CMOS 555 32mS TIMER
REF ENABLE
EFI HOLD
82C37A DMA
82C84A
82C88
80C88
82C82
82C86
82C59A INTERRUPT CONTROLLER
82C52 UART
74HC125
HALT LATCH
CMOS 555 15.5 TIMER
EFI DISABLE
PERIPHERAL CHIP SELECT (CS) DECODER
74HC139
82C52 UART
82C37A DMA
KEYBOARD CONTROLLER
82C59A INTERRUPT CONT
MA00 MA07
RAS0
RAS1
RAS2
RAS3
A0-A7
A8-A15
DATA I/O
ADDRESS BUS
ADDR/DATA
RESET

NOTE:
All unused inputs are tied high or low, as appropriate.
Ⓔ is the logical NAND of HALT and ALE.

280103-10

Figure 8. Low Power System Design

for the DMA controller, the interrupt controller and the UART. Following initialization, the DMA will begin its distributed refresh routine and the operating system software can be loaded through one of the I/O ports.

Write enable ($\overline{\text{WE}}$) to the DRAM is generated by the memory write command ($\overline{\text{MWTC}}$) from the 82C88 bus controller and the system clock. Column address strobe ($\overline{\text{CAS}}$) is generated by $\overline{\text{MWTC}}$ or $\overline{\text{MRDC}}$ (memory read command) and the system clock. The rising edge of the clock sets the latch (A) which switches the address multiplexer from the row address to the column address. The falling edge of the clock then sets the second latch (B) which sends $\overline{\text{CAS}}$ to the memory. During the DMA refresh cycles, the acknowledge signal (DACK) holds CAS and $\overline{\text{WE}}$ high and clears the DMA request (DRQ). Note that the $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ latches are buffered to the array. This is done because reflections from the line stubbing of the memory array back into the outputs of the latches could cause the latches to toggle, glitching the signals. Also, series terminators (~33Ω) are shown in the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and address lines. These terminators improve the impedance match of the driver to the line, reducing reflections. For best results, they should be located electrically less than one inch from the driver output.

3.1.2 MEMORY

The 51C259L devices used here are low power 256k bit memory devices organized as 64K x 4. This organization helps keep active power low by enabling only two devices during a memory access. If 256K×1 devices were used, all eight would be turned on, drawing about four times the current.

The EPROMs shown are CHMOS 8K x 8's, containing a boot loader and programming instructions for the DMA, the interrupt controller and the UART. The EPROM capacity could be increased to 64K bytes using the rest of the outputs of the 74HC138 decoder.

In max mode, the 80C88 provides two common I/O request/grant ($\overline{\text{RQ}}/\overline{\text{GRA}}$) lines to co-processors for bus access, one of which is used here for the DMA (Figure 9). This pin requires a low-active pulse in to request the bus, then sends a low-active pulse out to release (grant) the bus. The processor then waits for another low-active pulse in to indicate that the co-processor is through with the bus. The DMA has separate Hold Request (HRQ) and Hold Acknowledge (HLDA) pins which use active-high levels. Consequently, it is necessary to convert both the high-going and low-going edges of HRQ to low-active pulses. In the period between these pulses, the $\overline{\text{RQ}}/\overline{\text{GRA}}$ pin must be released for the 80C88 output "Grant" pulse. The Grant pulse presets a latch for the DMA Hold Acknowledge and returns the $\overline{\text{RQ}}/\overline{\text{GRA}}$ pin to the input circuit to wait for the end-of-hold pulse.

3.1.3 STANDBY MODE

One nice feature of the CMOS process is that the system can be put into a very low power standby mode by bringing the system clock to a complete stop. To do this, the external frequency in (EFI) on the 82C84A is used and the EFI clock is stopped, in this case, by a HALT instruction from the 80C88 (Figure 10). The HALT instruction first stops the EFI clock without any glitches and it then stops the oscillator itself, both at a high level. The timing through the 82C84A at this frequency stops the clock output low. Any interrupt (such as a key pressed) will cause the system to exit the standby mode and return to normal operation. The interrupt clears the halt latch which allows the oscillator to begin again. Because the oscillator was stopped at a high level, it will begin by transitioning low. Then, on the high transition, it will clock the EFI hold latch thus clearing it. The following low transition will get through the first stage OR gate. When the burst refresh initiated by clearing the EFI hold latch (see below) is completed, the oscillator will clock the EFI disable latch low and then the oscillator will be enabled through to the EFI input of the 82C84A. The burst

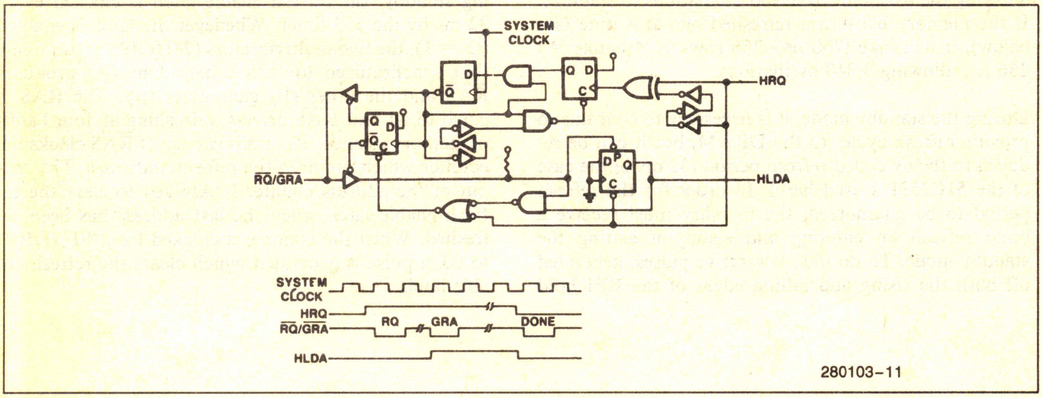
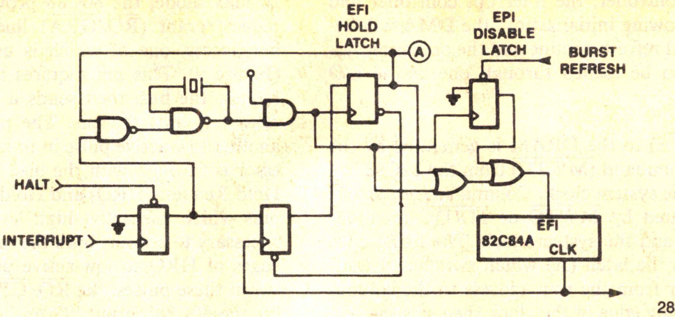

SYSTEM CLOCK
HRQ
$\overline{\text{RQ}}/\overline{\text{GRA}}$
HLDA
SYSTEM CLOCK
HRQ
$\overline{\text{RQ}}/\overline{\text{GRA}}$
RQ
GRA
DONE
HLDA
280103-11

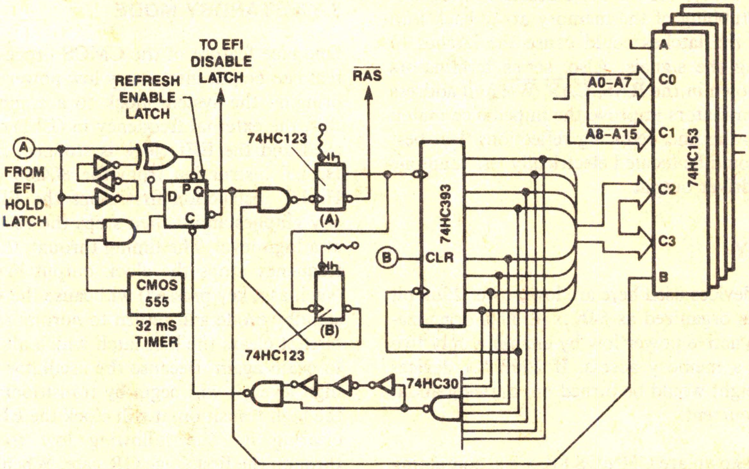
Figure 9. Bus Request Circuit


EFI HOLD LATCH
Ⓐ
EPI DISABLE LATCH
BURST REFRESH
HALT
INTERRUPT
82C84A
EFI
CLK

280103-12

Ⓐ Goes to the Refresh Enable Latch

Figure 10. Clock Circuit


Ⓐ
FROM EFI HOLD LATCH
REFRESH ENABLE LATCH
TO EFI DISABLE LATCH
D
P
Q
C
CMOS 555
32 mS TIMER
74HC123
(A)
RAS
74HC123
(B)
Ⓑ
CLR
74HC393
74HC30
A
A0–A7
C0
A8–A15
C1
C2
C3
B
74HC153

280103-13

Figure 11. Refresh Circuit

refresh will take about (250 ns × 256 rows =) 64 μs, allowing the oscillator over 900 oscillations to stabilize. If the memory banks are refreshed one at a time (see below), it will take (250 ns × 256 rows × 4 banks =) 256 μs, allowing 3,840 oscillations.

During the standby mode, it is necessary to continue to provide refresh cycles to the DRAM, but it can be reduced to the extended refresh period (32 ms in the case of the 51C259L's used here). In order for the refresh period to be guaranteed, the memory must receive a burst refresh on entering and again on exiting the standby mode. To do this, low-active pulses, generated off both the rising and falling edges of the EFI hold latch, preset the refresh enable latch (Figure 11). During standby, the refresh enable latch is clocked every 32 ms by the 555 timer. Whenever the latch is enabled (Q = 1), the two multivibrators (74HC123's) run freely (but synchronized to each other). One (A) produces $\overline{\text{RAS}}$ and the other (B) guarantees t_{RP}. The RAS is gated to all four $\overline{\text{RAS}}$ drivers, refreshing all four banks of memory at once. The trailing edge of $\overline{\text{RAS}}$ clocks the counter which provides the refresh addresses. The output of the address counter is ANDed to clear the refresh enable latch when the last address has been refreshed. When the counter is clocked from FF (HEX) to 00, a pulse is generated which clears the refresh enable latch.

While refreshing all four banks at once, as is shown here, does not use any more average power, refreshing one row at a time would reduce the peak power requirement during standby by a factor of four (see Figure 14 and the Data Retention design for power calculations, later in this section).

When exiting the standby mode, it is necessary to keep the 80C88 and the DMA off the bus until the last burst refresh has been completed. To do this, (Figure 10) the refresh enable latch presets the EFI disable latch in the clock hold circuitry, blocking the oscillator from the EFI input of the 82C84A and holding the system clock off. At the same time, it disables the DREQ input to the DMA and, for additional security, holds $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ off. When the burst refresh is complete, the oscillator clears the EFI disable latch, releasing the oscillator to the 82C84A.

3.1.4 POWER ANALYSIS

The system shown (Figure 8) contains ten VLSI devices(9), ten memory devices, thirty logic devices and two timers. To calculate the power consumption, some assumptions are made:

- where not given, typical values are 40% of the maximum value (rule of thumb)
- some values are estimates as final data sheets are not yet available.
- typical values are used as they should average out over a system.
- during normal operation, the memory receives a 15 μs distributed refresh
- The 80C88 can access the memory at 5 MHz/4 = 1.25 MHz max.(one bus cycle takes four T-states)
- The DRAM memory is capable of operating at (1/245 ns =) 4.082 MHz.
- System duty cycle is 2% (most of the system time is spent waiting for instructions such as keyboard entries)
- The speed/power curve is approximately linear

74HC logic current requirement (@25°C):
536 μA (logic) +144 μA (timers) = 0.68 mA

Eight 51C259L-15 DRAMs, 100% (4.082 MHz) duty cycle, I_{CC} (typ):

- operating = 45 mA each
- standby = 0.01 mA each (CMOS drivers)

Two 27C64 CMOS EPROM, I_{CC} (typ):

- operating = 20 mA × 0.4 = 8 mA each
- standby = 100 μA × 0.4 = 0.04 mA each

During constant DRAM memory accesses, memory activity is:

active: 1.25 MHz/4.082 MHz = 30.6%
refresh: 245 ns/15 μs = 1.7%
standby: 100% − (30.6 + 1.7) = 67.7%

Memory Current is:

active: [2(45 mA) + 6(0.01 mA)] 30.6% = 27.56 mA
refresh: [8(45 mA)] 1.7% = 6.12 mA
standby: [8(0.01 mA)] 67.7% = 0.054 mA
continuous memory access total current = 33.73 mA

At 2% system duty cycle, memory current is:

$(I_{oper} \times 2\%) + I_{ref} + [I_{stby} \times (100\% - (2 + 1.7)\%)] =$
$(27.56\text{ mA} \times 2\%) + 6.12\text{ mA} + [8(0.01\text{ mA})]\ 96.3\% =$
6.597 mA

EPROM Current is:

continuous active	16.0 mA
continuous standby	0.08 mA

Table 1 shows the typical current required for the VLSI:

Table 1

Device	Active	Standby
80C88	20.0 mA	0.2 mA
82C84A	6.0 mA	6.0 mA
82C37A	0.4 mA	0.004 mA
82C88	2.0 mA	0.004 mA
82C82 (3 each)	1.5 mA	0.012 mA
82C86	0.5 mA	0.004 mA
82C59A	0.4 mA	0.004 mA
82C52	1.0 mA (est)	0.004 mA
TOTAL	**31.8 mA**	**6.232 mA**

Rounding the DMA duty cycle up to 2% (from 1.7%) for simplicity, the current requirement for the VLSI at a 2% duty cycle is:

(31.8 mA × 2%) + (6.232 mA) × 98%) = 6.743 mA

Therefore, total current for the system during normal operation at the 2% duty cycle (DRAM accesses only) is:

logic + DRAM + EPROM + VLSI
0.68 mA + 6.597 mA + 0.08 mA + 6.743 mA = **14.1 mA**

During a RESET operation, for a period of less than 1 ms, current will be:

DRAM stby + refresh + EPROM + logic +
[8(0.01 mA)]98.3% + 6.12 mA + 16 mA + 0.68 mA +

μP + clk + DMA + bus + addr +
20 mA + 6 mA + 0.0107 mA + 2.0 mA + 1.5 mA

data + int + UART =
+0.5 mA + 0.004 mA + 0.004 mA = **52.9 mA**

Power Supply

Using the formula: $C = di*dt/dV$;

$$(52.9\text{ mA} - 14.1\text{ mA})1\text{ ms}/200\text{ mV} = 194\ \mu\text{F}$$

200 μF of storage capacitance will support V_{CC} during reset to no more than 200 mV of droop. This means the power supply need only be sized for normal operation. Normal operation should not exceed 70% of the power supply capacity (ye olde rule of thumb) so:

$$0.7\ I_{ps} = 14.1\text{ mA}$$
$$I_{ps} = 20.14\text{ mA}$$

a 20 mA supply would suffice and, incidentally, would reduce the maximum droop voltage during reset to:

$$(52.9\text{ mA} - 20\text{ mA})1\text{ ms}/200\ \mu\text{F} = 164.5\text{ mV}$$

3.2 Data Retention Design

A system with data retention can, but need not necessarily be a low power design. The main prerequisite is that that portion of the system to be supported by the battery in the absence of line power must be low power. The elements to be discussed here include:

- saving information in use by the processor
- ensuring refresh for the DRAM
- protecting the memory from false signals:
  a. during back-up
  b. at power up
- minimizing power dissipation during back-up

3.2.1 SAVING INFORMATION

When power fails, the processor will "lose its place", or forget the operations it was actively executing. To prevent this, one can, when the power sense signal occurs, interrupt the processor using the non-maskable interrupt. The NMI would send the processor to a routine causing it to store, in a fixed area of memory, the pointers, stack counter and program counter and then to set a flag. The area of memory used can be anywhere, but it should either be dedicated to this task or it should be a rarely used section such as the bottom of the stack. When power returns, following system initialization, the processor checks the flag and, if set retrieves the saved information and continues from where it was interrupted.

3.2.2 SYSTEM DESIGN EXAMPLE

For the sake of simplicity, we will use the low power design already discussed, modifying it for battery backup. In Figure 12, power fail circuitry is ORed with the EFI hold signal into the data retention refresh circuitry. A binary counter enabled by 'power sense' counts $\overline{\text{RAS}}$ pulses to the memory, allowing, in this case, fifteen memory accesses (including refresh) to store pointers, etc., and set a flag. It then starts the backup refresh circuitry. The maximum time before starting data retention refreshing would occur when all accesses counted are normal refresh cycles:

$$15\ \mu\text{s} \times 15\text{ cycles} = 225\ \mu\text{s}$$

This period is easily supported by the capacity of the power supply and V_{DD} grid, but it does limit the number of memory accesses and the time in which to do

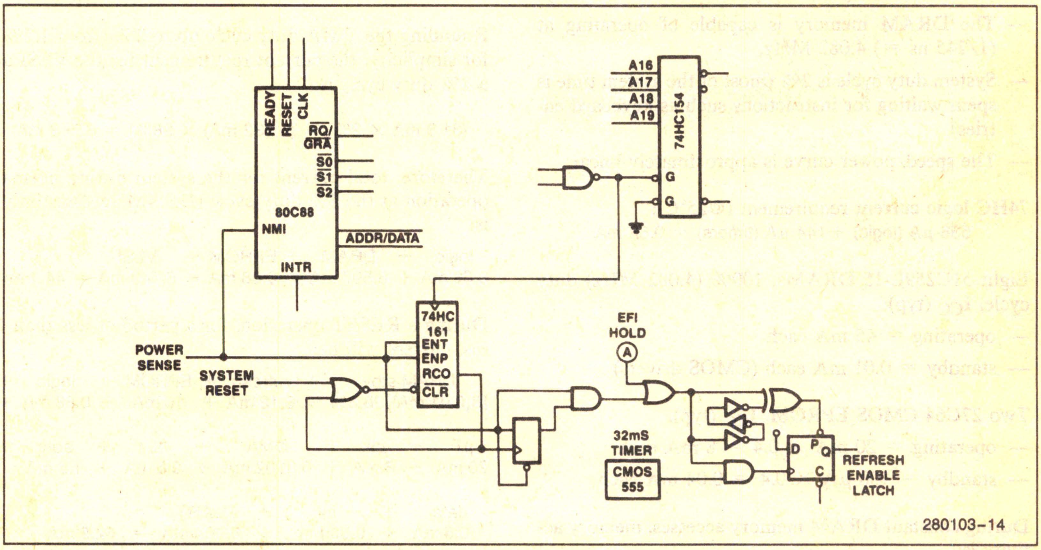


Figure 12. Provisions for Battery Back-up

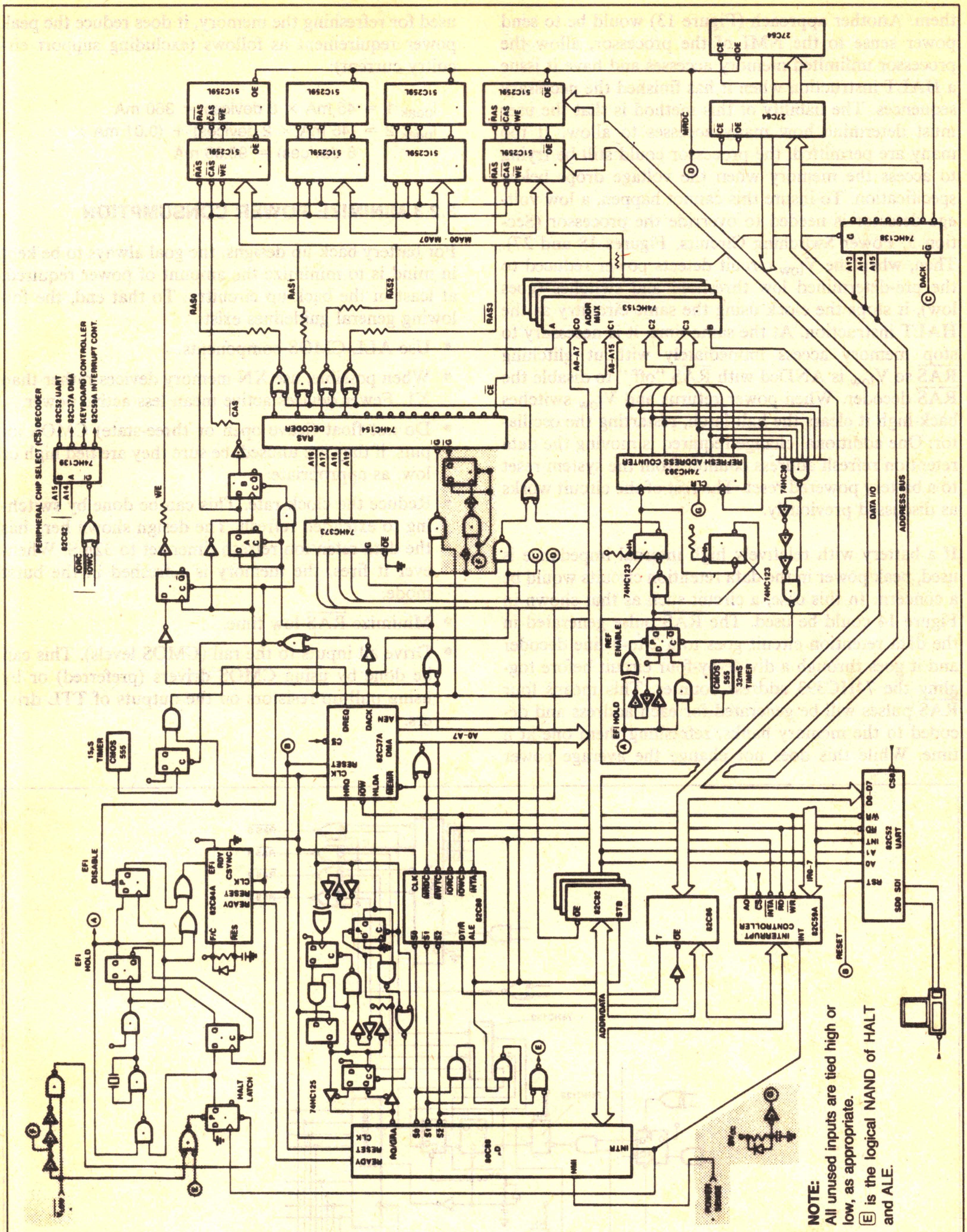

NOTE:
All unused inputs are tied high or low, as appropriate.
E is the logical NAND of HALT and ALE.
280103-15
51C256L
27C64
74HC138
74HC153
ADDR MUX
74HC154 RAS DECODER
74HC393 REFRESH ADDRESS COUNTER
74HC373
74HC123
CMOS 555 32mS TIMER
CMOS 555 15μS TIMER
82C37A DMA
82C84A
82C88
82C82
82C86
82C59A INTERRUPT CONTROLLER
82C52 UART
80C88
HALT LATCH
EFI DISABLE
EFI HOLD
REF ENABLE
74HC125
MA00 - MA07
RAS0
RAS1
RAS2
RAS3
CAS
WE
A0-A7
A8-A15
ADDR/DATA
DATA I/O
ADDRESS BUS
PERIPHERAL CHIP SELECT (CS) DECODER
82C52 UART
82C37A DMA
KEYBOARD CONTROLLER
82C59A INTERRUPT CONT.
RESET

Figure 13. Battery Back-up Design

them. Another approach (Figure 13) would be to send power sense to the NMI of the processor, allow the processor unlimited memory accesses and have it issue a HALT instruction when it has finished the necessary sequences. The liability of this method is that the user must determine how many accesses to allow. If too many are permitted, the processor could still be trying to access the memory when the voltage drops below specification. To insure this cannot happen, a low voltage detector is needed to override the processor (Section 5, Power Switching Circuits, Figures 18 and 27). Then, when the V_{low} circuit detects power reduced to the pre-determined low threshold and switches (goes low), it stops the clock using the same circuitry as the HALT instruction. At the same time, it is necessary to stop memory access immediately without glitching $\overline{RAS}$ so V_{low} is ANDed with $\overline{RAS}$ "off" to disable the $\overline{RAS}$ decoder. When power returns and V_{low} switches back high it clears the halt latch, restarting the oscillator. One additional change required is moving the data retention refresh address counter from the system reset to a battery powered reset. The rest of the circuit works as discussed previously.

If a battery with relatively high internal impedance is used, peak power in the data retention circuits would be a concern. In this case, a circuit such as that shown in Figure 14 could be used. The $\overline{RAS}$ pulse generated in the data retention circuit goes to a 2-to-4 line decoder and it goes through a divide-by-four circuit before toggling the 74HC393 address counter. This means four $\overline{RAS}$ pulses will be generated for each address and decoded to the memory banks, refreshing them one at a time. While this does not change the average power used for refreshing the memory, it does reduce the peak power requirement as follows (excluding support circuitry current):

I_{peak} 1 = 45 mA × 8 devices = 360 mA
I_{peak} 2 = (45 mA × 2 devices) + (0.01 mA × 6 devices) = 90.06 mA

3.2.3 MINIMIZE POWER CONSUMPTION

For battery back-up designs, the goal always to be kept in mind is to minimize the amount of power required, at least in the back-up circuitry. To that end, the following general guidelines exist:

- Use ALL CMOS components.
- When possible, use XN memory devices rather than X1. Fewer devices active mean less active power.
- Do not float (leave open or three-state) CMOS inputs. if they are unused, be sure they are tied high or low, as appropriate.
- Reduce the clock rate. This can be done by switching to extended refresh. The design shown here has the data retention refresh timer set to 32mS. Whenever it fires, the memory is refreshed in the burst mode.
- Minimize $\overline{RAS}$ low time.
- Drive all inputs to the rail (CMOS levels). This can be done by using CMOS drivers (preferred) or by using pull-up resistors on the outputs of TTL drivers.

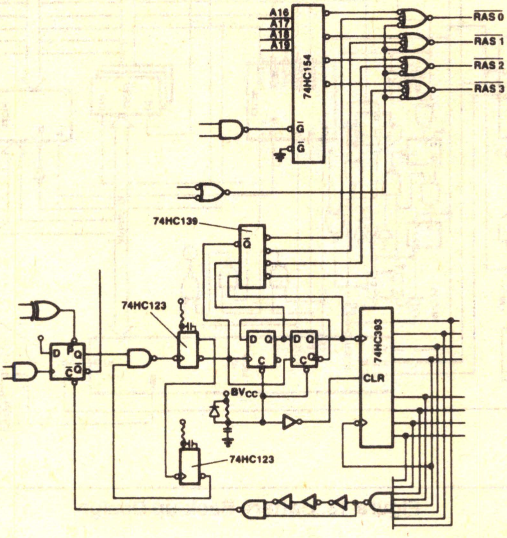


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Figure 14. Distributed Refresh Reduces Peak Current

- Minimize the number of pull-up resistors by using CMOS drivers wherever possible.
- Ensure bypass capacitors have low inductance paths across the device (Figure 15).
- Use good design practices. Reduce the load capacitances by keeping related sections physically close.

Control input transitions. When too slow (≥25 ns), excess current will flow. When too fast (<5 ns), the increased frequency increases the current requirement. When possible, distribute the power used over time to control peak currents. Figure 14 alternates the refresh to each bank of memory, reducing the peak power requirement.

(For more design guidelines, see #10 in the bibliography)

3.2.4 POWER ANALYSIS

For this example, the power requirements of just the battery back-up section will be analyzed. As shown in Figure 13, those elements identified by an asterisk (*) would be powered by the battery in data retention mode. To determine battery size, typical values may be used, but the application, particularly the ambient temperature should also be considered. The lesser values will be used here.

The current requirements are:

Memory (/dev.):	Logic (total,TYP.)
typical operating = 45 mA	464 μA
maximum operating = 65 mA	
typical standby = 0.01 mA	
maximum standby = 0.1 mA	

When supported by the battery, the memory is refreshed every 32 ms. Refresh cycle time is 250 ns and each device has 256 rows to be refreshed (the cycle time can be extended a little to provide margin for component tolerances but extend t_{RP} because as $\overline{\text{RAS}}$ low time is extended, power increases). Total current required will be determined by the amount of time spent in each of refresh and standby.

256 rows × 250 ns = 64 μs to refresh
64 μs/32 ms × 100 = 0.2%
8(45 mA) × 0.002 = 720 μA (active)
8(0.01 mA) × 0.998 = 79.84 μA (standby)
720 μA + 79.84 μA = 799.8 μA (averaged over refresh period)

Therefore, the total average current drawn by the battery back-up section of this design, at 25°C, is:

799.8 μA + 464 μA = 1.264 mA

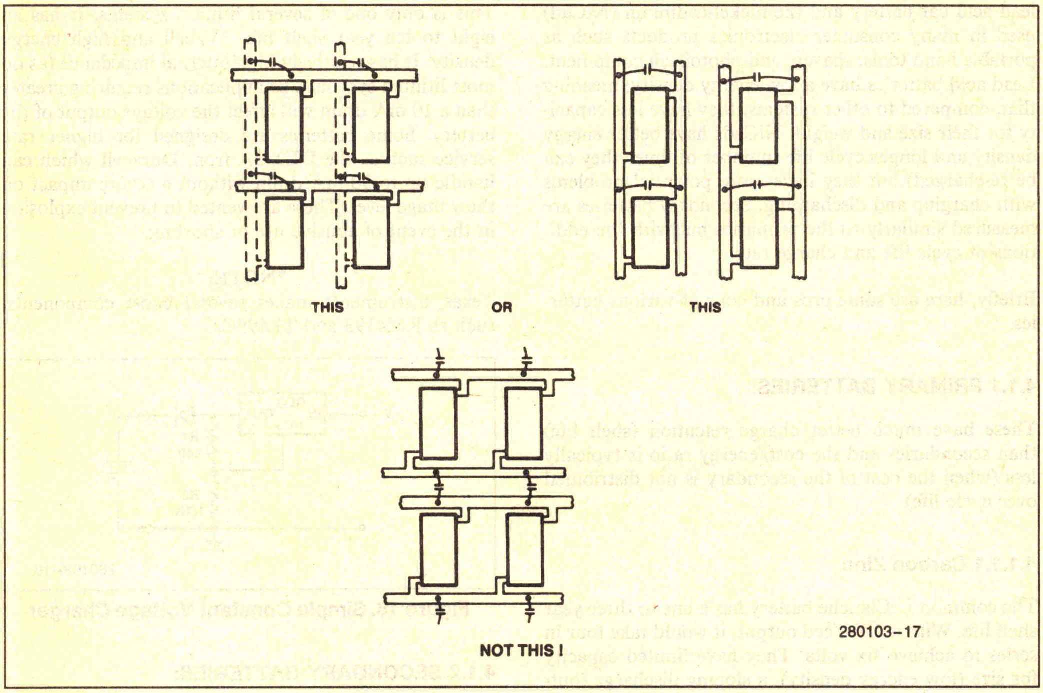


Figure 15. Effective Capacitive Decoupling

With this information, a reasonable choice of battery type can be made (see Section 4, Batteries).

4.0 BATTERIES

4.1 Battery Types

Batteries are divided into two basic types, primary and secondary. Primary batteries cannot, reasonably, be recharged. Secondary batteries are those that can be recharged. (For a comprehensive reference on batteries, see #12 in the bibliography.)

Primary batteries are created around a chemical reaction that, for all practical purposes, cannot be reversed. Consequently, when their charge is depleted they must be replaced. Some common examples are the zinc chloride, silver oxide and lithium batteries. They come in various sizes and most are in one of two styles, cylindrical or coin shaped. There are many electrochemical systems under the primary heading, each varying from the others in some unit of measure such as voltage, energy, energy density or cost. These variations can make them more or less suited for various applications (see chart 2)^{11}.

Secondary batteries use a reversible chemical reaction. Some common examples of secondary batteries are the lead acid car battery and the nickel-cadmium (NiCad) used in many consumer electronics products such as portable hand tools, shavers and photoflash equipment. Lead acid batteries have a low energy density, meaning that, compared to other systems, they have less capacity for their size and weight. NiCads have better energy density and longer cycle life (number of times they can be re-charged) but they have more potential problems with charging and discharging. Secondary batteries are measured similarly to the primaries but with the additions of cycle life and charge rate.

Briefly, here are some pros and cons of various batteries.

4.1.1 PRIMARY BATTERIES:

These have much better charge retention (shelf life) than secondaries and the cost/energy ratio is typically less (when the cost of the secondary is not distributed over cycle life).

4.1.1.1 Carbon Zinc

The common LeClanche battery has a one to three year shelf life. With a 1.5V/cell output, it would take four in series to achieve six volts. They have limited capacity for size (low energy density), a sloping discharge (output voltage decreases continuously over the period of the discharge), low cost and excellent availability in a wide variety of package sizes and capacities.

4.1.1.2 Alkaline Manganese

Similar to the carbon zinc, the alkaline battery has a two to five year shelf life, 1.5V/cell, limited capacity for size and a sloping discharge. It has higher energy density but higher cost than LeClanche and it is widely available in a variety of sizes and capacities.

4.1.1.3 Silver Oxide

This battery has a two to five year shelf life. It has a high energy density but, with 1.5V/cell, it would require four in series of a boost circuit* to achieve six volts. It has a flat discharge curve, relatively high cost and limited package configurations.

4.1.1.4 Mercuric Oxide

Similar to the silver oxide, the mercuric oxide battery has only 1.35V/cell. It has a flat discharge curve, higher cost and a potential ecological problem with the disposal of spent cells.

4.1.1.5 Lithium Manganese

This is only one of several lithium systems. It has an eight to ten year shelf life, 3V/cell and high energy density. It has relatively high internal impedance (as do most lithium systems), so applications requiring greater than a 10 mA drain will affect the voltage output of the battery. Some batteries are designed for higher rate service such as the DL2/3A from Duracell which can handle up to 50 mA drain without a severe impact on the voltage level. These are vented to prevent explosion in the event of abusive use or shorting.

*NOTE:

Texas Instruments makes several boost components, such as RM4193 and TL499C.

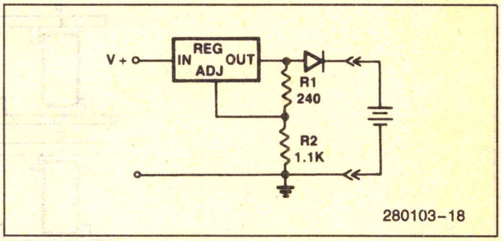


Figure 16. Simple Constant Voltage Charger

4.1.2 SECONDARY BATTERIES:

Because of self-discharge, these batteries have a relatively short shelf life but, with some means of charge

Chart 2. Eight Principal Battery Systems and Average Characteristics

Usual Name*	**Carbon Zinc***	**Zinc Chloride Super Heavy Duty***	**Alkaline-Manganese Dioxide (MnO_2)**	**Mercuric Oxide***
Electrochemical System	Zinc-Manganese Dioxide (often called Leclanche)	Zinc-Manganese Dioxide	Zinc-Alkaline Manganese Dioxide	Zinc-Mercuric Oxide
Voltage Per Cell	1.5	1.5	1.5	1.35
Negative Electrode	Zinc	Zinc	Zinc	Zinc
Positive Electrode	Manganese Dioxide	Manganese Dioxide	Manganese Dioxide	Mercuric Oxide
Electrolyte	Aqueous solution of ammonium chloride and zinc chloride	Aqueous solution of zinc chloride (may contain some ammonium chloride)	Aqueous solution of potassium hydroxide	Aqueous solution of potassium hydroxide or sodium hydroxide
Type	Primary	Primary	Primary	Primary
Rechargeability	Not Recommended	Not Recommended	Not Recommended	Not Recommended
Number of Cycles				
Input if Rechargeable				
Overall Equations of Reaction	$2MnO_2 + NH_4Cl + Zn \rightarrow ZnCl_2 + 2NH_3 + H_2O + Mn_2O_3$	$8MnO_2 + 4Zn + ZnCl_2 + 9H_2O \rightarrow 8MnOOH + ZnCl_2 \bullet 4ZnO \bullet 5H_2O$	$2Zn + 2KOH + 3MnO_2 \rightarrow 2ZnO + 2KOH + Mn_3O_4$	$Zn + HgO + KOH \rightarrow ZnO + Hg + KOH$
Typical Commercial Service Capacities	60 mAh to 30 Ah	Several hundred mAh to 18 Ah	30 mAh to 45 Ah	45 mAh to 14 Ah
Energy Density (Commercial) Watt-hour/Lb	20	40	20–45	50
Energy Density (Commercial) Watt-hour/Cubic Inch	2	3	2–5	8
Practical Current Drain Rates Pulse	Yes	Yes	Yes	Yes
Practical Current Drain Rates High (More Than 50 mA)	100 mA/square inch of zinc area ("D" cell)	150 mA/square inch of zinc area ("D" cell)	200 mA/square inch of separator area ("D" cell)	No
Practical Current Drain Rates Low (Less Than 50 mA)	Yes	Yes	Yes	Yes
Discharge Curve (Shape)	Sloping	Sloping	Sloping	Flat
Temperature Range: Storage	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 140°F (−40°C to 60°C)
Temperature Range: Operating	20°F to 130°F (−6°C to 54.4°C)	0°F to 130°F (−17.8°C to 54.4°C	−20°F to 130°F (−28.9°C to 54.4°C)	14°F to 130°F (−10°C to 54.4°C)
Effect of Temperature on Service Capacity	Poor low temperature	Good low temperature relative to carbon-zinc	Good low temperature	Good high temperature, low temperature depends upon construction
Impedance	Mode	Low	Very low	Low
Leakage	Low???Under Abusive conditions	Low	Rare	Some salting
Gassing	Medium	Higher than carbon-zinc	Low	Very low
Reliability (Lack of Duds: 95% Confidence Level)	99% at 2 years	99% at 2 years	99% at 2 years	99% at 2 years
Shock resistance	Fair to Good	Good	Good	Good
Cost Initial	Low	Low to Medium	Medium Plus	High
Cost Operating	Low	Low to Medium	Medium to high at high power requirements	High

***NOTE:**
Portions of this chart reprinted here courtesy of Union Carbide Corp. Eveready.

Chart 2. Eight Principal Battery Systems and Average Characteristics (Continued)

Usual Name*	**Silver Oxide***	**Nickel-Cadmium***	**Lithium**	**Lead Acid**
Electrochemical System	Zinc-Silver Oxide	Nickel-Cadmium	Lithium-Manganese Dioxide	Lead
Voltage Per Cell	1.5 (monovalent)	1.2	3	2
Negative Electrode	Zinc	Cadmium	Lithium	Lead
Positive Electrode	Monovalent Silver Oxide	Nickelic Hydroxide	Manganese Dioxide	Lead Dioxide
Electrolyte	Aqueous solution of potassium hydroxide or sodium hydroxide	Aqueous solution of potassium hydroxide	Non-aqueous mix propylene carbonate dimethoxy ethane	Sulfuric Acid
Type	Primary	Secondary	Primary	Secondary
Rechargeability	Not Recommended	Yes	Not Recommended	Yes
Number of Cycles		300 to 1,000		
Input if Rechargeable		Minimum of 140% of energy withdrawn		160% of energy withdrawn
Overall Equations of Reaction	$Zn + Ag_2O + KOH \rightarrow$ $ZnO + 2Ag + KOH$	$Cd + 2NiOOH + KOH + 2H_2O \rightleftarrows$ $Cd(OH)_2 + 2Ni(OH)_2 + KOH$	$2Li + 2MnO_2 \rightarrow$ $Li_2O + Mn_2O_3$	$PbO_2 + Pb + 2H_2SO_4$ $\rightleftarrows 2PbSO_4 + 2H_2O$
Typical Commercial Service Capacities	15 mAh to 210 mAh	150 mAh to 4 Ah	35 mAh to 1100 mAh	1.5 Ah to 400 Ah
Energy Density (Commercial) Watt-hour/Lb	50	12–16	100	10–100
Energy Density (Commercial) Watt-hour/Cubic Inch	8	1.2–1.5	6.6	0.8–7
Practical Current Drain Rates Pulse	Yes	Yes	Yes	Yes
Practical Current Drain Rates High (More Than 50 mA)	No	8.10A ≈ 1 amp/sq. in. of electrode	Cylindrical yes coin no	Yes
Practical Current Drain Rates Low (Less Than 50 mA)	Yes	Yes	Yes	Yes
Discharge Curve (Shape)	FLat	Flat	Flat	Sloping
Temperature Range: Storage	−40°F to 140°F (−40°C to 60°C)	−40°F to 140°F (−40°C to 60°C)	−60°C to +75°C	−60°C to 30°C
Temperature Range: Operating	14°F to 130°F (−10°C to 54.4°C)	Discharge: −4°F to 113°F (−20° to 45°C) Charge CH Types: 32°F to 113 °F (0°C to 45°C) Charge CF Type: 60°F to 113°F (15.6°C to 45°C)	−10°C to +70°C	−40°C to 60°C
Effect of Temperature on Service Capacity	Low temperature depends upon construction	Very good at low temperature	Good high temperature Low temperature depends upon construction	Low temperature depends upon construction
Impedance	Low	Very low	Medium	Low
Leakage	Some salting	No	Rare	Low to Medium. Some salting
Gassing	Very low	Low	Low	Medium
Reliability (Lack of Duds: 95% Confidence Level)	99% at 2 years	99% at 2 years		
Shock resistance	Good	Good	Good	Fair to Good
Cost Initial	High	High	High	Medium
Cost Operating	High	Low	High	Very Low

***NOTE:**
Portions of this chart reprinted here courtesy of Union Carbide Corp. Eveready.

maintenance, shelf life can be extended virtually indefinitely. For the most part, they have a better high rate performance than the primaries, an exception being lithium cells using soluble cathode materials which have comparable performance (i.e. lithium/sulfur dioxide, lithium/thionyl chloride). They can generate gasses when charging or discharging at excessively high rates. For brevity, and because they are generally the preferred design for this application, only the sealed versions will be considered here.

4.1.2.1 Lead Acid

With low energy density, these batteries are generally packaged three or six cells in series for six or twelve volts and in larger sizes for much higher capacities (i.e. 400 Amp hours). Fully charged, they contain strong sulfuric acid and shorting the outputs may cause an explosion. They self-discharge, forming lead sulfate ($PbSO_4$) crystals which can insulate the plate, reducing capacity. Lead filaments can form between the plates when charging and can short out cells. Excessive overcharging may cause venting. They can deliver large current surges and they have a sloping discharge curve which eases the task of sensing when the battery is low. They are normally charged with a constant voltage but can be charged with constant current if care is taken to avoid overcharging. They cannot be stored in a discharged state. They have a lower cycle life than NiCads but they cost less and they have no "memory" effect or thermal runaway problems. Charging circuits are discussed in more detail in the next section.

4.1.2.2 Nickel Cadmium

These batteries have low energy density and 1.2V/cell. If used in series, they should have closely matched discharge rates or the faster discharged cell can be driven to cell reversal (destroyed) when the battery is allowed to reach total discharge. NiCads are charged with constant current at a rate of 10% of capacity (0.1C) for 14 to 16 hours (standard cell) or 30% (0.3C) in 3 to 5 hours for quick charge cells. If constant voltage is used, care must be taken to limit the charge current during the final 25% of charging to prevent thermal runaway. If charged at less than a 10% rate, cell capacity will fade and a sustained overcharge will cause a lack of capacity on the first discharge. When partially discharged to the same level several times and then recharged, they develop a "memory" effect and will, thereafter, discharge no further than that level. It is a temporary effect in that forcing a deep discharge will erase the memory. They cost more than lead-acid but are more rugged, typically have a longer cycle life and they have a long shelf life in any state of charge. Normal discharge rate is fairly flat. Charging circuits are discussed in more detail in the next section.

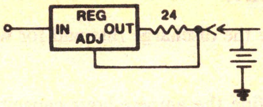


Figure 17. Simple Constant Current Charger

4.1.3 OTHER BATTERY SYSTEMS

This is by no means an exhaustive description of battery systems. Many other primaries and some additional secondaries are available and more are in development. For example, there are a number of primary lithium systems such as lithium/thionyl chloride, lithium/copper oxide, lithium/silver chromate, and so on. A silver oxide secondary is available with the highest energy and power density and best charge retention of any commercially available secondary. Its high cost and low cycle life, however, have held it to limited applications. Many more secondaries are in development, including lithium, nickel, zinc, aluminum, sodium and calcium systems(12). The concern of this document, however, was for those systems available today and was further narrowed for this application by energy density, availability, voltage/cell, cost, and so on. The LeClanche was included in this description primarily as a commonly known system for reference.

4.2 Key Parameters For Battery Selection

In the process of selecting a particular battery, first consider the application in which it will be used. That will usually encompass many of the characteristics that will identify the battery of choice. For example, in what environment (temperature, vibration, etc.) will the battery exist? What voltage is required. And so on. If necessary, applications engineers from the battery manufacturers can help in the selection process, but here are the main parameters to be considered, in no particular order. The application will generally prioritize them.

4.2.1 VOLTAGE:

What is the voltage range within which the application will be operating?

How low a voltage can be tolerated?

This will show either that a sloping discharge curve is acceptable or it may indicate a requirement for a battery with a flat discharge curve.

4.2.2 ENERGY:

What will be the discharge rate and for what period of time?

This will define the ampere-hour capacity required of the battery.

4.2.3 ENERGY DENSITY:

How much space will be available (or perhaps weight tolerable) in the area where the battery is to be located?

It may be possible to use multiple cells in series to achieve, say, six volts, but more than two cells may be two cumbersome. It is worth noting here that re-chargeable batteries require less service than primaries which have to be replaced periodically. So, particularly in stationary systems, they could be located with the system power supply, permitting larger sizes for greater capacity.

4.2.4 ENVIRONMENT:

What are the temperatures, standby and operating, to which the battery will be subjected?

Will it have to withstand vibration?

This will define how rugged the battery must be.

4.2.5 SERVICE LIFE:

How long must the batteries last, of at least, what is an acceptable period?

This will help define the capacity required of the battery. In the case of the re-chargeables, it can also define the cycle life of the battery.

4.2.6 COST:

Of course! What is acceptable?

Higher cost for a flat discharge rate or, perhaps, for higher service?

Higher initial but lower operating (or the reverse) cost?

Depending on the priority of this issue, it may be the deciding factor between a preferred battery and one that is merely acceptable.

Other factors that may be considered include shelf life, duty cycle, safety, reliability and availability.

4.3 Choosing a Battery

Of course, the issues being considered here are low power systems and systems with battery backup. A hypothetical example of each is examined to illustrate the battery selection process.

4.3.1 EXAMPLES

The first application is a low power system. It is portable, so it must be kept both small and light. The voltage will be in the range of six volts to four-and-a-half volts, using not more than two batteries in series that together do not exceed one half inch in height. Peak current drain is 8mA and duty cycle is 1%. A sloping discharge curve will give an early "battery low" indication which will permit continued operation for a reasonable period to allow time for purchase of a replacement. So size, voltage and discharge curve are the first considerations. Within those parameters we will look for greatest capacity and lowest cost. Referring back to the chart of battery comparisons (Chart 2), the carbon zinc and alkaline manganese have limited capacity for size (energy density) and silver oxide and mercuric oxide would require four cells or a boost circuit. The lithium/manganese dioxide has relatively high energy density, sufficient voltage to achieve six volts with just two cells and an acceptable discharge curve. Both initial and operating costs are high but expense is not a high priority (in this example). Current drain is low enough that the internal impedance of the battery should not be a problem. In the re-chargeables, lead-acid has a low energy density (too big and too heavy). The NiCad has slightly better energy density, it will require four cells and a charging circuit, but has low operating cost. Therefore, it will increase the size of the system (small size was a high priority) but keep operating costs down (cost was a low priority).

The battery of choice for this system is the lithium.

The second application is battery backup. A small computer, stationary, has a four megabyte CHMOS DRAM memory (sixty-four 51C259L's) organized as 2M × 16 and serving as both main memory and as mass storage. Using the 64K × 4 51C2259L means that only four devices will be active at a time, keeping both operating and (if banks are refreshed one at a time) refresh currents low. Since the system is not portable and the battery is for backup, it can be located with the primary power supply so size is not as restricted as in the previous example. This will permit a larger, higher capacity battery to be used for the relatively large memory, but it will probably be less accessible. This implies a battery that rarely needs servicing. Since the system normally draws power from the AC line, a recharging circuit can be added to the system quite easily. Therefore, a rechargeable battery will be used, but which one? Size was not an issue so cost can be. Nickel cadmium batteries are more expensive than lead acid and require more care in charging and discharging. So the battery of choice for this system is the lead acid.

Table 2

System	# = 6V	Capacity	Size (inches)	Typical Life Cycle @ 14mA
Alkaline	4 each	1600 mAh	1.97×2.25×0.56	114.3 hours
Silver Oxide	1 each	150 nAh	0.99×0.51×0.51	10.7 hours
Mercuric Oxide	1 each	500 mAh	1.77×0.68×0.68	35.7 hours
Lithium Mang.	1 each	1200 mAh	1.41×1.37×0.76	85.7 hours
Lead Acid	1 each	6000 mAh	3.6×4.5×1.9	428.6 hours
NiCad (quick chg)	5 each	1200 mAh	1.7×4.5×0.9	85.7 hours

4.3.2 BATTERY SELECTION FOR THE LOW POWER SYSTEM

The low power system discussed in Section 3 could be powered by a secondary battery instead of the power supply. It would have to support about 14 mA during normal operation and a random pulsed high rate of 53 mA (I_{reset}). As discussed in Section 3, storage capacitance could help during the high rate, but a battery with some high rate capacity could reduce the size of the capacitance required. What remains is to determine an acceptable tradeoff between life cycle, size and cost. Beginning with primaries, Table 2 has a few randomly selected examples of battery systems to further illustrate the concept.

Either the NiCad or the lead acid would work well in this particular design. The final choice would depend on other requirements of the application such as cycle life (NiCad) or cost (lead acid).

4.3.3 BATTERY SELECTION FOR BATTERY BACK-UP SYSTEM

The battery back-up system discussed in Section 3 required 1.26 mA average drain at 6 Vdc. Most line power failures are very short, so assuming AC powers the memory at all times except failures and the longest failure might be four hours, the minimum battery capacity is:

$$1.26\text{ mA} \times 4 = 5.04\text{ mAh}$$

Referring to Chart 2, it can be seen that any of the battery types can easily support this requirement. Primary batteries in this system will require a battery low indicator (see Section 5, Power Switching Circuits) and regular servicing. Since AC line power is normally used, this is an excellent application for secondary batteries with a recharging circuit. As above, if the system is to be mobile, smaller NiCads might be used. If stationary or if cost is a significant factor, less expensive lead-acid might be preferred.

If the system is used eight hours a day, five days a week and the batteries are required to support the memory whenever normal power is off, the minimum capacity would have to support the weekend, so:

$$1.26\text{ mA} \times 63\text{ hours} = 79.4\text{ mAh}$$

With the addition of off-hours during the week:

$$1.26\text{ mA} \times 64\text{ hours} = 80.6\text{ mAh}$$

$$\text{Total: } 79.4 + 80.6 = 160\text{ mAh per week}$$

Referring above to Table 2, the highest capacity primary would last:

$$1600\text{ mAh}/160\text{ mAh per week} = 10\text{ weeks.}$$

The secondaries would last to the extent of their cycle life, typically from one to four years at five cycles per week.

5.0 POWER SWITCHING CIRCUITS

A battery back-up system required some means to smoothly enter and exit the battery back-up mode of operation. It must, in an orderly fashion, stop the system and switch the volatile memory over to battery power before the line power is lost. It must also return the memory to line power when that power is restored and it must do it without loss of the data stored and with an orderly transfer of the bus back to the now-active system. In addition, it may be necessary to sense when the battery is in a low state of charge and flag the operator. Where appropriate, it must provide battery charging circuits.

Briefly, these are the elements to be covered in this section:

a. Power sensing
b. Switching to back-up power
c. Sensing battery low
d. Recharging

5.1 Power Sensing

The power sensing circuit is connected to the front-end of the power supply. Essentially, it must provide a look-ahead signal to tell the system that the line power is going down. The system can then invoke a predetermined series of operations that take it to back-up power quickly and in an orderly manner. The sensing circuit is powered at all times by the battery.

5.1.1 μWATTS CMOS LOW POWER DETECTOR

The first circuit shown here is a microwatt CMOS low power detector. It provides two outputs. The first tells the system that power is going down early enough that the system has time to store pointers, stack counter and program counter and shift over to battery power. The second output tells the system to stop all activities, power is gone.

5.1.2 DIFFERENTIAL COMPARATOR FOR POWER FAIL DETECTION

The second circuit uses a comparator that relies on the ripple out of the bridge rectifier. When power starts to go down, the ripple becomes more pronounced. As it fluctuates below the trigger level of the circuit, the comparator output goes high, signalling the beginning of a power loss. As the ripple swings high again (momentarily shutting the comparator off), it provides a little more boost to the regulator, keeping power up a little longer. Because of the relatively low frequency of the ripple (60 × 2 = 120 cps), this provides at least (1/120 =) 8 ms of continued power. Time for the system to shut itself down in orderly sequence.

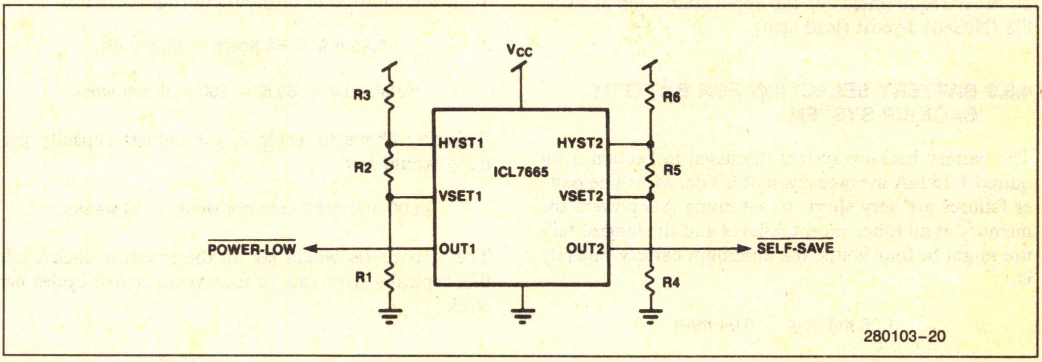


Figure 18. μWatt CMOS Low Power Detector

5.2 Power Switching Circuits

5.2.1 SIMPLE SWITCHING CIRCUIT

The first requirement of a power switching circuit is that the power for the portion of the system what will be supported by the battery when power fails (CMOS) be isolated from the power for the rest of the system (TTL).

This can be done quite simply with a low-leakage diode as shown in the simple diode switching circuit, below. A second diode is installed in the TTL line to keep the normal voltage to both circuits at the same level. V_{CC} must be higher to allow for the diode drop. The lithium battery shown also has a diode to prevent charging of the primary cell. The NiCad has a resistor both to allow charging and to limit the charge current. Battery power to the system will be lower by the voltage drop across the resistor. Relays could be used, but a capacitor would have to support the CMOS circuits during switching and is not recommended.

5.2.2 DUAL VOLTAGE SWITCH

The second switching circuit shown uses transistor isolation. This is a dual voltage circuit, providing normal voltage when the system is operating, and a lower, support voltage on battery power. The voltage drop across the transistor Q2 is small enough (100 to 200mV) that it is unnecessary to match the TTL and CMOS V_{CC} as was done in the diode circuit. During normal operation, Q1 is turned on and the power supply powers the circuit. At the same time, the battery is charged by the base current of Q1. When power goes down, Q2 turns on, Q1 turns off and the battery powers the circuit.

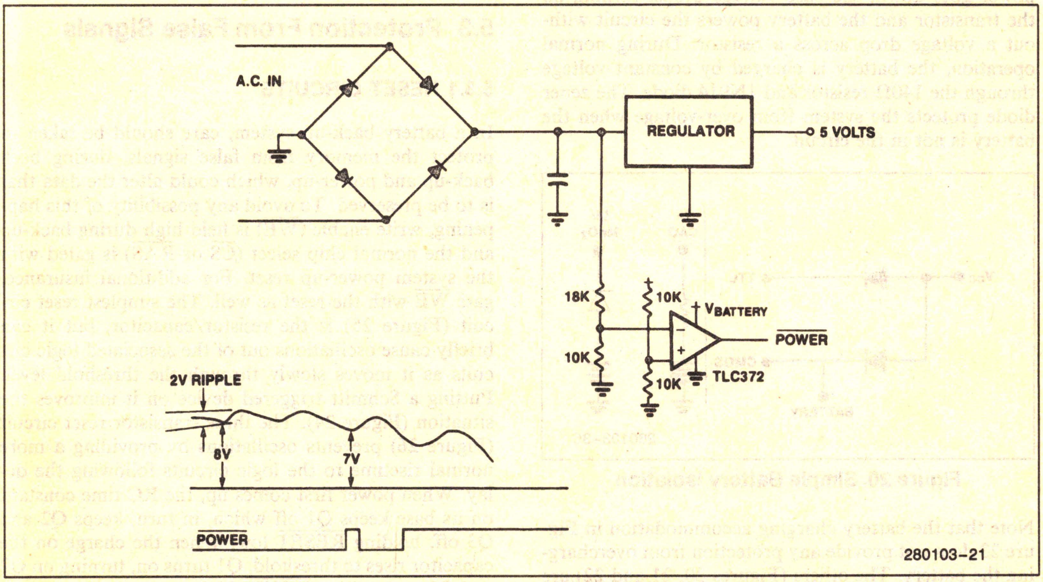


Figure 19. Power Failure Detection

5.2.3 SINGLE-BUS SWITCH

The next switching circuit is a single voltage transistor circuit for a system that has all circuits backed up by the battery. Q2 and its bias network are a regulating circuit that establishes the voltage at which the circuit switches from normal to battery power. As power goes down, that voltage turns off Q2 which, in turn, shuts off Q1 and the battery takes over. The battery is charged by constant voltage, and R_C in the NiCad circuit establishes the maximum charging current for the battery.

5.2.4 DUAL-BUS SWITCH

The last switching circuit uses diode isolation for the two circuits and a transistor switch for the battery. Normally biased off by the unregulated voltage, as power goes down, the base voltage drops, turning on the transistor and the battery powers the circuit without a voltage drop across a resistor. During normal operation, the battery is charged by constant voltage through the 140Ω resistor and 1N914 diode. The zener diode protects the system from over-voltage when the battery is not in the circuit.

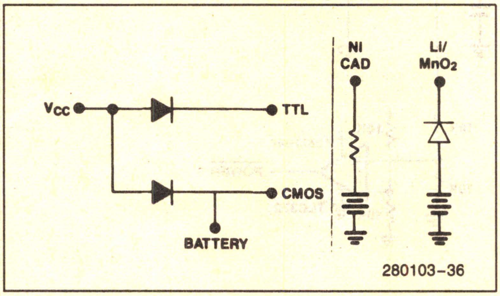


Figure 20. Simple Battery Isolation

Note that the battery charging accommodation in Figure 23 does not provide any protection from overcharging the battery. The others (Figures 20, 21 and 22) are somewhat protected by the lower input voltage used. Overcharging is addressed in the two stage battery charging circuits later in this section.

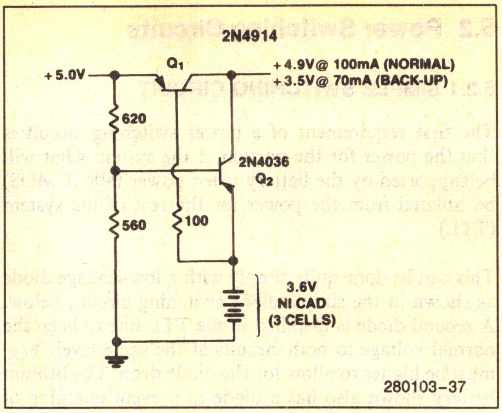


Figure 21. Dual Voltage Circuit

5.3 Protection From False Signals

5.3.1 RESET CIRCUITS

In a battery back-up system, care should be taken to protect the memory from false signals, during both back-up and power-up, which could alter the data that is to be preserved. To avoid any possibility of this happening, write enable ($\overline{\text{WE}}$) is held high during back-up and the normal chip select ($\overline{\text{CS}}$ or $\overline{\text{RAS}}$) is gated with the system power-up reset. For additional insurance, gate $\overline{\text{WE}}$ with the reset as well. The simplest reset circuit (Figure 25) is the resistor/capacitor, but it can briefly cause oscillations out of the associated logic circuits as it moves slowly through the threshold level. Putting a Schmitt triggered device on it improves the situation (Figure 24). The three transistor reset circuit (Figure 26) prevents oscillations by providing a more normal risetime to the logic circuits following the delay. When power first comes up, the RC time constant on its base keeps Q1 off which, in turn, keeps Q2 and Q3 off, holding $\overline{\text{RESET}}$ low. When the charge on the capacitor rises to threshold, Q1 turns on, turning on Q2 and Q3 and pulling $\overline{\text{RESET}}$ high.

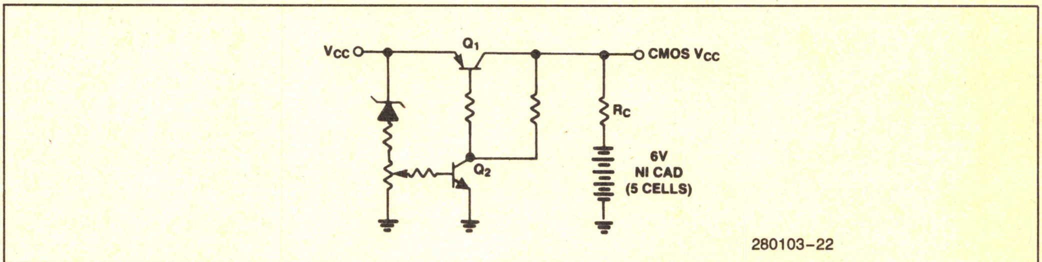


Figure 22. Transistor Isolation for Battery Back-up

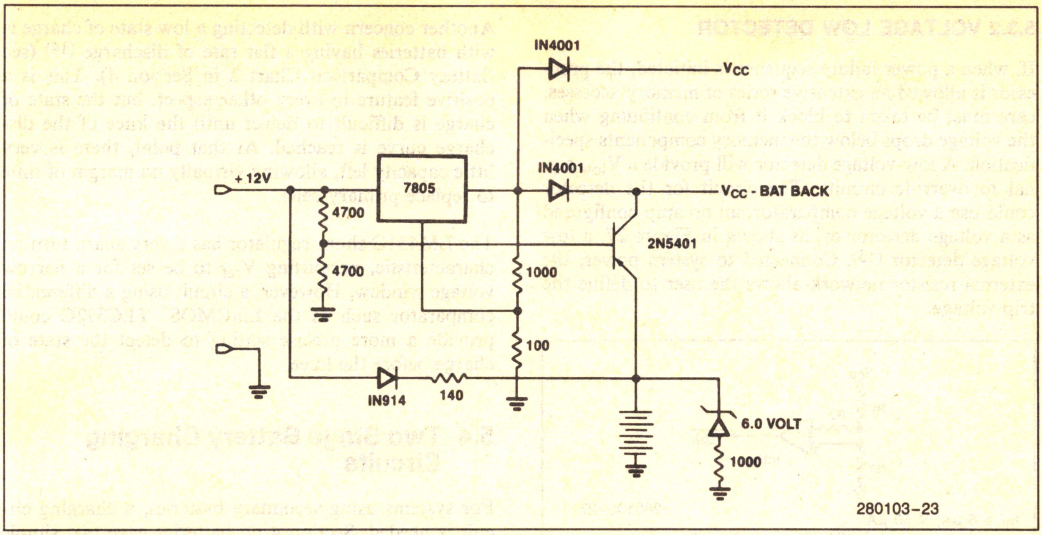

IN4001
Vcc
IN4001
Vcc - BAT BACK
+12V
7805
4700
4700
2N5401
1000
100
IN914
140
6.0 VOLT
1000
280103-23

Figure 23. Transistor Switch for Battery

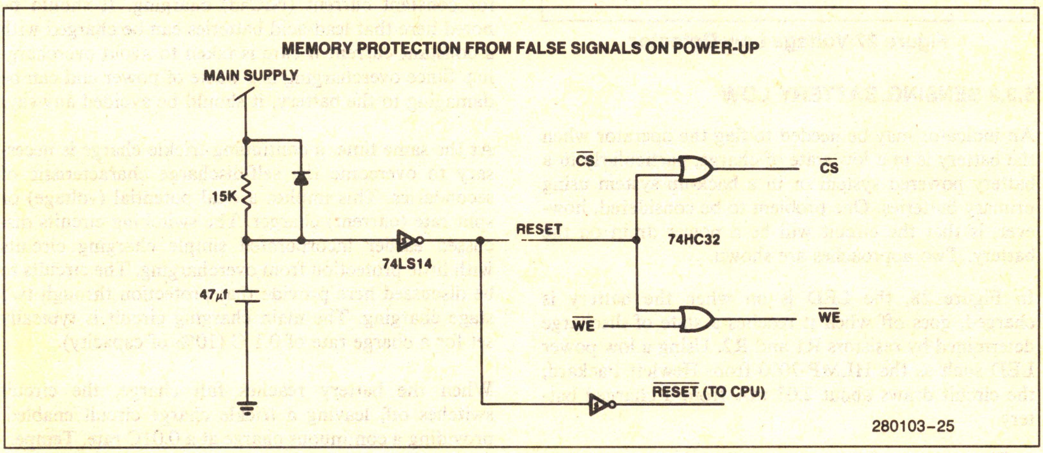

MEMORY PROTECTION FROM FALSE SIGNALS ON POWER-UP
MAIN SUPPLY
15K
74LS14
47μf
RESET
CS
CS
74HC32
WE
WE
RESET (TO CPU)
280103-25

Figure 25. Schmitt Trigger Isolated Reset

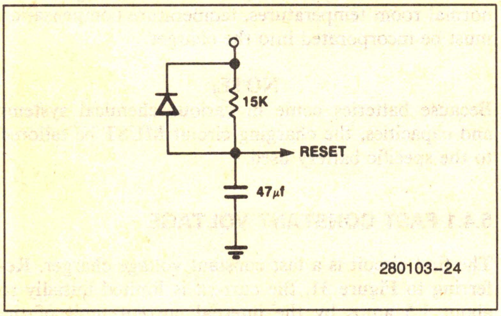

15K
RESET
47μf
280103-24

Figure 24. Simple Reset Circuit

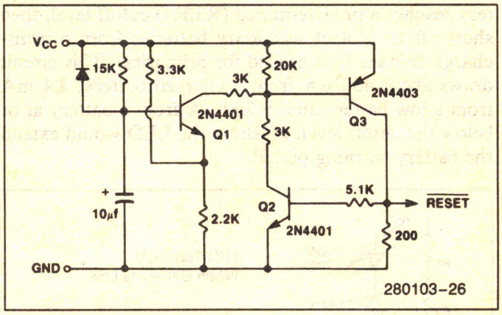
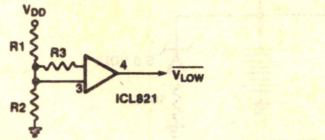

Vcc
15K
3.3K
20K
3K
2N4403
2N4401
Q1
3K
Q3
+
10μf
2.2K
Q2
2N4401
5.1K
RESET
200
GND
280103-26

Figure 26. Reset Circuit Protects From Oscillation

5.3.2 VOLTAGE LOW DETECTOR

If, when a power failure sequence is initiated, the processor is allowed an extensive series of memory accesses, care must be taken to block it from continuing when the voltage drops below the memory components specification. A low-voltage detector will provide a V_{low} signal to override circuits. The circuit for the detector could use a voltage comparator, an op amp configured as a voltage detector or, as shown in Figure 27, a low voltage detector (13). Connected to system power, the external resistor network allows the user to define the trip voltage.



$I_{R1} \geq 6\ \mu A, \leq 50\ \mu A$

$$\text{Trip Voltage } V_{TR} = \left(\frac{R1\ R3}{(R1 + R3)} + R2\right) \times \frac{1}{R2} \times 1.15V$$

Figure 27.Voltage Low Detector

5.3.3 SENSING BATTERY LOW

An indicator may be needed to flag the operator when the battery is in a low state of charge, particularly in a battery powered system or in a back-up system using primary batteries. One problem to be considered, however, is that the circuit will be a power drain on the battery. Two approaches are shown.

In Figure 28, the LED is on when the battery is charged, goes off when it reaches a state of discharge determined by resistors R1 and R2. Using a low power LED such as the HLMP-7000 from Hewlett Packard, the circuit draws about 2.03 mA from a charged battery.

In Figure 29, the LED turns on when the battery is low (determined by R1 and R2). It stays on until the battery reaches a predetermined (R3,R4) cutoff level, then shuts off to protect secondary batteries from overdischarge damage (not needed for primaries). This circuit draws about 430 μA from a charged battery, 2.4 mA from a low battery and ~200 μA from a battery at or below the cutoff level. Flashing the LED would extend the battery warning period.

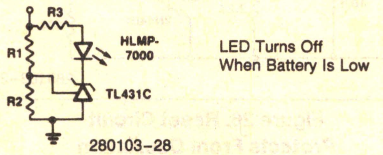


Figure 28. Battery Low Indicator #1

Another concern with detecting a low state of charge is with batteries having a flat rate of discharge (14) (see Battery Comparison Chart 2 in Section 4). This is a positive feature in every other aspect, but the state of charge is difficult to detect until the knee of the discharge curve is reached. At that point, there is very little capacity left, allowing virtually no margin of time to replace primary cells.

The LM431C shunt regulator has a very sharp turn-on characteristic, permitting V_{ref} to be set for a narrow voltage window. However, a circuit using a differential comparator such as the LinCMOS* TLC372C could provide a more precise setting to detect the state of charge before the knee.

5.4 Two Stage Battery Charging Circuits

For systems using secondary batteries, a charging circuit is needed. Section 4 on batteries gave two simple circuits, one for constant voltage (lead-acid), the other for constant current (NiCad) charging. It should be noted here that lead-acid batteries can be charged with a constant current if care is taken to avoid overcharging. Since overcharging is a waste of power and can be damaging to the battery, it should be avoided anyway.

At the same time, a continuing trickle charge is necessary to overcome the self-discharge characteristic of secondaries. This implies a dual potential (voltage) or split rate (current) charger. The switching circuits discussed earlier incorporated simple charging circuits with little protection from overcharging. The circuits to be discussed here provide that protection through two stage charging. The main charging circuit is typically set for a charge rate of 0.1 C (10% of capacity).

When the battery reaches full charge, the circuit switches off, leaving a trickle charge circuit enabled, providing a continuous charge at a 0.01C rate. Temperature affects the charge acceptance of the battery so, if it is to be re-charged at higher rates or in higher than normal room temperatures, temperature compensation must be incorporated into the charger.

NOTE:

Because batteries come in various chemical systems and capacities, the charging circuit MUST be tailored to the specific battery used.

5.4.1 FAST CONSTANT VOLTAGE

The first circuit is a fast constant voltage charger. Referring to Figure 31, the current is limited initially to about 1.5 amps by the internal current limit of the

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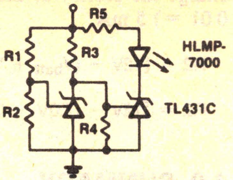
*LinCMOS is a trademark of Texas Instruments



LED Is Off When Battery Is Charged, Turns On When Battery Is Low And Turns Off Again When Battery Is Discharged To Cutoff Level.

280103-29

$$R1 + R2 = \frac{V_L}{10(I_{ref})}$$

$$R2 = \frac{V_{ref}}{10(I_{ref})}$$

$$R3 = \frac{V_L - V_{RF}}{I_F} \quad \text{or} \quad \frac{V_C - V_{ref}}{I_T}$$

$$I_T = \frac{V_C - V_{ref}}{R3}$$

$$R4 = \frac{V_{ref}}{I_T}$$

$$R5 = \frac{V_C - V_{LF} - V_{RF}}{I_L}$$

Where:

V_L = Battery Low Voltage
V_C = Battery Cutoff Voltage
V_{ref} = Regular Ref. Input Voltage
I_{ref} = Reg. Ref. Input Current
V_{LF} = Led Forward Volt. Drop
V_{RF} = Reg. Forward Volt. Drop
I_L = Led Min. Forward Current
I_F = Reg. Min. Forward Current
I_T = R3 + R4 Current To Turn On Led

For Example:

V_L = 5.8V
V_C = 5.1V
V_{ref} = 2.5V
I_{ref} = 2 μA
V_{LF} = 1.8V
V_{RF} = 0.0005V
I_L = 2 mA
I_F = 400 μA

$$R1 + R2 = \frac{5.8\text{V}}{20\ \mu\text{A}} = 290\text{K}$$

$$R2 = \frac{2.5\text{V}}{20\mu\text{A}} = 125\text{K}$$

$$R1 = 290\text{K} - 125\text{K} = 165\text{K}$$

$$R3 = \frac{5.8 - 0.0005}{400\ \mu\text{A}} = 14.5\text{K}$$

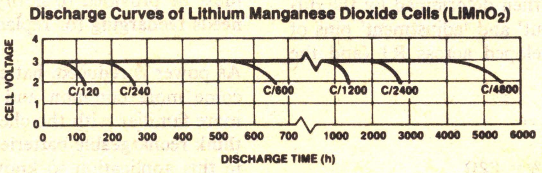
$$I_T = \frac{5.1 - 2.5}{14.5\text{K}} = 179.3\ \mu\text{A}$$

$$R4 = \frac{2.5}{179.3\ \mu\text{A}} = 13.9\text{K}$$

$$R5 = \frac{5.1 - 1.8 - 0.1}{2\ \text{mA}}$$

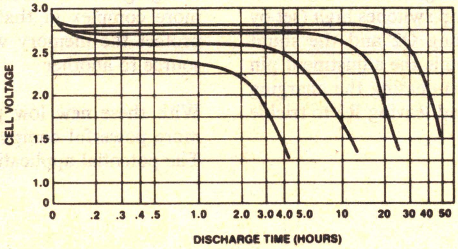
$$R5 = 1.6\text{K}$$

Figure 29. Battery Low Indicator #2


Discharge Curves of Lithium Manganese Dioxide Cells ($LiMnO_2$)

280103-30

A. Typical Discharge Curves for Button Cells at 68°F (20°C)



280103-31

B. Typical Discharge Curves, Cylindrical Cells at 68°F (20°C)

Reprinted Courtesy of Duracell Bulletin # 980LM, MAY 1984

Figure 30. Discharge Curves of Lithium Manganese Dioxide Cells

LM317. As the charge on the battery increases, the current to the battery (through R6) decreases. When the voltage across R6 decreases below the voltage across R2, the outout of the op amp goes low, reducing the effective value of R1 and lowering the output of the voltage regulator. This terminates the voltage regulator charging of the battery and leaves the trickle charge resistor R7 to maintain the battery at the 0.01C rate. In addition, when the output of the op amp goes low, it turns on the LED, indicating the battery has reached full charge. A momentary contact switch is provided to initiate a charge cycle on a partially discharged battery. The diodes on the positive terminal of the battery prevent the battery from being discharged through the charger circuits when the line power is off.

5.4.2 CURRENT LIMITED CONSTANT VOLTAGE

The second circuit is a current limited constant voltage charger. The charge current is set by resistor R3. When the voltage across the battery reaches (for lead acid, 2.35 × 3 =) 7.05 volts indicating full charge, the shunt regulator turns on which, through the transistor, pulls the LM317 'adjustment' pin low shutting down the voltage regulator. This leaves the trickle charge resistor to maintain the battery.

5.4.3 CONSTANT CURRENT

The final circuit is a constant current charger. R3 adjusts the range wherein the voltage regulator turns on and off, R9 and R12 adjust the point at which the op amp switches. The charge current is set by R1. At 5.0V the op amp switches low (adjusted by R3 and R12), turning off Q2 and the shunt regulator and turning on Q1. The charge current is then determined by the differential between the 'output' and 'adjustment' pins of the voltage regulator, developed across R1 (and the transistor). In this case:

$$R1 = (1.2V - V_{CE})/0.1C =$$

$$R1 = (1.2V - 0.1V/50\ mA = 22\Omega$$

When the battery reaches full charge (for NiCad, 1.4V/cell × 5 cells = 7.0V) the op amp switches high (set by the zener diode and R9), turning Q2 and the shunt regulator on and Q1 off. This pulls the adjustment pin of the voltage regulator low, terminating the charging of the battery by the regulator and leaving R2 to trickle charge the battery at the 0.01C rate of (500 mAh × 0.01 =) 5 mA.

$$R2 = [12V - (V_{batt} + V_{diode})]/0.01C =$$

$$R2 = [12V - (7.0V + 0.8V)]/5\ mA = 840\Omega$$

6.0 SUMMARY

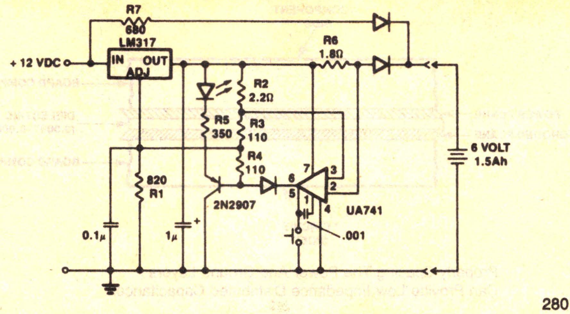
The new availability of a wide variety of fast CMOS products can lead to many new, low power applications such as lap or portable computers and high-speed solid state disks. The designer will have to consider a number of issues unique to this low power environment. For example, CMOS products have a much greater change from standby to active current than NMOS products so, while they expand the options (low power, high bandwidth, etc.) available to the design engineer, care must be taken to power them properly. This means proper decoupling and possibly more use of four layer printed circuit boards with power and ground inner layers. (Figure 34)

Many new products are in development (such as an 82C85 clock generator with the ability to stop the clock and an 82C08 CHMOS DRAM controller that supports extended refresh) that will help the designer take advantage of the features of the CMOS products and (s)he will have to stay abreast of them.

Systems to be operated with the limited power of a battery must be designed with careful attention to keeping active power low and making maximum use of the low power features of CMOS, features like stopping the clock and extended refresh. At the same time, means must be provided to notify the user when the battery needs recharging (or replacing).

As power is reduced, battery powered systems will become more common and the designer must become more familiar with the chemical systems available. We think rechargeable batteries will be the more prevalent in this application so knowledge of methods both for detecting batteries in a low state of charge and for recharging will be necessary. Battery backup is a little more complex in that special care must be taken to protect the memory when switching from one power source to another.

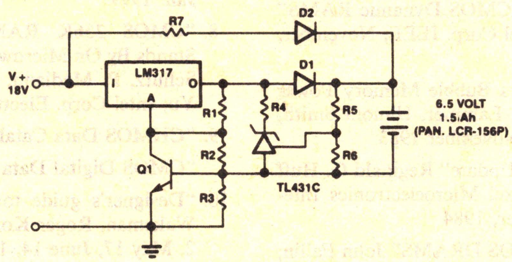
With these new low power products, new and much more powerful computing products can be developed. The potential applications are legion.


R7
680
LM317
+12 VDC
IN
OUT
ADJ
R6
1.8Ω
R2
2.2Ω
R5
350
R3
110
R4
110
820
R1
2N2907
0.1μ
1μ
7
3
6
2
5
1
4
UA741
.001
6 VOLT
1.5Ah

280103-32

Figure 31. Two Stage Fast Constant Voltage Charger

Current Limited Constant Voltage Charger


R7
D2
LM317
V+
18V
I
O
A
D1
R1
R4
R5
6.5 VOLT
1.5 Ah
(PAN. LCR-156P)
R2
R6
Q1
TL431C
R3

280103-33

Overcharge Protection:

V_{REF} (TL431C) = 2.5V

$$\text{High Limit} \approx V_{REF}\left(1 + \frac{R5}{R6}\right)$$

High Limit = 2.35 V/Cell × 3 Cells = 7.05V

$I_{REF} = 3\ \mu A$

I_{R5} (and I_{R6}) = 10 (I_{REF}) = 30 μA

$$R5 + R6 = \frac{7.05}{30\ \mu A} = 235\ K\Omega$$

$$R6 = \frac{V_{REF}}{I_{R6}} = \frac{2.5V}{30\ \mu A} = 83.3\ K\Omega$$

R5 = 235K − 83.3K = 151.7 KΩ

Trickle Charge:

$$R7 = \frac{(V+) - V_{D2} - V_B}{I_T}$$

$$R7 = \frac{18V - 0.8V - 7.05V}{15\ mA} = 676.7 = 680\Omega$$

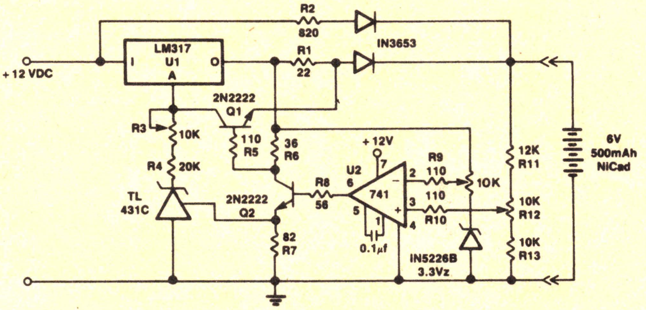
Where:

V_{D2} = Voltage Drop Across D_2

V_B = Voltage Across Fully Charged Battery

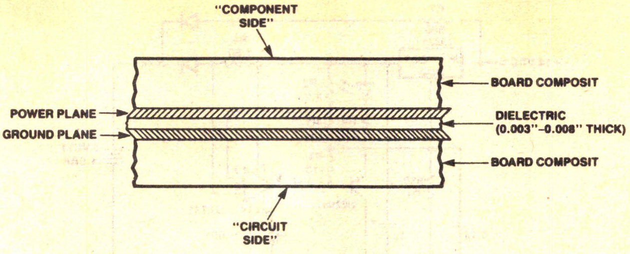
I_T = Trickle Charge Current

Figure 32. Two Stage Current Limited Constant Voltage Charger


R2
820
LM317
U1
I
O
A
+12 VDC
R1
22
IN3653
2N2222
Q1
R3
10K
110
R5
36
R6
+12V
R4
20K
R9
110
10K
U2
7
2
6
741
12K
R11
6V
500mAh
NiCad
TL
431C
2N2222
Q2
R8
56
3
110
5
1
4
R10
10K
R12
82
R7
0.1μf
IN5226B
3.3Vz
10K
R13

280103-34

Figure 33. Two Stage Constant Current Charger



280103-35

Properly Spacing The Power And Ground Layers
Can Provide Low Impedance Distributed Capacitance

Figure 34. Four Layer P.C. Board

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Modular Approach To C-MOS Technology Tailors Process To Application

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Modular approach to C-MOS technology tailors process to application

Despite the proliferation of applications, a few C-MOS process variations can address the functional requirements of many different products

by Kim Kokkonen and Richard Pashley, *Intel Corp., Santa Clara, Calif.*

☐ In the past few years, the interest in complementary-MOS technology and its applications to new products has exploded. Traditional arguments for C-MOS center on its low power dissipation, the large noise margins of complementary logic, and its simple ratioless design. With the advent of very large-scale integration, these arguments are taking on new meaning and importance.

As an example, Fig. 1 compares the performance of H-MOS (high-performance n-channel MOS) inverters with their equivalent in Intel's C-H-MOS (complementary high-performance MOS) technology. Though H-MOS's speed continues to improve with further scaling, its delay-power product is more than an order of magnitude higher than a C-H-MOS implementation with identical n-channel transistors. In a VLSI part with 50,000 gates, C-H-MOS could mean the difference between 1 and 10 watts of power dissipation, which might save the expense and difficulty of a sophisticated cooling system or extend a portable system's operating time by a factor of 10.

That C-MOS performance is now on a par with n-MOS technology has also accelerated its popularity. In addition, the density of C-MOS circuitry has improved dramatically with advances in technology. Finally, the number of process alternatives has grown so large that almost any integrated-circuit design can be supported with available C-MOS technology.

Unfortunately, the wave of enthusiasm for C-MOS and the needs of different applications have multiplied the number of approaches that C-MOS developers are taking. Several major issues remain in VLSI C-MOS design—namely latchup and soft-error prevention, interconnections, and logic-design techniques. A building-block approach with a limited number of basic process modules can be used to create a close-knit family of technologies that squarely addresses these issues and simultaneously supports a wide range of applications.

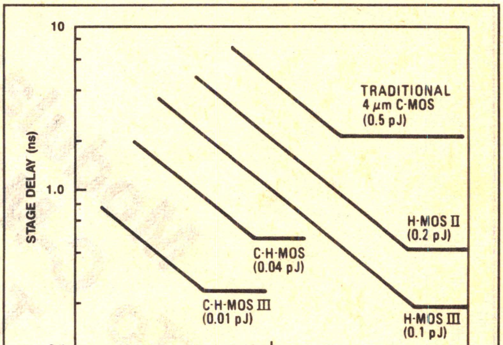
The basis for C-H-MOS

A firm foundation in n-MOS-transistor physics will support the advancement of C-MOS technology. As channel lengths approach 1 micrometer, n-channel transistors become more difficult to optimize because the standard 5-volt power supply causes problems with high-intensity fields. Improperly designed transistors may be unreliable as a result of hot-carrier injection into gate oxides, or they may cause less localized problems by injecting carriers into the MOS substrate—there to bleed charge from storage nodes or even trigger a destructive latchup.

The resources to develop and verify the reliability of a 1-μm n-channel transistor are well established and substantial. In Intel's C-H-MOS process, the basic design of the n-channel transistor is identical to its H-MOS counterpart, as shown in the table. Even at the more detailed levels of doping profiles, the H-MOS and C-H-MOS transistors are nearly identical.

Thus a high-performance C-MOS technology may be born out of an established n-MOS line. The relatively simple addition of an n-well in the same high-resistivity substrate results in a C-MOS process that serves as the basis for several optimized technologies. This is just a start, however, as other important issues remain.

Latchup has been the traditional nemesis of C-MOS. Given the presence of parasitic silicon controlled rectifiers within every bulk C-MOS chip, a current pulse of sufficient magnitude either inside or outside the chip may cause a catastrophic latchup. Many schemes have been proposed to combat latchup, ranging from carefully scrutinizing the layout (which imposes no burden on the technology) to a buried layer (which significantly in-



1. Power down. Despite the continuous improvement of H-MOS (high-performance MOS) by scaling, the delay-power product for C-H-MOS (complementary-MOS H-MOS) is more than an order of magnitude lower in the typical integrated circuit.

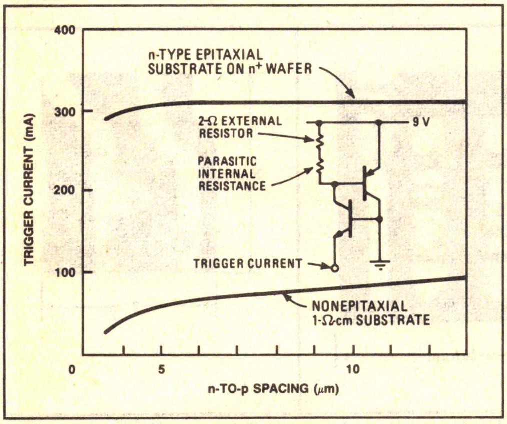
n-CHANNEL TRANSISTOR COMPARISON					
Technology		Gate-oxide thickness (Å)	Channel length (μm)	Threshold voltage (V)	Graded drain profile
n-MOS	C-MOS				
H-MOS I	—	700	3.0	0.7	no
H-MOS II	C-H-MOS	400	2.0	0.7	no
H-MOS II	C-H-MOS III	250	1.0	0.7	yes

creases complexity and processing cost). All have some degree of effectiveness.

A modular approach to a broad-based line of C-MOS technologies requires other measures besides mere physical latchup resistance. The latchup spoiler must be applicable to dynamic random-access memories, erasable programmable ready-only memories, and static RAMs, as well as to microprocessors and controllers. In order to improve latchup resistance, it cannot increase the distance between n- and p-channel transistors (this constraint is most significant in random logic and full C-MOS six-transistor static-RAM cells). The technique must be compatible with low-cost and large-volume manufacturing. Finally, the approach must be consistent with the use of an automated checking algorithm, so that every gate of a large semirandom logic design need not be scrutinized for latchup susceptibility.

Epitaxial benefits

Figure 2 shows the margin gained in latchup trigger current when an epitaxial substrate is used. The epitaxial substrate brings the same latchup benefits to all product lines, and in many cases provides additional advantages such as improved surface lifetimes (for dynamic RAMs) and reduced dc resistance (for E-PROMs and logic). Epitaxial substrates are now available in volume from commercial silicon vendors, adding less than 5% to the cost of a finished wafer. No additional or exotic fabrication equipment needs to be installed. Because the epitaxial substrate's heavily doped bulk effectively eliminates the vertically triggered latchup mode, it is possible to develop a set of computer-aided-design tools that can flag latchup-sensitive layouts on the largest VLSI chips.



2. Benefits. By raising the margin of latchup trigger current, an epitaxial substrate effects a dramatic improvement in combatting latchup, a major concern in complementary-MOS chip design.

Since grasping the phenomenon of upsets induced by alpha particles, in 1977, memory designers have taken care to ensure that enough charge is stored within each cell to minimize the problem. As critical chip dimensions are reduced, this problem becomes more severe, however, since both parasitic and storage capacitances are naturally reduced. For the latest 1.5-μm n-MOS process, stored charge is low enough to caution even microprocessor designers to guard against random storage nodes suffering from soft errors. Fortunately, C-MOS provides a natural barrier against soft errors if the storage node is located within the C-MOS well.

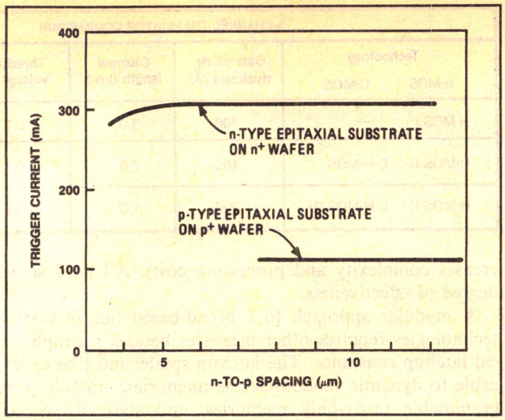
The well junction is reverse-biased by the power-supply voltage. The electric field at this junction naturally repels any carriers generated outside the well that might otherwise diffuse up to surface storage nodes. The combination of the well structure and an epitaxial substrate is even more effective. Here the funneling mechanism that usually collapses local electric fields during the passage of an alpha particle is also minimized. By using epitaxial substrates and the protection of a C-MOS well, the amount of charge collected during an alpha event can be reduced by an order of magnitude.

Of course, the designer must arrange for the storage node to reside within the well. This constraint, combined with other performance issues, leads to different choices of well and substrate polarities, depending on application. For example, in a C-MOS technology that is optimized for dynamic RAM, the ideal memory cell should have a p-channel pass gate and a p-channel capacitor located within an n-well in a p-type substrate. The p-channel transistor is chosen because it injects far fewer spurious carriers into the substrate and thus does not by itself disturb the state of neighboring cells.

The conductance of the p-channel device, while lower than that of an n-channel device of the same size, does not degrade the RAM's performance, since dynamic-RAM sensing is limited primarily by the amount of stored charge. Experimental results with C-H-MOS dynamic RAMs based on these principles show a soft-error rate of less than 300 FIT (failures in time, or device failures per billion hours) at a power supply of only 3 V. This is an improvement of more than three orders of magnitude over traditional n-MOS dynamic-RAM technology and offers the possibility of dynamic-RAM systems that require no error correction and that are compatible with low-voltage battery backup.

High-density, high-performance static RAMs present the other side of the coin. The smallest static-RAM cells today are built using polysilicon-load resistors that sustain the stored-node voltage. On the time scale of an alpha event, however, these resistors in effect do not exist. Because the storage node's RC time constant is on the order of milliseconds and the alpha event's time scale is nanoseconds, the cell appears dynamic. In this sense, polysilicon-load static-RAM cells are very similar to dynamic-RAM cells. The major difference arises in the way the cells sense the cell's information. The static-RAM cell provides a direct current, and to maximize the cell's performance, that current must be as large as possible while contained in a minimum area. Thus the chip designer must use high-gain n-channel transistors for the cell's pass gates and pulldowns. For good soft-error protection, then, the cell must be located in a p-well within an n-type substrate.

The p-well approach benefits even full C-MOS six-transistor static-RAM cells. The area of such cells depends strongly on the distance allowed between n- and p-channel devices. Using a straightforward implementation of epitaxial C-MOS, the p-well approach provides more margin against latchup at small n-to-p spacings (Fig. 3). This phenomenon occurs because of the differing diffusion properties of n- and p-type dopants. The heavy doping in the n-type substrate is less mobile than is the p-type dopant, resulting in less outdiffusion during thermal processing and thus minimizing the shunt resistance that controls latchup.



3. P-well margin. With an epitaxial substrate, a p-well structure (upper curve) yields a greater margin against latchup than n-well at smaller n- and p-device spacings.

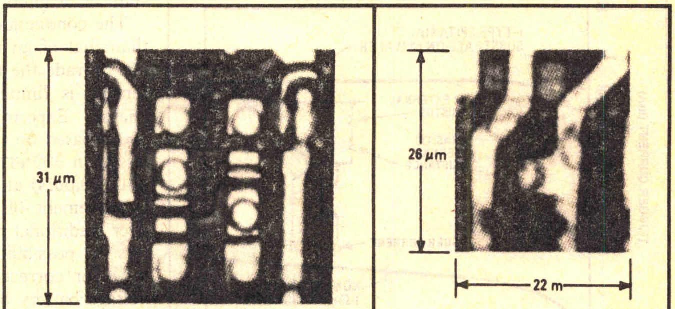
Hooking it up

One of the challenges of C-MOS in logic applications is interconnection. Designers of n-MOS chips are accustomed to buried contacts, which directly connect n-type polysilicon and n-type transistor source or drain regions. Because C-MOS requires contact to both p and n regions, the traditional n-type buried contact becomes much less useful, and a version suitable for both diffusion polarities is quite difficult to implement. This increases the burden on contact and metallization modules.

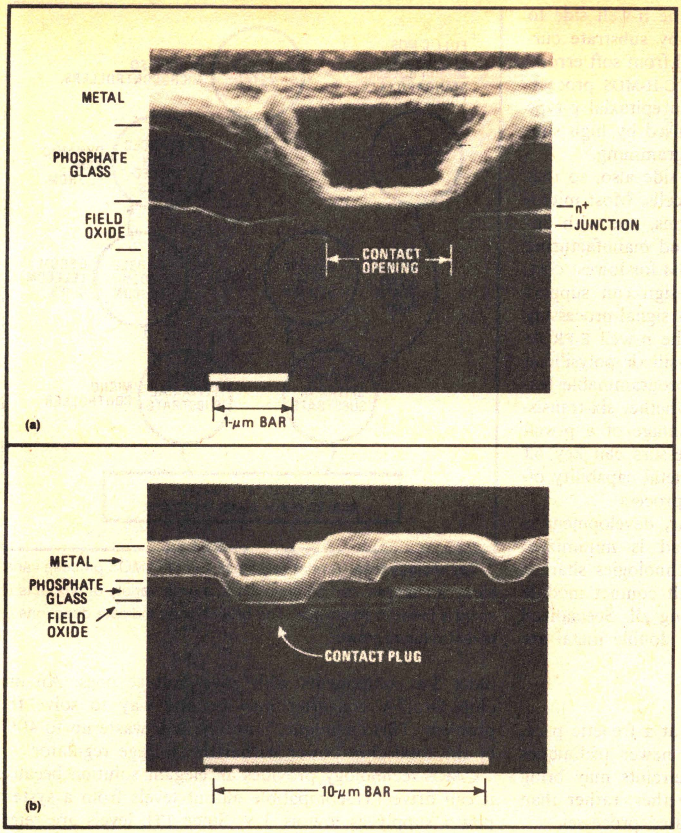
For high-density C-MOS logic, the first level of metal is all but consumed by local connections between p and n transistors. The payback from adding a second level of metal for longer-distance routing is very high. A good example exists for the six-transistor static-RAM cell commonly used by logic designers. Figure 4 compares single- and double-metal versions of this cell, both implemented with 1.5-μm design rules. Here the second-metal layer provides the bit lines for the cell. Similar arguments justify the use of second metal in global power, clock, and data routing in complex microprocessor chips.

Contacts themselves are more difficult to build in C-MOS. N-MOS technology accustomed process engineers to adding a phosphorus contact plug after the contacts have been etched. This plug brought several advantages: the phosphorus gettered metallic contaminants from the wafer, reducing junction leakage; and the high-temperature diffusion rounded the profile of the contact sidewall, easing the step coverage of the metal subsequently deposited. Further, the plug had self-aligning features. If the contact etch attacked the silicon substrate or if the contact was misaligned toward the field-oxide edge, the plug would rejuvenate the resulting weakened junctions. In C-MOS, these same attributes must be obtained differently, through improved fabrication, cleanliness, new gettering techniques, improved dielectrics, and tightly controlled contact etching. Figure 5 shows the difference in implementing a 1.5-μm contact structure in n-MOS and C-MOS.

Along with the proliferation of C-MOS technologies has come a wave of innovation in C-MOS design techniques. For digital logic, the major contenders for broad use are full complementary design and domino logic, first proposed by AT&T Bell Laboratories (Fig. 6). For many applications, traditional C-MOS logic is a winner. It requires no clocks, has larger operating margins, and uses fewer transistors for simple gates. For more complex gates, however, domino logic uses fewer transistors and runs faster. The speed results from connecting fewer transistors in series and reducing gate-fanout loading by



4. Payback. The use of double-metal layers for a six-transistor static-RAM cell can produce a large savings in real-estate. In two cells implemented with a 1.5-μm design rules, the savings can amount to one third of the total area. The cell at right uses second-layer metal for bit lines.



5. Making contact. Contacts are more difficult to build in C-MOS than in conventional n-MOS. The phosphorous contact plug used in n-MOS after contact etching (a) adds desirable features such as reduced junction leakage and improved step coverage by the metal layer. To gain the same advantages in C-MOS requires greater process control (b).

up to a factor of two compared with full C-MOS.

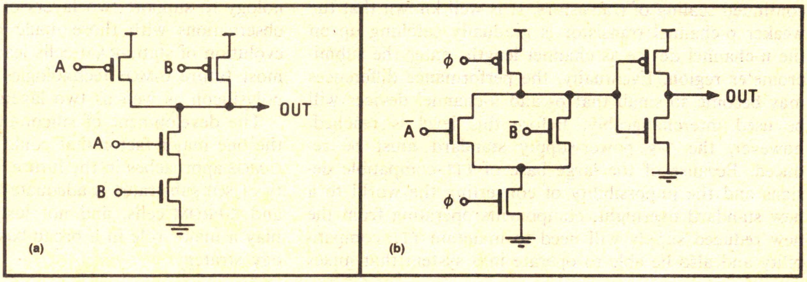
Interestingly, the choice of design style influences the optimal type of C-MOS well. The speed of full C-MOS is limited by the slower of the two transistor polarities. Since the trip point is quite close to half the power supply, the time required for either transistor type to discharge its load capacitance by about 2.5 V sets the gate's speed. Since the p-channel device is the weaker one, it pays to choose a well type that improves the p-channel's conductance. P-well does this because the p-device is fabricated in an uncompensated substrate and thus has maximum mobility. Comparisons between n- and p-well construction show that the p-channel's conductance may be improved by as much as 10% with the proper well type.

By contrast, domino logic is at its best in an n-well technology. Here, the n-channel transistor dominates both performance and transistor count. Placing the n-channel device outside the well improves its conductance and reduces the dominant parasitic junction capacitance. Density also increases because no well contacts are required for the majority of the transistors.

The twin-well approach to C-MOS blurs these distinctions. In this approach, a high-resistivity epitaxial layer is grown on a heavily doped starting wafer. Then the doping for each transistor polarity may be independently optimized without need for doping compensation. Performance arguments based on mobility or junction capacitance thus become moot. Nonetheless, domino logic will still be best on a p-type substrate (equivalent to n-well) because it does not require well contacts to collect the large parasitic substrate currents from the n-channel transistors, thus improving packing density.

Matching process to product

These and other technical arguments may be combined into a consistent strategy (Fig. 7) for creating a line of C-MOS processes serving a broad marketplace. For at least the next several years, a complete technology line must include C-MOS based on both p- and n-type substrates. Fortunately, choosing epitaxial-latchup control minimizes the development cost of running both process-



6. Logic. Two major contenders for digital logic design are full complementary (a) and domino logic (b). The former requires no clocks and is simpler for many applications. Domino logic, which performs best in an n-well technology, is faster and simpler for more complex circuits.

es. Dynamic RAMs are supported on the n-well side to minimize pattern sensitivities induced by substrate currents while protecting the p-channel cell from soft errors. E-PROMs are built in a similar n-well C-H-MOS process. Placing Intel's n-MOS E-PROM cell in an epitaxial p-type substrate eliminates parasitic effects caused by high substrate currents flowing during cell programming.

Microcontrollers land on the n-well side also, so that they may incorporate on-chip E-PROM cells. Most microcontroller products come in two versions, one with on-chip E-PROM for system-development and manufacturing flexibility, and another with on-chip ROM for lowest cost. Using n-well C-MOS, a single core design can support both versions. Telecommunications and signal-processing products can also take advantage of the n-well E-PROM process, both for its high-quality polysilicon-polysilicon capacitors and for the E-PROM cell's programmable features. High-performance static RAMs, whether six-transistor or polysilicon-load, can take advantage of a p-well C-H-MOS process. High-end microprocessors can key off the dense n-to-p packing and double-metal capability offered by the six-transistor static-RAM process.

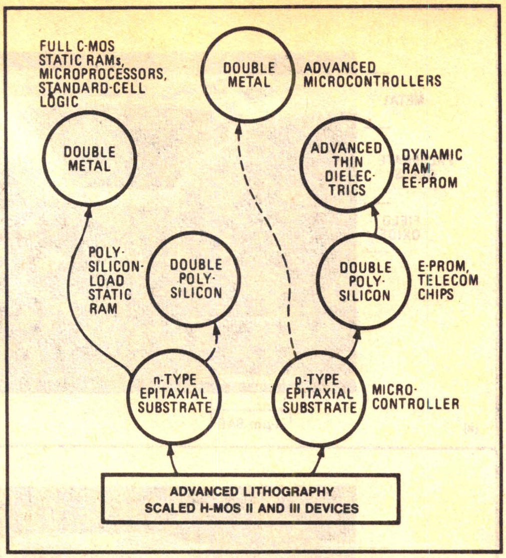
Because these processes are modular, development is simplified and manufacturing overhead is minimized. Just as all the 1.5-μm C-H-MOS III technologies share a common transistor module, the difficult contact module was developed once to be shared among all. Specialized features such as double polysilicon or double metal are extensions of the common base.

The future

C-MOS technology is still developing at a frenetic pace. Surprisingly, the application of some newer techniques and the demands of next-generation circuits may bring the various forms of C-MOS closer together, rather than further splitting the number of integrated processes.

One example of this trend is the development of a trench-isolation technique for separating n and p devices. When this module is perfected, there will be no reason to develop six-transistor static-RAM cells on p-well technology. The near-ideal trench isolation will prevent latchup on either substrate type. Similarly, if stacked C-MOS static-RAM cells can be perfected, there will be no need for polysilicon loads. The stacked C-MOS cell will have the same density but with improved performance and soft-error immunity. At that time, twin-well C-MOS on a p-type substrate, augmented by specialized features for specific product lines, will become the one approach to a broad line of C-MOS processes.

Another factor affecting future C-MOS integration is the continued scaling of transistors. It is well known that the weaker p-channel transistor is gradually catching up on the n-channel device as channel lengths enter the submicrometer region. Eventually, the performance differences may become so small that p- and n-channel devices will be used interchangeably. Before this level is reached, however, the 5-V power-supply standard must be reduced. Because of the large base of TTL-compatible designs and the impossibility of converting the world to a new standard overnight, components operating from the new reduced supply will need to maintain TTL compatibility and also be able to operate in a system that mixes older 5-V components with lower-voltage ones. An on-chip 5-to-3-V converter may be one way to solve the problem. This technique, however, will waste up to 40% of the total chip power within the voltage regulator.


FULL C-MOS STATIC RAMs, MICROPROCESSORS, STANDARD-CELL LOGIC
DOUBLE METAL
DOUBLE METAL
ADVANCED MICROCONTROLLERS
ADVANCED THIN DIELEC-TRICS
DYNAMIC RAM, EE-PROM
POLY-SILICON-LOAD STATIC RAM
DOUBLE POLY-SILICON
DOUBLE POLY-SILICON
E-PROM, TELECOM CHIPS
n-TYPE EPITAXIAL SUBSTRATE
p-TYPE EPITAXIAL SUBSTRATE
MICRO-CONTROLLER
ADVANCED LITHOGRAPHY SCALED H-MOS II AND III DEVICES

7. Technology tree. A relatively small line of C-MOS process variations, or modules, can be matched to a wide variety of products to serve a broad marketplace. The broken lines indicate directions of potential future growth.

C-MOS technology provides an elegant solution because it can drive TTL-compatible output levels from a system power supply as low as 3 V. Since TTL levels are referenced to the negative (ground) rail, the grounded substrate offered by n-well C-MOS is a much-preferred means of integrating submicrometer transistors into such a system. This will be a strong motive to standardize on p-substrate C-MOS.

A final factor that tends to drive future C-MOS processes toward commonality is the growing importance of RC delays in overall chip performance. The latest high-performance static RAMs use an aluminum strap in parallel with the polysilicon word line because the RC delay induced by even the best refractory metal polycides is several nanoseconds too long. Studies of dynamic RAMs larger than 1 megabit similarly indicate that refractory word lines will probably be inadequate, forcing the technology to support two layers of metal. Combining these observations with those made previously regarding the evolution of static-RAM cells leads to the conclusion that most future C-MOS technologies will have two layers of polysilicon as well as two layers of metal.

The development of silicon-on-insulator technology is the one major factor that could renew the divergence of C-MOS approaches in the future. However, until the quality of SOI substrates is adequate to support dynamic RAM and E-PROM cells, and not just static logic, it will not play a major role in a broad-based and modular technology strategy. ☐

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CMOS outshines NMOS on high-speed digital chips

After many years in the shadow of NMOS technology, CMOS is taking over the bulk of NMOS applications, with high-speed, low-power architecture. A new CMOS RAM proves it can top NMOS in both performance and price

Steve Smith
Program Manager
of Technology Development

Dan Freitas
Senior Engineer

Intel Corp.
Static RAM Operation
Santa Clara, CA

Until recently NMOS technology was the front-running process for manufacturing digital memories and logic. It was simpler and cheaper than its archrival, CMOS. It was faster, too, and had no latch-up problems. But the scene has changed. NMOS is giving way and CMOS is taking the lead.

For one thing, today's state-of-the-art NMOS processes are far more complex than those of their predecessors. Four or five transistor types have replaced the two basic types of the past. The single-layer polysilicon and metal-interconnect schemes of early NMOS devices are losing ground to double-level polysilicon and double-level metal.

At the same time, RC time-constant delays, once critical CMOS speed limiters, are dropping, thanks to a variety of low-resistance gate techniques. The result is that the complexity of NMOS fabrication—and hence its cost—is now on par with that of CMOS.

Many factors at work

Other factors have also been at work. CMOS, with its new submicron, high-speed-geometry transistors, has been rapidly moving into NMOS high-speed digital-IC territory. In addition, its latch-up sensitivity has been brought under control, and transistor scaling has boosted the formerly weak p-channel CMOS chip to reasonable strength.

Of course, CMOS's traditional forte, low power dissipation, hasn't changed, so new chip designs can be pushed to the limit without violating package power limits. And the inherently high CMOS noise immunity allows future power-supply scaling to low signal levels with a minimum

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number of circuit changes. Clearly, CMOS is moving into the No. 1 spot for all semiconductor classifications.

Taking advantage of the new capabilities of CMOS, Intel has developed a CMOS version of its high-performance NMOS process (HMOS III). The new technology, called CHMOS III, uses p-wells on n$^-$ Epi-layer processing, which incorporates 1.3-μm p and n devices. Transistors are interconnected by two-layer metal and single-layer polysilicon. P-well processing maximizes performance. This permits tighter well-to-diffusion spacing than other methods—and the denser packing of devices.

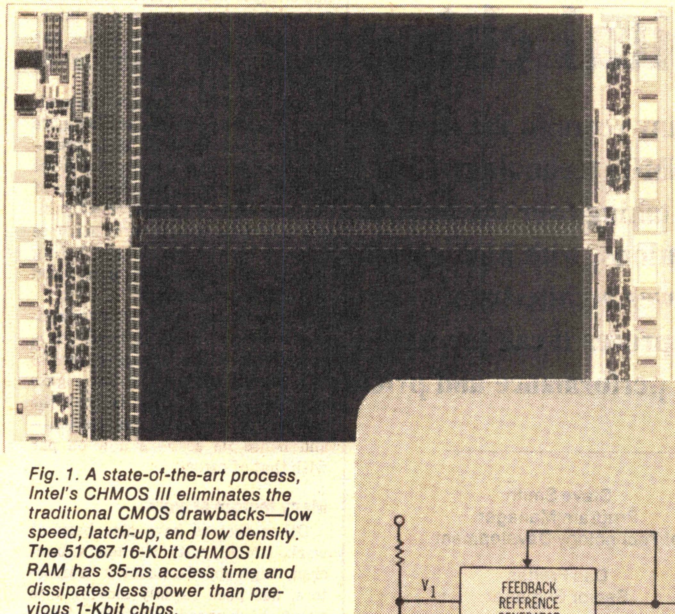


Fig. 1. A state-of-the-art process, Intel's CHMOS III eliminates the traditional CMOS drawbacks—low speed, latch-up, and low density. The 51C67 16-Kbit CHMOS III RAM has 35-ns access time and dissipates less power than previous 1-Kbit chips.

An n$^-$ Epi layer on an n$^+$ substrate virtually eliminates latch-up woes, while the low resistivity of the n$^+$ substrate shunts mosts of the dangerous substrate current to the V_{CC} supply. P-well V_{SS} taps collect any stray well currents. Double-level metal reduces parasitic RC delays in the CHMOS III. It eliminates all polysilicon interconnections of heavily loaded nodes and reduces delay significantly. For example, a typical metal-strapped static-RAM word line has a delay of ¼ ns. Using an equivalent length of polysilicon, the delay is close to 15 ns.

Sound physics

Proving that the semiconductor physics theory behind CHMOS III is sound, Intel has designed a new 16 K x 1-bit static RAM, the 51C67, using the process (see *Fig. 1*). Performance tests indicate that the device's maximum read-write cycle time is 35 ns—measured between signal lows of 0.8 V and highs of 2.0 V—with 100-mA active and 10-mA standby current limits.

To achieve a speed of 35 ns consistently throughout a manufacturing process, various process-tolerant circuit architectures must be used. One of the most process-sensitive circuits is an input buffer. Typically, a simple inverter serves as the first stage of the buffer. Although such an input device can be optimized for typical (5-V) operation, its performance is very sensitive and can degrade rapidly with variations in V_{CC}, temperature or processing.

The 51C67's input buffer uses a resistor-divider ratio to set a reference voltage (V_1) of about 1.4 V as shown in *Fig. 2*. Voltage V_1 is fed into a feedback reference generator to produce a bias voltage (V_2) for the input buffers. Voltage V_2 is maintained at such a level that the input inverters are biased just to their trip point. Thus, a small change in a pad voltage will cause a buffer's output to trip.

The reference generator is designed so that V_2 depends only on V_1. An inverter's trip point, in turn, depends on bias voltage V_2. In effect, the input buffer trip point is determined by the resistor-divider

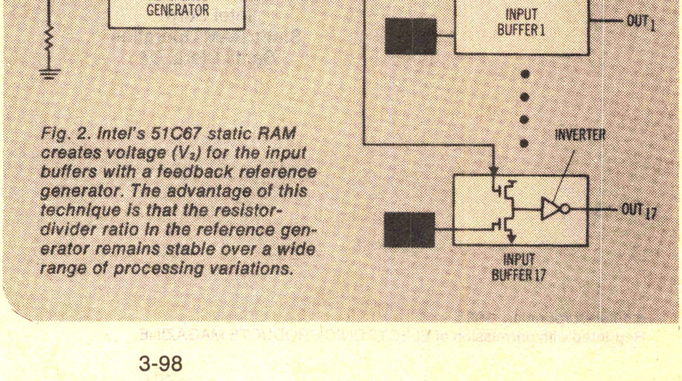


Fig. 2. Intel's 51C67 static RAM creates voltage (V_2) for the input buffers with a feedback reference generator. The advantage of this technique is that the resistor-divider ratio in the reference generator remains stable over a wide range of processing variations.

voltage. Since a resistor divider is constant over any processing variation, the input buffer's trip point is also constant over these variations.

In a high-speed RAM, the heavily loaded data path is usually clamped to avoid large, low-slew voltage swings. These clamped data signals are fed to a differential sense amplifier for level restoration and buffering before being fed to the data-out terminal pin.

The sense amplifier is usually the first device to fail under extended V_{CC}-range operation because it is a saturated-transistor circuit strongly dependent on bias voltage. Improper biasing causes the input, load, or current-source transistors to fall out of saturation. This leads to reduced gain, less common-mode rejection, and ultimately, operational failure.

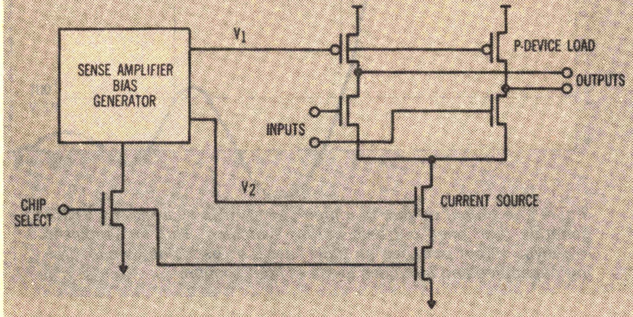


Fig. 3. A bias generator that self-compensates for temperature, voltage, and processing variations extends the range of the 51C67's sense amplifiers. Voltage V_1 and V_2 change with variations in supply voltage to rebias the sense amplifiers.

To extend the usable range of the sense amplifier, the 51C67 uses a bias-controlled differential amplifier (see *Fig. 3*). The amplifier's load and current-source transistors are biased by V_1 and V_2. As V_{CC} rises or falls, V_1 and V_2 are varied to rebias the amplifier. The bias generator is self-compensating for variations in temperature, process, and voltage. In standby, both the bias generator and sense amplifier powerdown, eliminating any linear DC power dissipation.

After differential data signals have been amplified to full CMOS levels, additional buffering is necessary before driving the output pin. The 51C67 uses a preferential delay technique to speed up the read-1 path—the reading of a logic-1 from the device. That is, the read-1 path through the buffer inverters is optimized at the expense of the time through the read-0 path.

To compensate for the additional delay in the read-0 bath, the sense-amplifier output is preset to zero upon the transition of any address. Essentially, this gives the read-0 path a head start, so the additional delay through the sense amplifier does not limit the overall access time of the device.

The 51C67's preset-to-zero scheme eliminates any unknown data-out states. It turns out that the same pulse used to preset the output also equalizes the data path. As in any equalized device, the sense-amplifier input becomes invalid during equalization. With the inputs invalid, the output data is indeterminate.

To eliminate the indeterminate state, a designer can latch, three-state, or preset the output. Latching requires a latch/unlatch clock with adequate margin to prevent latching the wrong data. But margins built into the latch directly increase access time, a less-than-desirable situation for a high-speed RAM.

Three-stating the output offers little improvement since during equalization, the output state is determined by the output load configuration. Presetting, on the other hand, forces data values to a known state during equalization, allowing the optimization of the other state.

Writing and power-down

There are always tradeoffs between the read and write circuitry of a RAM. For example, high-speed design practice dictates strong column clamps to minimize bit-line voltage swings. This is a good procedure for fast reads, but the write drivers must pull against the clamps when writing data to a memory cell. The result is a degraded low signal level, which, under some conditions, may be insufficient to write correct data to the cell.

In the 51C67, column-load switching is used to get the best of both worlds. During a read, strong column clamps enhance read speed while eliminating marginal cell conditions such as read-disturb in a noisy environment. During a write, the column clamps are switched off, allowing the column drivers to pull the column essentially to V_{SS}. This low level ensures a solid write signal in any system environment.

A key characteristic of the 51C67 is its power-down feature. During deselect—chip select (CS) set to a logic 1—the RAM goes into a low-power standby mode, dissipating only 1/10 of its active power.

However, some high-speed portions of a system cannot take advantage of power-down. An instruction cache, for example, must be continuously updated with new instructions, and thus can never be deselected.

For non-power-down applications, Intel offers a sister chip to the 51C-67, the 51C66. This RAM's access time is specified at 20 ns. Both active and standby power are specified the same, 100 mA. The 20-ns access time is the equivalent of an output-enable access for a common I/O device. In other words, after the addresses are first set up, the CS pin (equivalent to an output enable) is brought low. For normal access—with CS always low and the addresses changing—the read-access time is the same as that of the 51C67, namely 35 ns max.

Effects of noise

A data sheet may specify a RAM as a 35-ns device, yet the system fails to operate with a 40-ns strobe signal. Before concluding that the RAM is bad, the designer should check the system's cleanliness.

First, high-speed devices use extremely strong output drivers. An output can easily generate a 150-mA peak during switching. When driving a 100-pF load with a V_{SS} inductance on the order of 10 nH, the low output-level can easily bounce up to 0.8 V (see *Fig. 4*). With data-word lines of 16 or 32 bits, the V_{SS} line must be implemented with large-gauge wire.

The bouncing of V_{SS} not only degrades speed. It affects input-level specifications such as the input high- and low-levels V_{Ih}/V_{Il}. If the input to the device sits 200 mV above the trip point and the output driver bounces 400 mV below ground, the device suddenly sees an effective input voltage 200 mV below the trip point. Such a large amount of noise means that the input must be driven further to overcome the so-called V_{SS} feedback (see *Fig. 5*).

High-speed systems can be built, of course, but they require care. Reducing inductance is the first step. Inductance in power-supply lines causes anl I x L drop when large current surges occur. That is, the magnitude of the drop is L (di/dt). Thus, memory boards that were satisfactory for the last generation of RAMs may be inadequate for the latest super RAMs because of the larger current glitches made possible by strong output drivers. Clearly, power planes or gridding with ample bypass capacitor density are a necessity in the power-distribution design of today's high-speed memory systems.

To reduce the inductance of components, lead lengths should be trimmed appropriately on filter capacitors. Long leads interface with the filtering effect since a lead's series inductance increases the capacitor-to-power supply impedance.

Series inductance in an output lead is just as detrimental because it contributes to impedance mismatching with the signal transmission line. Mismatching causes the ringing of the output signal, and if the ringing is severe enough, it causes a false data transition to the next stage. Thus, the bottom line on high-speed memory system performance is that it is as dependent on careful board design as on fast memory access-time.

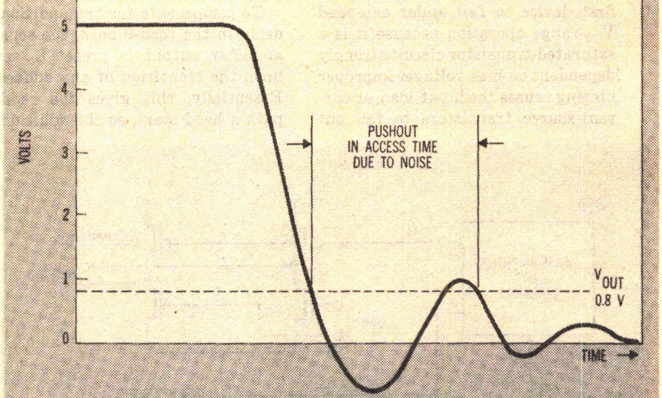


Fig. 4. The output drivers in a high-speed RAM such as the 51C67 generate high peak currents during switching. This can result in low-level output voltages as high as 0.8 V, especially when driving capacitive and inductive loads at high speeds.

Fast RAM applications

Since microprocessors operate at fixed clock rates, their data-fetch cycles consume a predetermined amount of time based on the clock rate. If the access time of external RAM is longer than a data-fetch cycle, wait states must be generated. Essentially, a wait state is wasted time since the processor cannot execute its current instruction without the data coming from the RAM. The end result is reduced system-level throughput.

One technique for decreasing the memory-access time delay is to use a fast intermediate memory—called a cache memory—located between the processor and the large main-storage memory. Caches are designed with extremely fast static RAMs that store blocks of data from main memory. Since static RAMs are faster than the dynamic RAMs that make up main memory, the processor can access data from the cache within its data-fetch cycle and thus eliminate time-consuming wait states.

Cache RAM is a system application that demands the highest speed RAMs. But the most stringent demands don't always come from end-user system designers. Most logic-system designers use microprocessor emulators to debug new applications. And the emulator itself demands the fastest static RAMs.

Emulators use RAMs for programmable control store, state machines, and capture memory. Each of these functions emulates the target microprocessor's internal functions. As

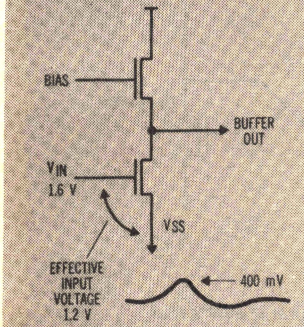


Fig. 5. When the V_{ss} line bounces (as shown in Fig. 4), it affects the high- and low-level voltage inputs to the RAM. Here an input voltage of 1.6 V is reduced significantly—to 1.2 V—by a 400-mV bounce in the V_{ss} line. Noise such as this effectively debiases the input, slowing down the throughput of the device.

such, they must be capable of running at the speed of the processor's internal clock rate.

The internal control memory must be faster than the external data memory since one external fetch cycle is equal to many internal control cycles. To make matters worse, an emulator is a board-level system that must operate at chip-level data speeds.

Another problem is writing to the RAM. One of the functions of an emulator is to trap and record blocks of data in real time. To do this, the RAM must be able to write as fast or faster than it can read.

RAM speed is the priority in high-performance systems, but dense chips—large storage capacity—are also desirable. In a cache memory, if the data block is small, there is little chance of having all the needed data within a single block. To maximize the "hit rate" (the probability of having the required data in the cache at the proper time), a large cache is necessary.

Emulators can also benefit from large memories. Circuits, such as a programmable control store, copy the functions of internal control ROMs, which are often large memories. And circuits such as the capture RAM determine how much status data can be recorded during a trapping operation. Traditionally, however, only small memories (1 to 4 Kbits) had sufficient speed to serve in these applications. Thus, there is a clear need for high-density, high-speed static RAMs.

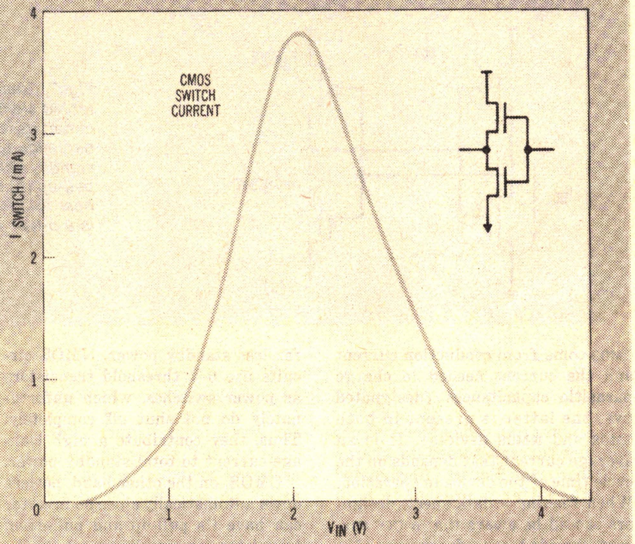


Fig. 6. One of the contributors to a CMOS RAM's power dissipation is simultaneous conduction current, which results when the CMOS complementing transistors are both partially on during switching. Reducing transition time reduces dissipation.

NMOS can't do the job

The principal difficulty with NMOS technology is that it is up against a power wall. As speed demands increase, more powerful transistors are required to charge external parasitic capacitances faster. The NMOS solution is transistor scaling—building a smaller and more powerful transistor. Scaling, therefore, puts a greater number of powerful transistors on a single chip. But the increased density means that the chip must dissipate more power per unit area, and the entire chip, therefore, must be capable of dissipating more power.

As a chip's dissipation increases, the limits of its package dissipation are reached. When this happens, the only alternative is to slow down the circuitry to reduce the power. As a result, the tradeoff in NMOS technology is to build slower devices to conserve power.

CMOS technology, on the other hand, has no such limitations. The CMOS advantage lies in its complementary pull-up and pull-down transistors. Since only one device is on at a time, DC power dissipation is extremely low. Using CMOS, it is possible to get the best of both worlds—very dense chips that can run at high speed.

The major power contributions in

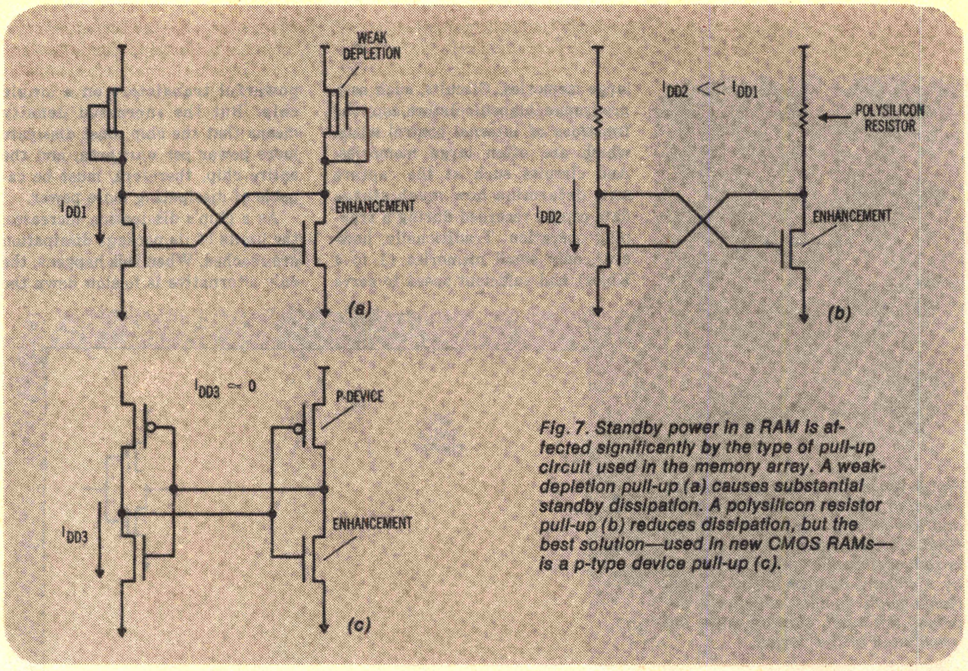


Fig. 7. Standby power in a RAM is affected significantly by the type of pull-up circuit used in the memory array. A weak-depletion pull-up (a) causes substantial standby dissipation. A polysilicon resistor pull-up (b) reduces dissipation, but the best solution—used in new CMOS RAMs—is a p-type device pull-up (c).

CMOS come from conduction current and the current needed to charge parasitic capacitances (designated CVF, the latter is present in both CMOS and NMOS devices). It is an average current that depends on the cycle time of the device in operation. When reading a data sheet, designers should be aware that a CVF current specified at a frequency of 1 MHz is meaningless if the device will actually cycle at 20 MHz.

Simultaneous conduction current (see *Fig. 6*) is switching current. In a CMOS inverter, both the pull-up and pull-down transistors are on for a brief time as the output switches.

High-speed CMOS devices may also have a DC component. The resultant DC power comes mostly from linear circuitry dissipation by non-CMOS devices such as differential sense-amplifiers, which are necessary in memory devices to achieve maximum performance, even at the expense of high power dissipation.

A major advantage of CMOS over NMOS RAMs is that CMOS dissipates far less standby power. NMOS circuits use 0-V threshold transistors as power switches, which unfortunately do not shut off completely. Thus, they contribute a high leakage-current to total standby power.

CMOS, on the other hand, powers down automatically since no inverter can have its pull-up and pull-down transistors on simultaneously in the DC case. In fact, CMOS linear-circuit leakage is reduced to almost zero by using ½-V threshold p- and n-type power-switching transistors.

A second source of standby power dissipation is in the memory array itself. Since a RAM cell is simply a set of cross-coupled inverters, the type of pull-up an inverter uses has a significant effect on standby power dissipation.

Some NMOS RAMs use a weak depletion-transistor as a pull-up (see *Fig. 7a*). The standby power is I_{pu} times the number of memory cells. For a 16-Kbit RAM having a weak-depletion drain current of 10 μA, the arrays contribution to standby current is 16 mA. Such a large current is far from optimum for a large memory array.

A resistor load is another type of pull-up (see *Fig. 7b*) in which lightly doped polysilicon forms the resistor. Resistor values as high as hundreds of megaohms can be fabricated with this technique, thereby substantially reducing array current. But the problem with polysilicon resistors is high sensitivity to noise, soft errors, and pull-down leakage. The biggest problem, however, is that the sensitivities are "soft" by nature. That is, they are all but impossible to identify in a production test environment.

CMOS offers another possibility—the p-type load (see *Fig. 7c*). A p-device is much stronger than either a resistor or weak-depletion pull-up. A strong p-device virtually eliminates soft sensitivities and draws no standby power. The resulting overall standby power is reduced to just a fraction of an equivalent NMOS chip's power. ☐

EPROMs (Erasable Programmable Read Only Memories)

4

2732A
32K (4K x 8) PRODUCTION AND UV ERASABLE PROMS

- **200 ns (2732A-2) Maximum Access Time . . . HMOS*-E Technology**
- **Compatible with High-Speed Microcontrollers and Microprocessors . . . Zero WAIT State**
- **Two Line Control**
- **10% V_{CC} Tolerance Available**
- **Low Current Requirement**
  - **—100 mA Active**
  - **—35 mA Standby**
- **int$_e$ligent Identifier™ Mode**
  - **—Automatic Programming Operation**
- **Industry Standard Pinout . . . JEDEC Approved 24 Pin Ceramic and Plastic Package**
  (See Packaging Spec. Order #231369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

The 2732A is currently available in two different package types. Cerdip packages provide flexibility in prototyping and R & D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments. Inventoried in the unprogrammed state, the P2732A is programmed quickly and efficiently when the need to change code arises. Costs incurred for new ROM masks or obsoleted ROM inventories are avoided. The tight package dimensional controls, inherent non-erasability, and high reliability of the P2732A make it the ideal component for these production applications.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE} = V_{IH}$) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.

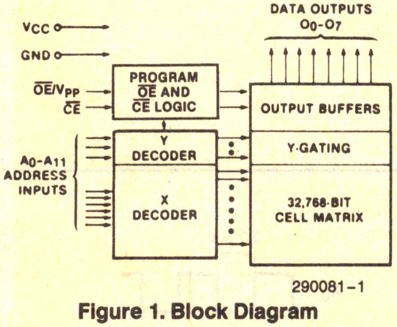
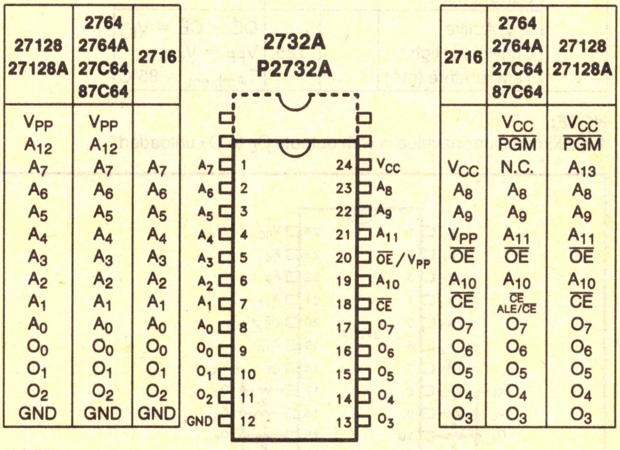


Figure 1. Block Diagram

Pin Names

A_0–A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$/V_{PP}	Output Enable/V_{PP}
O_0–O_7	Outputs



27128 27128A	2764 2764A 27C64 87C64	2716	2732A P2732A	Pin	Pin	2732A P2732A	2716	2764 2764A 27C64 87C64	27128 27128A
V_{PP}	V_{PP}							V_{CC}	V_{CC}
A_{12}	A_{12}							$\overline{PGM}$	$\overline{PGM}$
A_7	A_7	A_7	A_7	1	24	V_{CC}	V_{CC}	N.C.	A_{13}
A_6	A_6	A_6	A_6	2	23	A_8	A_8	A_8	A_8
A_5	A_5	A_5	A_5	3	22	A_9	A_9	A_9	A_9
A_4	A_4	A_4	A_4	4	21	A_{11}	V_{PP}	A_{11}	A_{11}
A_3	A_3	A_3	A_3	5	20	$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_2	A_2	A_2	A_2	6	19	A_{10}	A_{10}	A_{10}	A_{10}
A_1	A_1	A_1	A_1	7	18	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
A_0	A_0	A_0	A_0	8	17	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	9	16	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	10	15	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	11	14	O_4	O_4	O_4	O_4
GND	GND	GND	GND	12	13	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.
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October 1986
Order Number: 290081-002

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
$I_{CC_1}{}^{(1)}$	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:

1. Maximum current value is with outputs O_0 to O_7 unloaded.

EXPRESS EPROM PRODUCT FAMILY

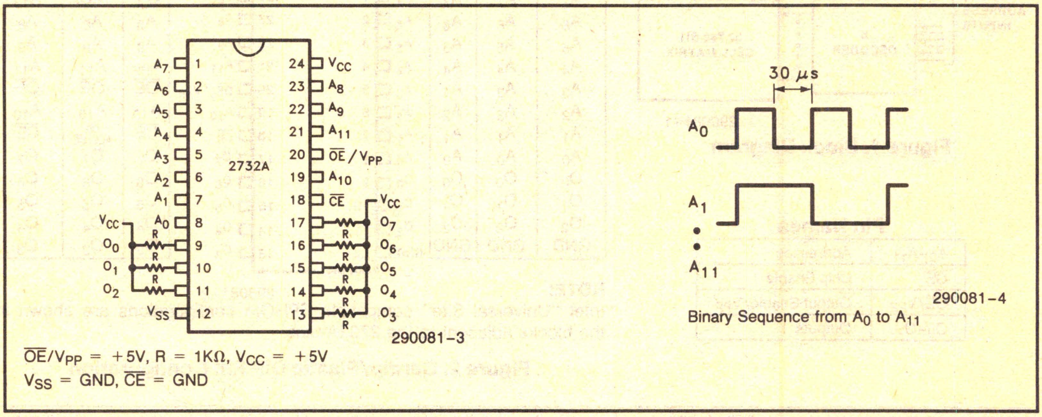
PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2732A Versions

Speed Versions	Packaging Options	
	Cerdip	Plastic
−2	Q	
STD	Q, T, L	
−3	Q	
−4	Q, T, L	
−20	Q	
−25	Q, T, L	
−30	Q	
−45	Q, T, L	



$\overline{OE}/V_{PP} = +5V$, $R = 1K\Omega$, $V_{CC} = +5V$
$V_{SS} = GND$, $\overline{CE} = GND$

Binary Sequence from A_0 to A_{11}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. During Read . . . . 0°C to +70°C
Temperature Under Bias . . . . −10°C to +80°C
Storage Temperature . . . . −65°C to +125°C
All Input or Output Voltages with
Respect to Ground . . . . −0.3V to +6V
Voltage on A9 with Respect
to Ground . . . . −0.3V to +13.5V
V_{PP} Supply Voltage with Respect to Ground
During Programming . . . . −0.3V to +22V
V_{CC} Supply Voltage with
Respect to Ground . . . . −0.3V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(2)	V_{CC} Current (Standby)			35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(2)	V_{CC} Current (Active)			100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \leq T_A \leq 70°C$

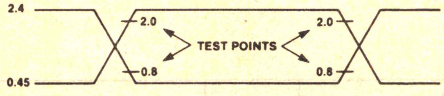
Versions	V_{CC} ±5%	2732A-2 P2732A-2		2732A P2732A		2732A-3 P2732A-3		2732A-4 P2732A-4		Units	Test Conditions
	V_{CC} ±10%	2732A-20		2732A-25		2732A-30		2732A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		70		100		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}/V_{PP}$ High to Output Float	0	60	0	60	0	130	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE (2) $T_A = 25°C, f = 1\ MHz$

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	$V_{IN} = 0V$
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

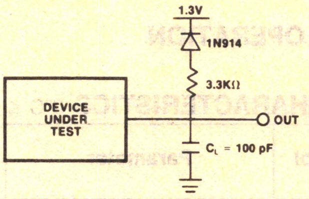
A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8

290081-5

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

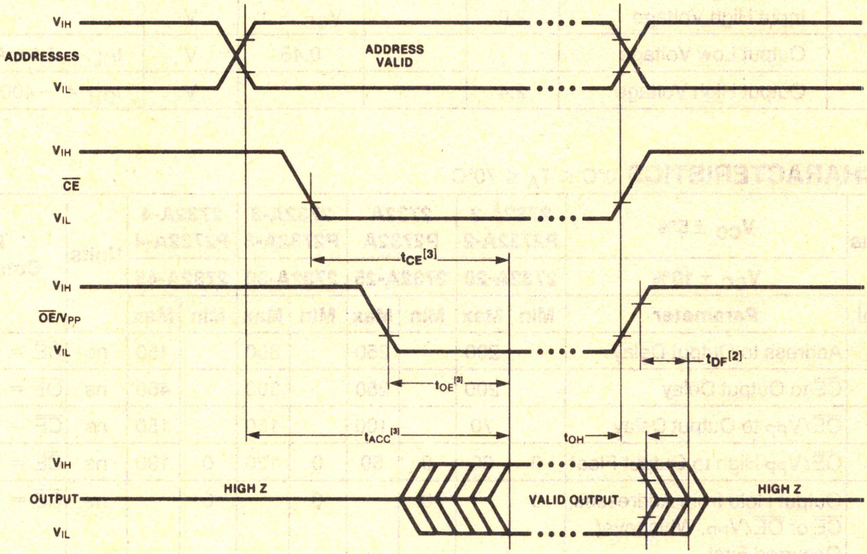
A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

290081-6

$C_L = 100\ pF$
C_L Includes Jig Capacitance

A.C. WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}[3]
V_{IH}
$\overline{OE}/V_{PP}$
V_{IL}
t_{DF}[2]
t_{OE}[3]
t_{ACC}[3]
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z

290081-7

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{CE}.

PLASTIC EPROM APPLICATIONS

Intel's P2732A is the result of a multi-year effort to make EPROMs more cost effective for production applications. The benefits of a plastic package enable the P2732A to be used for high volume production with lower profile boards and easier production assembly (no cover over UV transparent windows).

The reliability of plastic EPROMs is equivalent to traditional CERDIP packaging. The plastic is rugged and durable making it optimal for auto insertion and auto handling equipment. Design and testing ensures device programmability, data integrity, and impermeability to moisture.

Intel's Plastic EPROMs are designed for total compatibility with their CERDIP packaged predecessors. This encompasses quality, reliability, and programming. All Intel Plastic EPROMs have passed Intel's strict process and product reliability qualifications.

DEVICE OPERATION

The modes of operation of the 2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming and 12V on A_9 for the intₑligent Identifier™ mode. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read/Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	X	V_{CC}	High Z
Intₑligent Identifier(3)						
—Manufacturer	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	89H
—Device	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	01H

NOTES:

1. X can be V_{IH} or V_{IL}.
2. $V_H = 12V \pm 0.5V$.
3. $A_1-A_8, A_{10}, A_{11} = V_{IL}$.

Read Mode

The 2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum active current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) The lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's two-line control and by use of properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

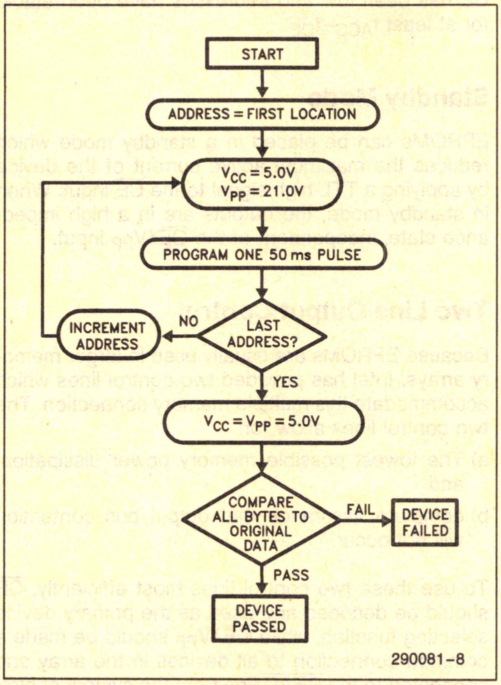


Figure 3. Standard Programming Flowchart

PROGRAMMING MODES

CAUTION: Exceeding 22V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure (cerdip EPROMs), all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" in cerdip EPROMs is by ultraviolet light erasure.

The device is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 µF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 20 ms (50 ms typical) active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed (see Figure 3). Any location can be programmed at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high level $\overline{CE}$ input inhibits the other EPROMs from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that selected device.

Program Verify

A verify (Read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_{e}$ligent Identifier™ Mode

The int$_{e}$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_{e}$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

Rob sullivan

A= 12 volts program

Not A = 21 volts

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming™ Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions (Note 1)
		Min	Typ(3)	Max		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC_2}(4)	V_{CC} Supply Current (Program and Verify)		85	100	mA	
I_{PP_2}(4)	V_{PP} Supply Current (Program)			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5		12.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions* (Note 1)
		Min	Typ(3)	Max		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Not Driven	0		130	ns	(Note 2)
t_{PW}	$\overline{CE}$ Pulse Width During Programming	20	50	55	ms	
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{IL}$
t_{VR}	V_{PP} Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

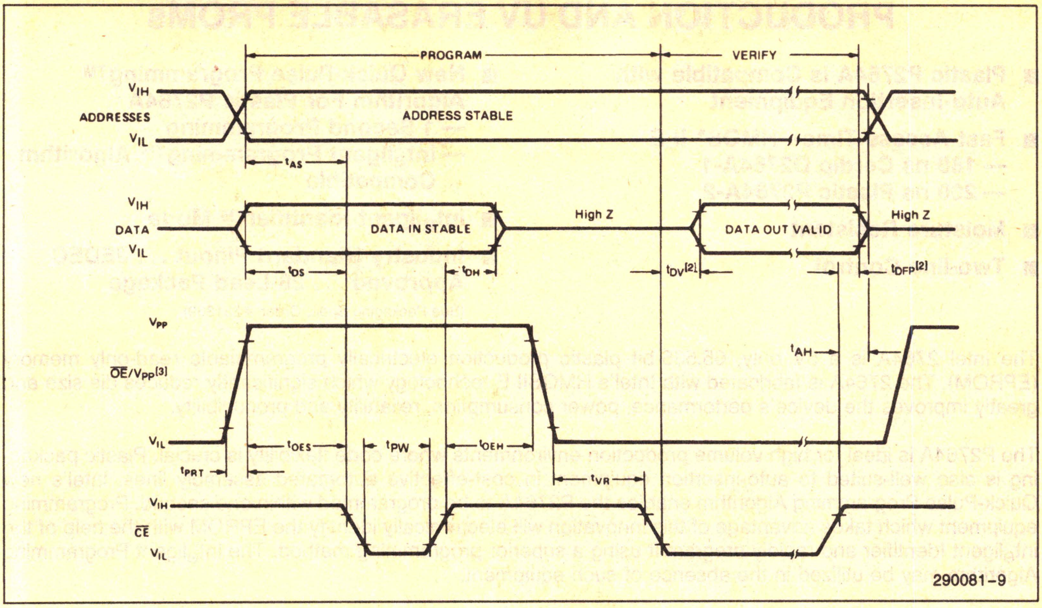
NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

*A.C. TEST CONDITIONS

Input Rise and Fall Time (10% to 90%) . . . . . ≤20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
VIH
ADDRESSES
VIL
ADDRESS STABLE
tAS
VIH
DATA
VIL
DATA IN STABLE
High Z
DATA OUT VALID
High Z
tDS
tOH
tDV[2]
tDFP[2]
VPP
OE/VPP[3]
tAH
VIL
tOES
tPW
tOEH
tPRT
tVR
VIH
CE
VIL

290081-9

NOTES:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

2764A
ADVANCED 64K (8K x 8) PRODUCTION AND UV ERASABLE PROMs

- **Plastic P2764A is Compatible with Auto-Insertion Equipment**
- **Fast Access Time—HMOS* II E**
  - **— 180 ns Cerdip D2764A-1**
  - **— 200 ns Plastic P2764A-2**
- **Moisture Resistant**
- **Two-line Control**
- **New Quick-Pulse Programming™ Algorithm For Plastic P2764A**
  - **— 1 Second Programming**
  - **— int$_{e}$ligent Programming™ Algorithm Compatible**
- **int$_{e}$ligent Identifier™ Mode**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Package**
  (See Packaging Spec, Order #231369)

The Intel 2764A is a 5V only, 65,536-bit plastic production electrically programmable read-only memory (EPROM). The 2764A is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, power consumption, reliability and producibility.

The P2764A is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P2764A to be programmed within one second. Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_{e}$ligent Identifier and rapidly program it using a superior programming method. The int$_{e}$ligent Programming Algorithm may be utilized in the absence of such equipment.

The 2764A provides access times to 180 ns (2764A-1). This is compatible with high-performance microprocessors, such as Intel's 8 MHz iAPX 186 allowing full speed operation without the addition of WAIT states. The 2764A is also directly compatible with the 12 MHz 8051 family.

Two-line control and JEDEC-approved, 28 pin packaging are standard features of all Intel higher density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between non-volatile memory alternatives.

*HMOS is a patented process of Intel Corporation.

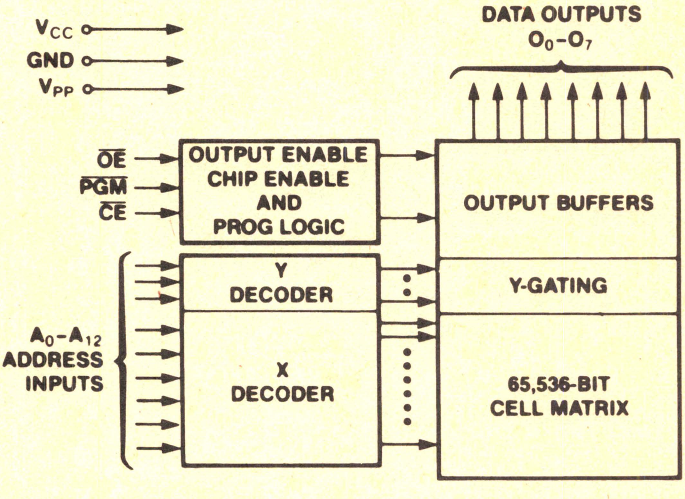


Figure 1. Block Diagram

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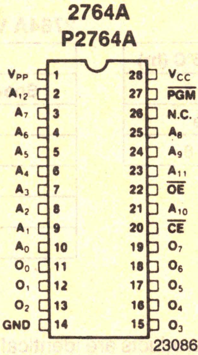
October 1985
Order Number: 230864-004

Pin Names

$A_0–A_{12}$	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$O_0–O_7$	Outputs
$\overline{PGM}$	Program
N.C.	No Connect
D.U.	Don't Use

27916	27513	27512	27256	27128A	2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	I/O_0	O_0	O_0	O_0	O_0	O_0
O_1	I/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd


2764A
P2764A
VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
28 VCC
27 PGM
26 N.C.
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3

2716	2732A	27128A 27664	27256	27512	27513	27916
		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}	$\overline{WE}$	$\overline{PGM}/\overline{WE}$
V_{CC}	V_{CC}	A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

230864-2

NOTE:
Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P2764A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2764A VERSIONS

	Packaging Options	
Speed Versions	Cerdip	Plastic
−2	Q	
STD	Q, T, L	T
−3	Q, T, L	T
−25	Q, T, L	T
−30	Q, T, L	

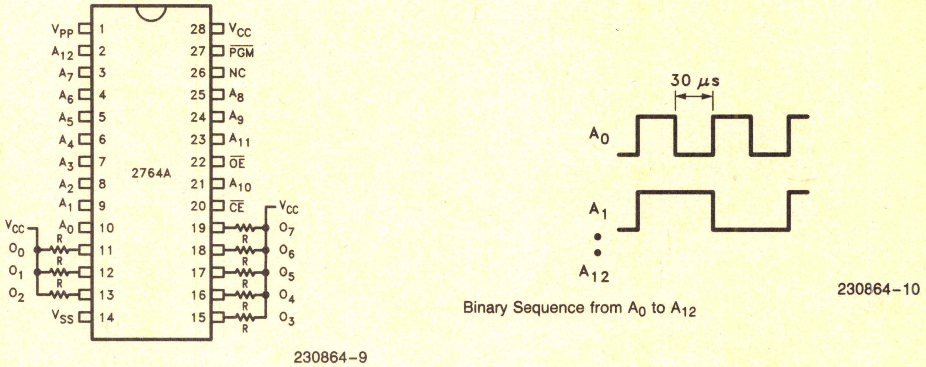
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2764A LD2764A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		40	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		75	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
11
12
13
VSS 14
28 VCC
27 PGM
26 NC
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3
2764A
VCC
O0
O1
O2
R
230864-9
30 µs
A0
A1
A12
Binary Sequence from A0 to A12
230864-10

$\overline{OE}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V V_{SS} = GND $\overline{CE}$ = GND
PGM = +5V

Burn-in Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .... 0°C to +70°C
Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Inputs or Output Voltages with
Respect to Ground .... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground .... −0.6V to +13.5V
V_{PP} Supply Voltage with
Respect to Ground
During Programming .... −0.6V to +14.0V
V_{CC} Supply Voltage with Respect
to Ground .... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Symbol	Parameter	Limits			Conditions
		Min	Max	Unit	
I_{LI}	Input Load Current		10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 5.5V
I_{PP}(2)	V_{PP} Current Read		5	mA	V_{PP} = 5.5V
I_{SB}	V_{CC} Current Standby		35	mA	$\overline{CE} = V_{IH}$
I_{CC}(2)	V_{CC} Current Active		75	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
V_{PP}(2)	V_{PP} Read Voltage	3.8	V_{CC}	V	V_{CC} = 5.0V ± 0.25V

A.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Versions(4)	V_{CC} ± 5%	2764A-1		2764A-2 P2764A-2		2764A P2764A		2764A-3 P2764A-3		2764A-4		Unit	Test Conditions
	V_{CC} ± 10%			2764A-20		2764A-25 P2764A-25		2764A-30 P2764A-30		2764A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		180		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		180		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		65		75		100		120		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	55	0	55	0	60	0	105	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

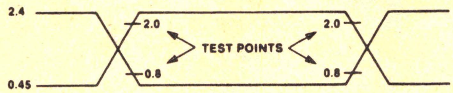
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. Model Number Prefixes: No prefix = CERDIP; P = Plastic DIP.

CAPACITANCE[2] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ [1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

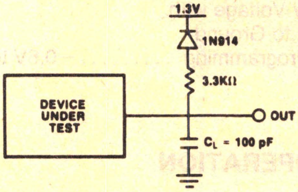
A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8

230864-3

A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

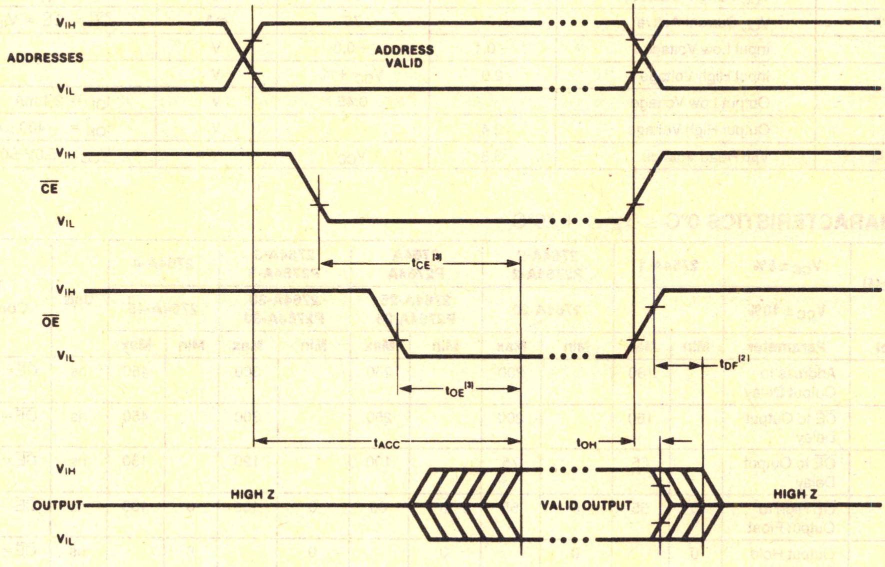
A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

230864-4

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE} [3]
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} [2]
t_{OE} [3]
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
V_{IL}

230864-5

NOTES:

1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 2764A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A_9 for int$_e$ligent identifier mode.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	High Z
int$_e$ligent Identifier(3) —manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89H(5) 88H(5)
—device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	08H

NOTES:

1. X can be V_{IH} or V_{IL}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1–A_8, A_{10}–A_{12} = V_{IL}.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturers identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

Read Mode

The 2764A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage (see Table 2) will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int_eligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C±5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1(A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The EPROM should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the EPROM to high intensity UV light for longer periods may cause permanent damage.

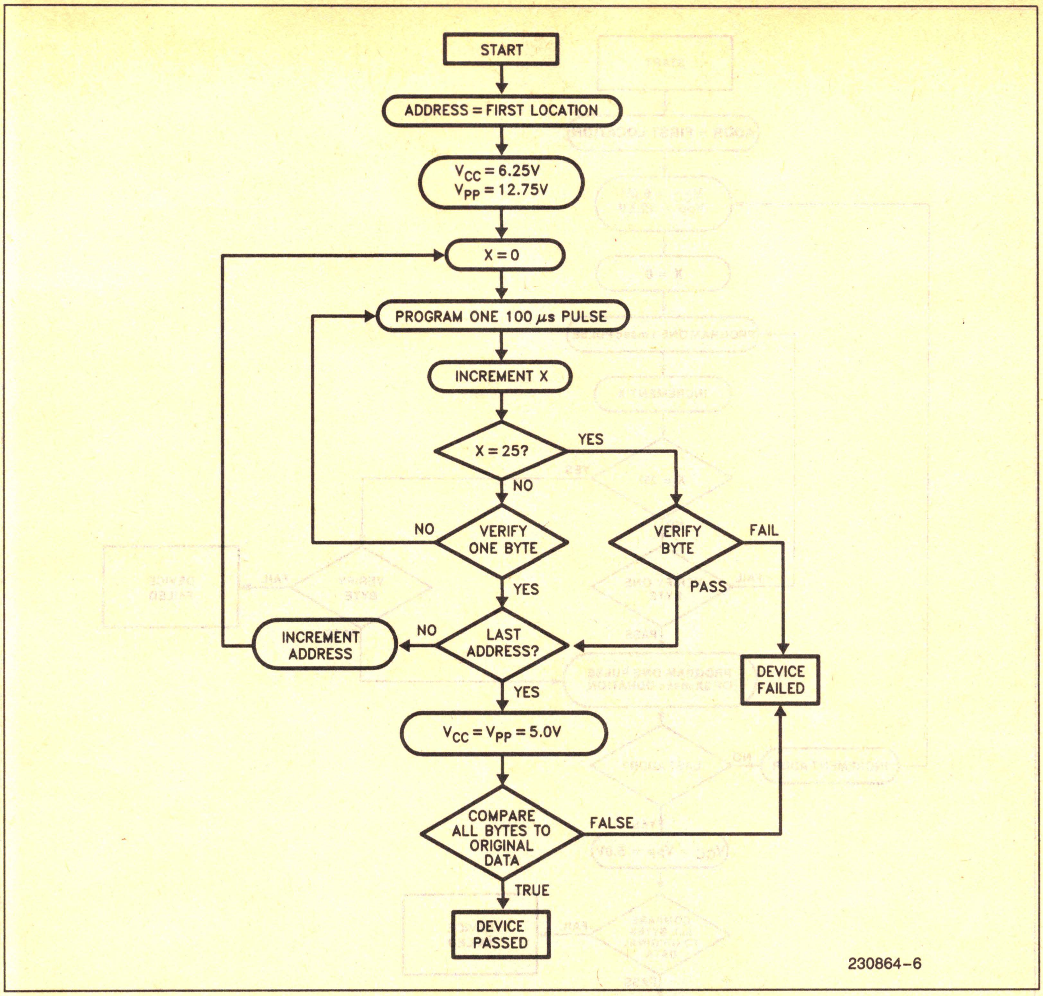

START
ADDRESS = FIRST LOCATION
VCC = 6.25V
VPP = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
NO
YES
VERIFY BYTE
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FALSE
TRUE
DEVICE PASSED
230864-6

Figure 3. Quick-Pulse Programming™ Flowchart

Quick-Pulse Programming™ Algorithm (Plastic P2764A)

Intel's Plastic and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic P2764A devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25–100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic and PLCC EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

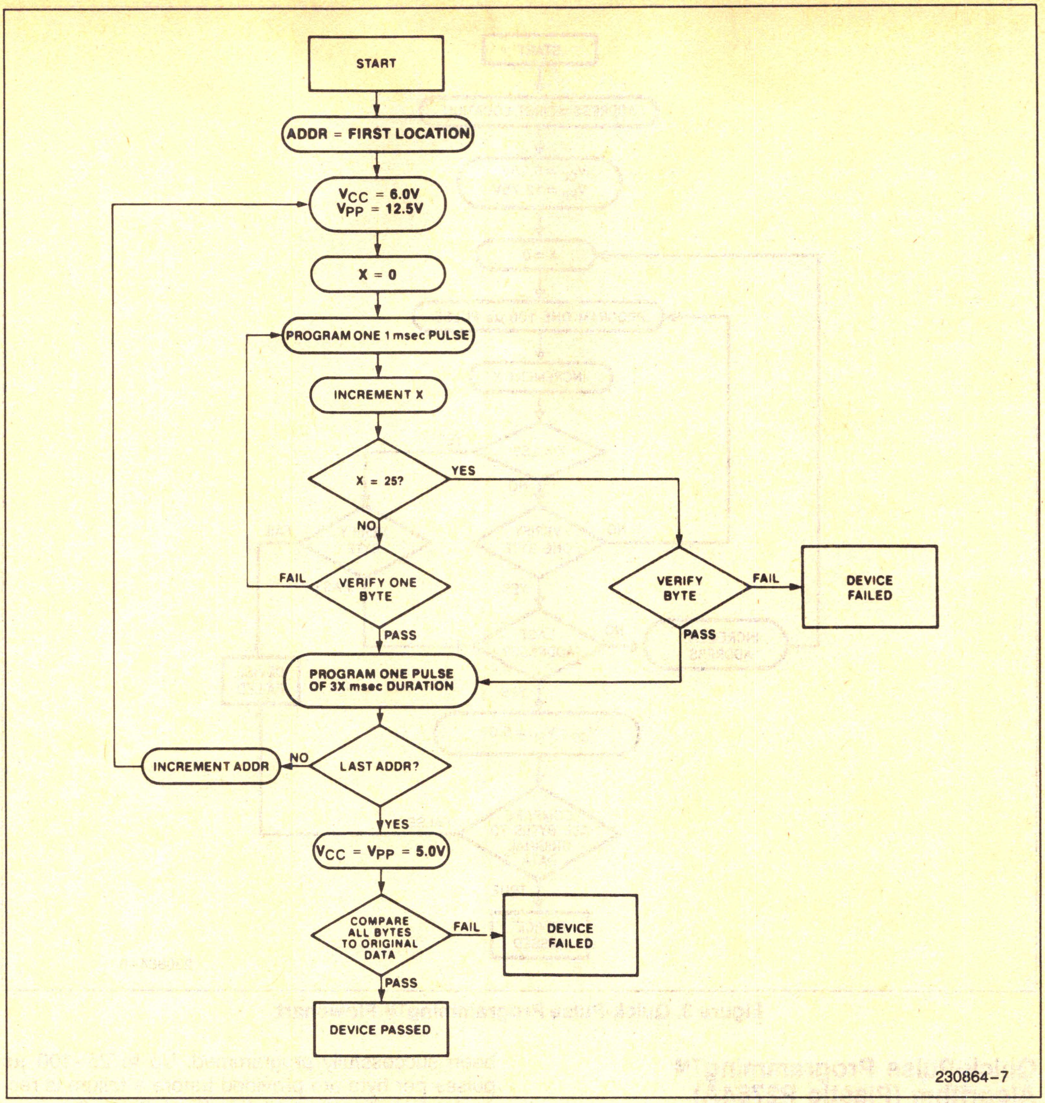

START
ADDR = FIRST LOCATION
VCC = 6.0V
VPP = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
230864-7

Figure 4. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, is required for all of Intel's 12.5V CERDEP EPROMs. Plastic and PLCC EPROMs may also be programmed using this method. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

Table 2

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\ \mu$A
$I_{CC2}^{(4)}$	V_{CC} Supply Current (Program & Verify)		75	mA	
$I_{PP2}^{(4)}$	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

Symbol	Parameter	Limits				Test Conditions* (see Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(see Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) .... 20 ns

Input Pulse Levels .... 0.45V to 2.4V

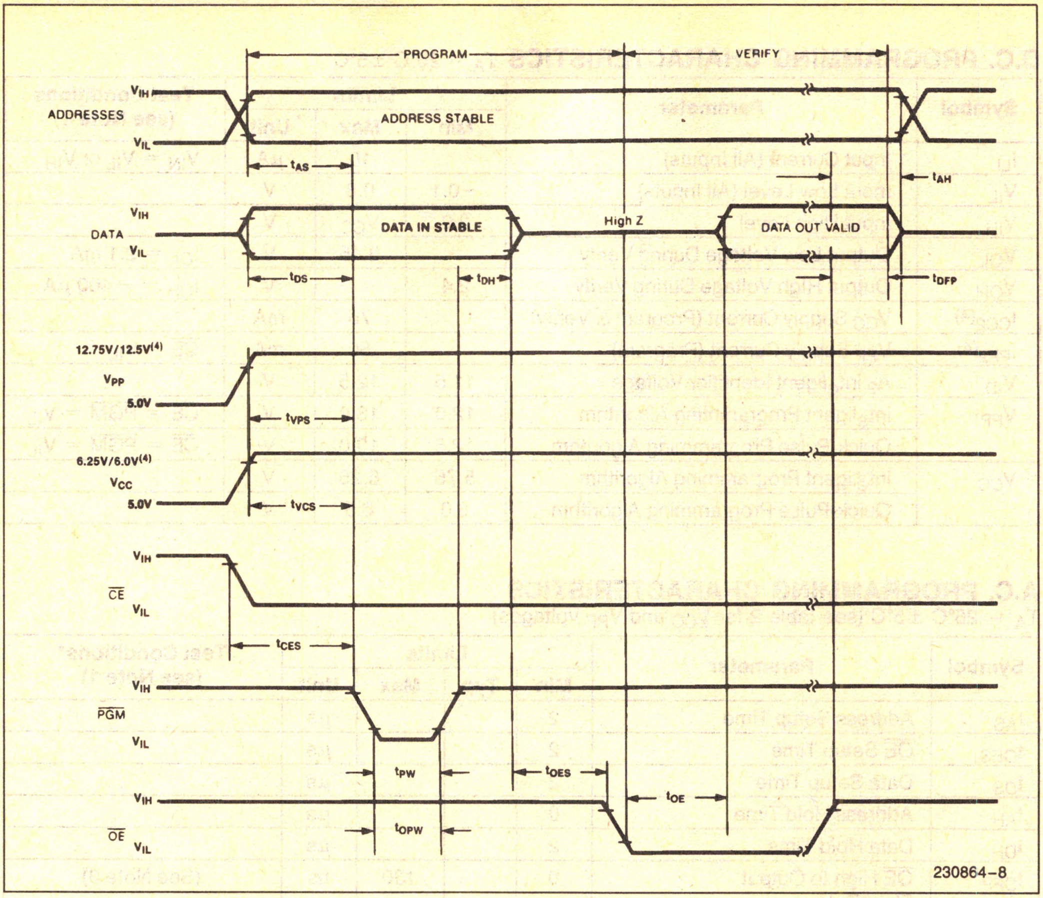
Input Timing Reference Level .... 0.8V and 2.0V

Output Timing Reference Level ...... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (int$_e$ligent Programming Algorithm only).
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with Outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
V_{IH}
DATA
V_{IL}
DATA IN STABLE
High Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
12.75V/12.5V(4)
V_{PP}
5.0V
t_{VPS}
6.25V/6.0V(4)
V_{CC}
5.0V
t_{VCS}
V_{IH}
$\overline{CE}$
V_{IL}
t_{CES}
V_{IH}
$\overline{PGM}$
V_{IL}
t_{PW}
t_{OES}
t_{OE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{OPW}
230864-8

NOTES:

1. The input timing reference level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2764A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for Int$_{e}$ligent Programming Algorithm.

27C64/87C64
64K (8K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **CHMOS Microcontroller and Microprocessor Compatible**
  - **87C64-Integrated Address Latch**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **High Performance Speeds**
  - **150 ns Maximum Access Time**
- **New Quick-Pulse Programming™ Algorithm (1 second programming)**
  - **Use with Plastic DIP and PLCC EPROMs**
- **Available in 28-Pin Cerdip and Plastic DIP Package and 32-Lead PLCC Package.**

  (See Packaging Spec, Order #231369)

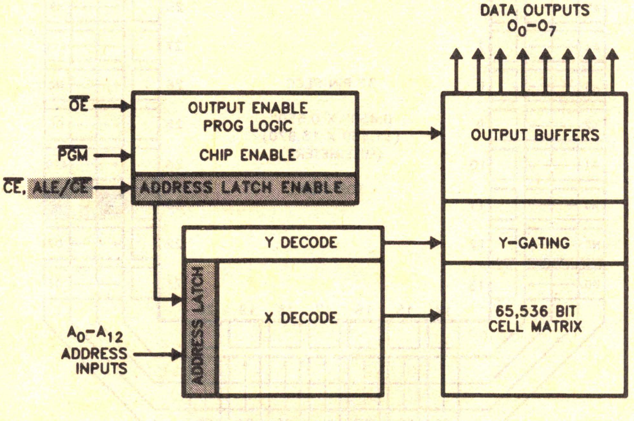
Intel's 27C64 and 87C64 CHMOS EPROMs are 64K bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 2764A (HMOS II-E).

The 27C64 and 87C64 are offered in both a ceramic DIP, Plastic DIP, and Plastic Leaded Chip Carrier (PLCC) Packages. Cerdip packages provide flexibility in prototyping and R&D environments, whereas Plastic DIP and PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming™ Algorithm is employed on Plastic DIP and PLCC devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse compatible programming equipment and with Cerdip devices, the int$_e$ligent Programming Algorithm may be utilized.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate an external address latch by tieing address and data pins of the 87C64 directy to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs (A_0–A_{12}) of the 87C64 is latched internally. The address inputs are then ignored as data information is passed on the same bus.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.



Shaded Areas ▨ represent the 87C64 version

290000-1

Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

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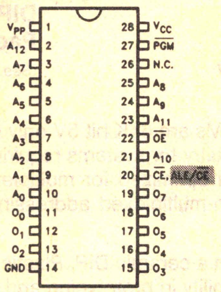
Pin Names

A_0-A_{12}	ADDRESSES
O_0-O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/$\overline{CE}$	ADDRESS LATCH ENABLE /CHIP ENABLE
$\overline{PGM}$	PROGRAM STROBE
N.C.	NO CONNECT
D.U.	DON'T USE

27256	27128	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

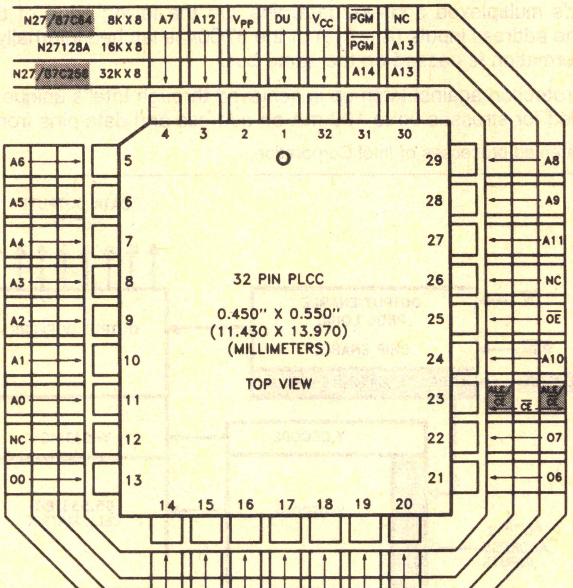

27C64/87C64
P27C64/P87C64
V_{PP} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}$
26 N.C.
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$
21 A_{10}
20 $\overline{CE}$, ALE/$\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

2716	2732A	27128	27256
		V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}
V_{CC}	V_{CC}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

290000-2

NOTE:
Intel "Universal Site" Compatible EPROM Pin Configurations are shown in the adjacent blocks to 27C64 Pins.
Shaded Areas ▨ represent the 87C64 version

Figure 2. Pin Configuration


N27/87C64 8K X 8
N27128A 16K X 8
N27/87C256 32K X 8
A7
A12
V_{PP}
DU
V_{CC}
$\overline{PGM}$
NC
$\overline{PGM}$
A13
A14
A13
4
3
2
1
32
31
30
A6
A5
A4
A3
A2
A1
A0
NC
O0
5
6
7
8
9
10
11
12
13
29
28
27
26
25
24
23
22
21
A8
A9
A11
NC
$\overline{OE}$
A10
ALE/$\overline{CE}$
$\overline{CE}$
ALE/$\overline{CE}$
O7
O6
32 PIN PLCC
0.450" X 0.550"
(11.430 X 13.970)
(MILLIMETERS)
TOP VIEW
14
15
16
17
18
19
20
O1
O2
GND
DU
O3
O4
O5

290000-11

Figure 3. PLCC(N) Lead Configuration

Extended Temperature (Express) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications.

EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0 to +70	168 ±8
T	−40 to +85	NONE
L	−40 to +85	168 ±8
A	−40 to +125	NONE
B	−40 to +125	168 ±8

EXPRESS Options

27C64/87C64 Versions

	Packaging Options		
Speed Versions	Cerdip	PLCC	Plastic DIP
−1	T, L, Q	T	T
−15	T, L, Q	T	T
−2	T, L, Q, A, B	T, A	T, A
−20	T, L, Q, A	T	T
−STD	T, L, Q, A, B	T, A	T, A
−25	T, L, Q, A	T	T
−3	T, L, Q, A, B	T, A	T, A
−30	T, L, Q, A	T	T

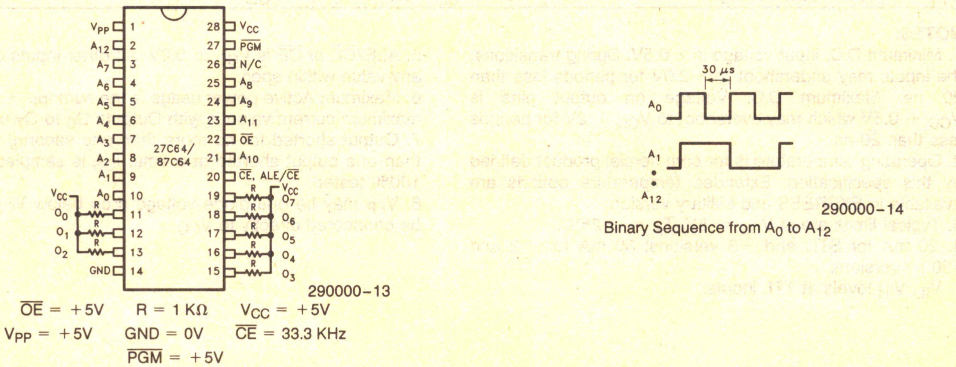
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter		27C64 87C64 Min	27C64 87C64 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)	CMOS		0.1	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
		TTL		1.0	
I_{CC_1}(1)	V_{CC} Active Current (mA)	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{ambient} = 85°C$

NOTE:
1. See notes 4 and 6 of Read Operation D.C. Characteristics.



290000-13

$\overline{OE}$ = +5V   R = 1 KΩ V_{CC} = +5V

V_{PP} = +5V   GND = 0V $\overline{CE}$ = 33.3 KHz

$\overline{PGM}$ = +5V

290000-14

Binary Sequence from A_0 to A_{12}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ....0°C to +70°C(2)

Temperature Under Bias ....−10°C to +80°C

Storage Temperature ....−65°C to +150°C

Voltage on Any Pin with
Respect to Ground ....−2.0V to 7V(1)

Voltage on Pin A_9 with
Respect to Ground ....−2.0V to +13.5V(1)

V_{PP} Supply Voltage with Respect to Ground
During Programming ....−2.0V to +14V(1)

V_{CC} Supply Voltage with
Respect to Ground ....−2.0V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter		Notes	Min	Typ(3)	Max	Unit	Test Condition
I_{LI}	Input Leakage Current				0.01	1.0	μA	$V_{IN} = V_{CC} = 5.5V$
I_{LO}	Output Leakage Current				0.01	1.0	μA	$V_{OUT} = V_{CC} = 5.5V$
I_{PP_1}	V_{PP} Current Read		6			100	μA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby with Inputs—	CMOS	5			100	μA	$\overline{CE} = V_{IH}$
		TTL	4			1.0	mA	
I_{CC_1}	V_{CC} Current Active		4, 6			20, 30	mA	$\overline{CE} = V_{IL}$ f = 5 MHz, $I_{OUT} = 0$ mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage(±10% Supply) (TTL)			2.0		$V_{CC}+0.5$	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			$V_{CC}-0.2$		$V_{CC}+0.2$		
V_{OL}	Output Low Voltage					0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage			3.5			V	$I_{OH} = -2.5$ mA
I_{OS}	Output Short Circuit Current		7	100			mA	
V_{PP}	V_{PP} Read Voltage		8	$V_{CC}-0.7$		V_{CC}	V	

NOTES:

1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. Voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. 20 mA for STD and −3 versions; 30 mA for −2 and 150 ns versions.
   V_{IL}, V_{IH} levels at TTL inputs.
5. ALE/$\overline{CE}$ or $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O_0 to O_7 unloaded.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

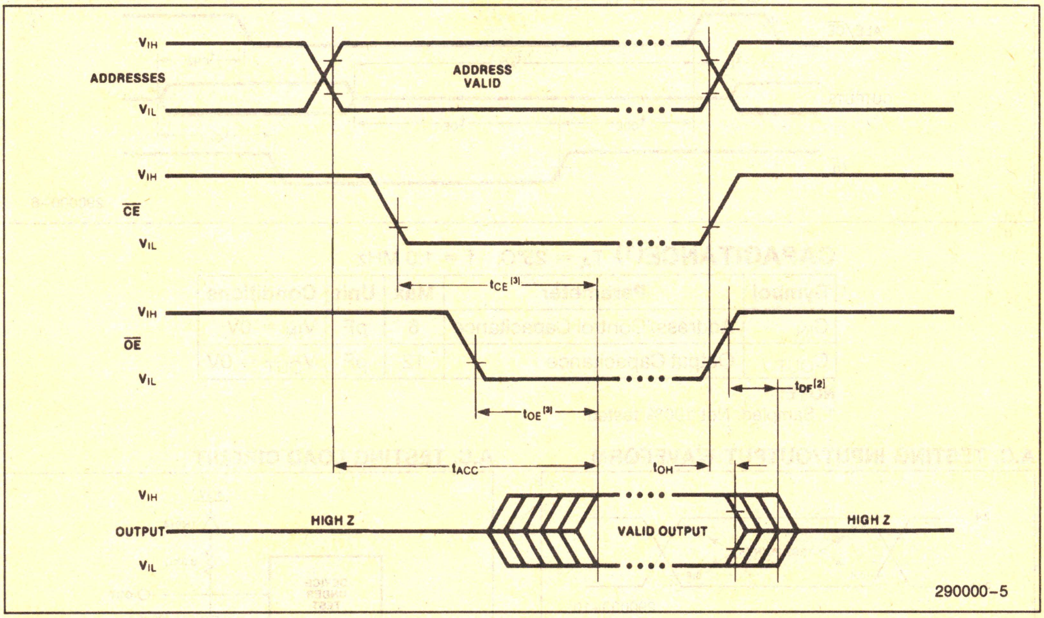
READ OPERATION

A.C. CHARACTERISTICS 27C64(1) 0°C ≤ T_A ≤ +70°C

Versions (3)	V_{CC} ±5%	27C64-1 N27C64-1 P27C64-1		27C64-2 N27C64-2 P27C64-2		27C64 N27C64		27C64-3 N27C64-3		Unit
	V_{CC} ±10%	27C64-15 N27C64-15 P27C64-15		27C64-20 N27C64-20 P27C64-20		27C64-25 N27C64-25		27C64-30 N27C64-30		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		75		100		120	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z		35		55		60		105	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V.
   Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 27C64


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE (3)
VIH
OE
VIL
tDF (2)
tOE (3)
tACC
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
290000-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

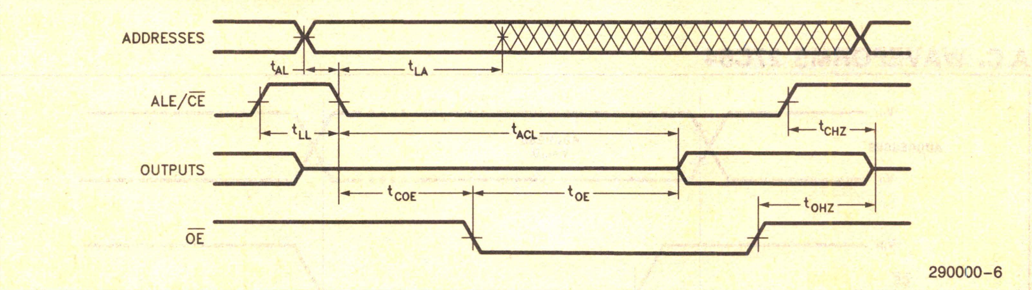
A.C. CHARACTERISTICS 87C64[1] 0°C ≤ T_A ≤ +70°C

Versions (3)	V_{CC} ±5%	87C64-1 N87C64-1 P87C64-1		87C64-2 N87C64-2 P87C64-2		87C64 N87C64		87C64-3 N87C64-3		Unit
	V_{CC} ±10%	87C64-15 N87C64-15 P87C64-15		87C64-20 N87C64-20 P87C64-20		87C64-25 N87C64-25		87C64-30 N87C64-30		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LL}	Chip Deselect Width	50		50		60		75		ns
t_{AL}	Address to $\overline{CE}$-Latch Set-up	7		20		25		30		ns
t_{LA}	Address Hold from $\overline{CE}$-LATCH	30		45		50		60		ns
t_{ACL}	CE-Latch Access Time		150		200		250		300	ns
t_{OE}	Output Enable to Output Valid		75		75		100		120	ns
t_{COE}	ALE/$\overline{CE}$ to Output Enable	30		45		50		60		ns
t_{CHZ}(2)	Chip Deselect to Output in High Z		45		50		60		75	ns
t_{OHZ}(2)	Output Disable to Output in High Z		35		50		60		75	ns

NOTES:

1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 87C64


ADDRESSES
t_{AL}
t_{LA}
ALE/$\overline{CE}$
t_{LL}
t_{ACL}
t_{CHZ}
OUTPUTS
t_{COE}
t_{OE}
t_{OHZ}
$\overline{OE}$

290000-6

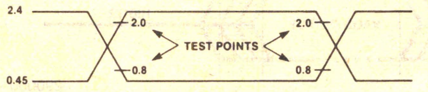
CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:

1. Sampled. Not 100% tested.

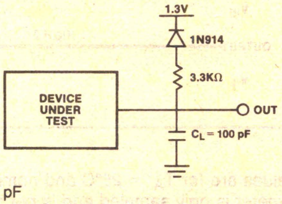
A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8

290000-10

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

290000-3

C_L = 100 pF

C_L Includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C64/87C64 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier mode.

Table 1. Mode Selection for 27C64 and 87C64

Mode \ Pins	ALE/$\overline{CE}$ $\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (7)	A_9	A_0	V_{PP} (7)	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	HIGH Z
inteligent Identifier(3) -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H (6) 88 H (6)
inteligent Identifier(3) -27C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	07 H
inteligent Identifier(3, 5) -87C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:

1. X can be V_{IL} or V_{IH}.
2. $V_H = 12.0V \pm 0.5V$.
3. $A_1 - A_8$, $A_{10-12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.
6. The Manufacturer's identifier reads 89H for Cerdip devices; 88H for Plastic DIP and PLCC devices.
7. In Read Mode tie $\overline{PGM}$ and V_{PP} to V_{CC}.

Read Mode: 27C64

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Read Mode: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C64. All address inputs of the 87C64 are latched when ALE/$\overline{CE}$ is brought low, thus eliminating the need for a separate address latch.

The 87C64 internal address latch is directly enabled through the use of the ALE/$\overline{\text{CE}}$ line. As the transition occurs on the ALE/$\overline{\text{CE}}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM by the $\overline{\text{OE}}$ pin.

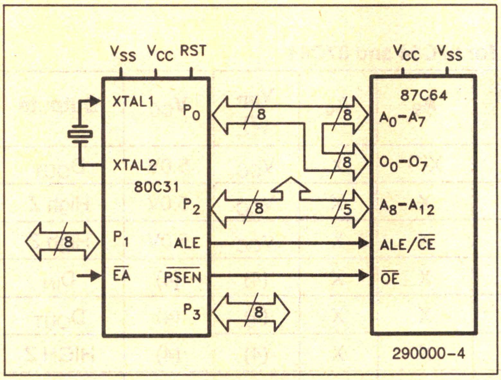


Figure 4. 80C31 with 87C64 System Configuration

Standby Mode

The 27C64 and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100 μA. Both are placed in the Standby mode when $\overline{\text{CE}}$ or ALE/$\overline{\text{CE}}$ are in the CMOS-high state. When in the Standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{\text{CE}}$ (or ALE/$\overline{\text{CE}}$) should be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{\text{CE}}$ (or ALE/$\overline{\text{CE}}$) and $\overline{\text{PGM}}$ are both at TTL low and $\overline{\text{OE}}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{\text{CE}}$ (or ALE/$\overline{\text{CE}}$) or $\overline{\text{PGM}}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$ (or ALE/$\overline{CE}$), all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ (or ALE/$\overline{CE}$) = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ (or ALE/$\overline{CE}$) at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1. ALE/$\overline{CE}$ of the 87C64 has to be toggled in order to latch in the addresses and read the Signature Codes.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from $-1V$ to $V_{CC} + 1V$.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

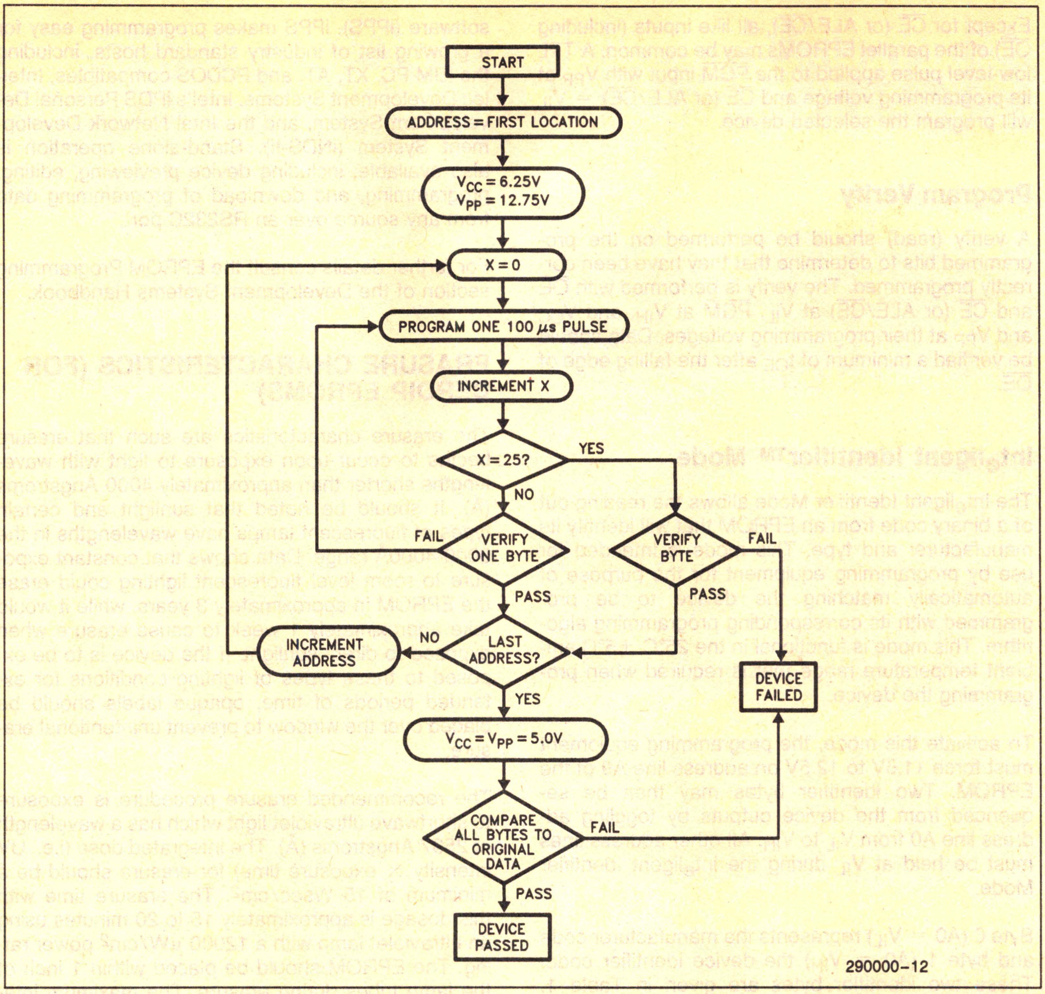

START
ADDRESS = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
FAIL
PASS
VERIFY BYTE
FAIL
PASS
LAST ADDRESS?
NO
INCREMENT ADDRESS
YES
DEVICE FAILED
V_{CC} = V_{PP} = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
290000-12

Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (for Plastic DIP and PLCC EPROMs)

Intel's Plastic DIP and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production environment. This algorithm allows these devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, 27C64/87C64 EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

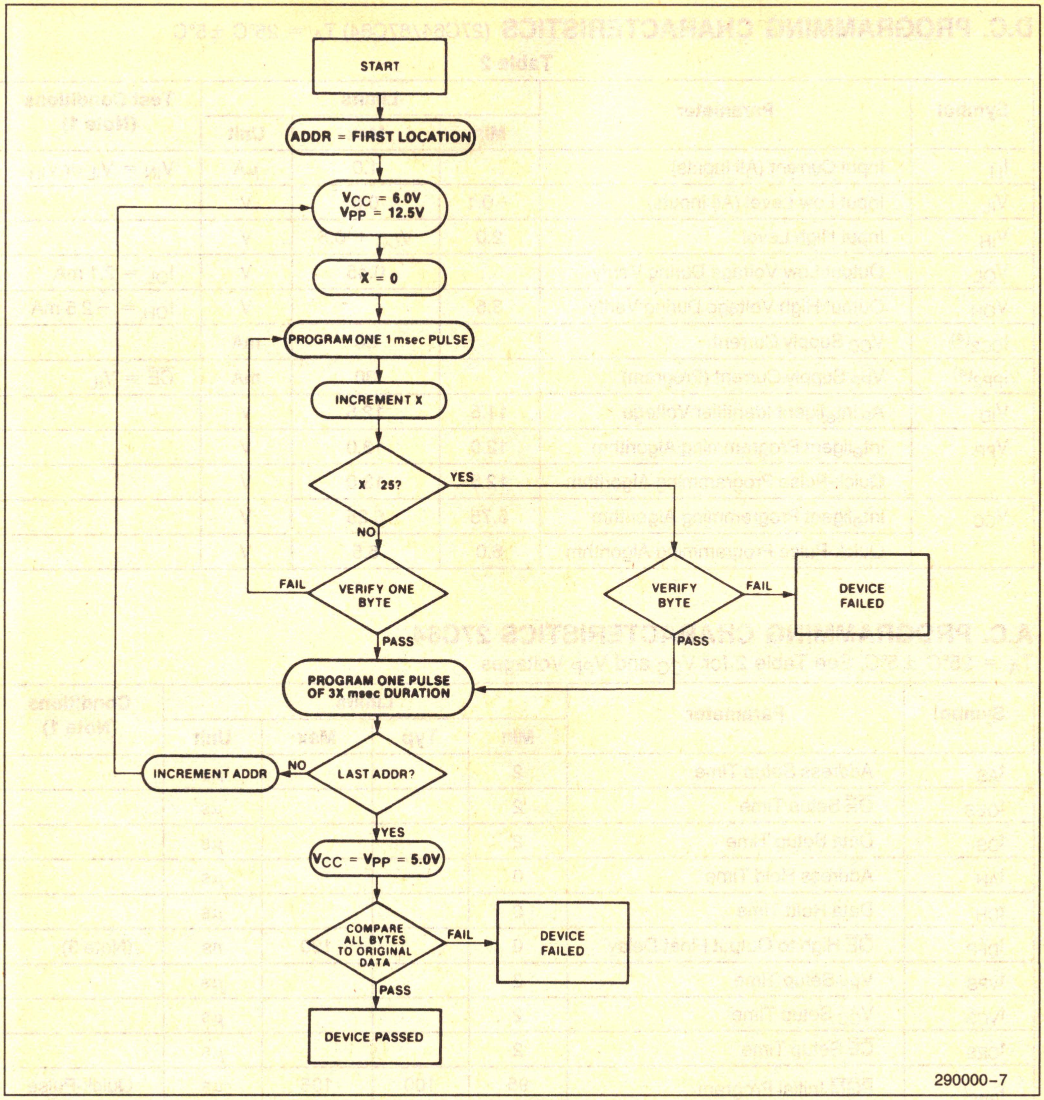

START
ADDR = FIRST LOCATION
VCC = 6.0V
VPP = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
290000-7

Figure 6. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 6.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS (27C64/87C64) $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 27C64

$T_A = 25°C \pm 5°C$, See Table 2 for V_{CC} and V_{PP} Voltages

Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse
		0.95	1.0	1.05	ms	int$_e$ligent
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

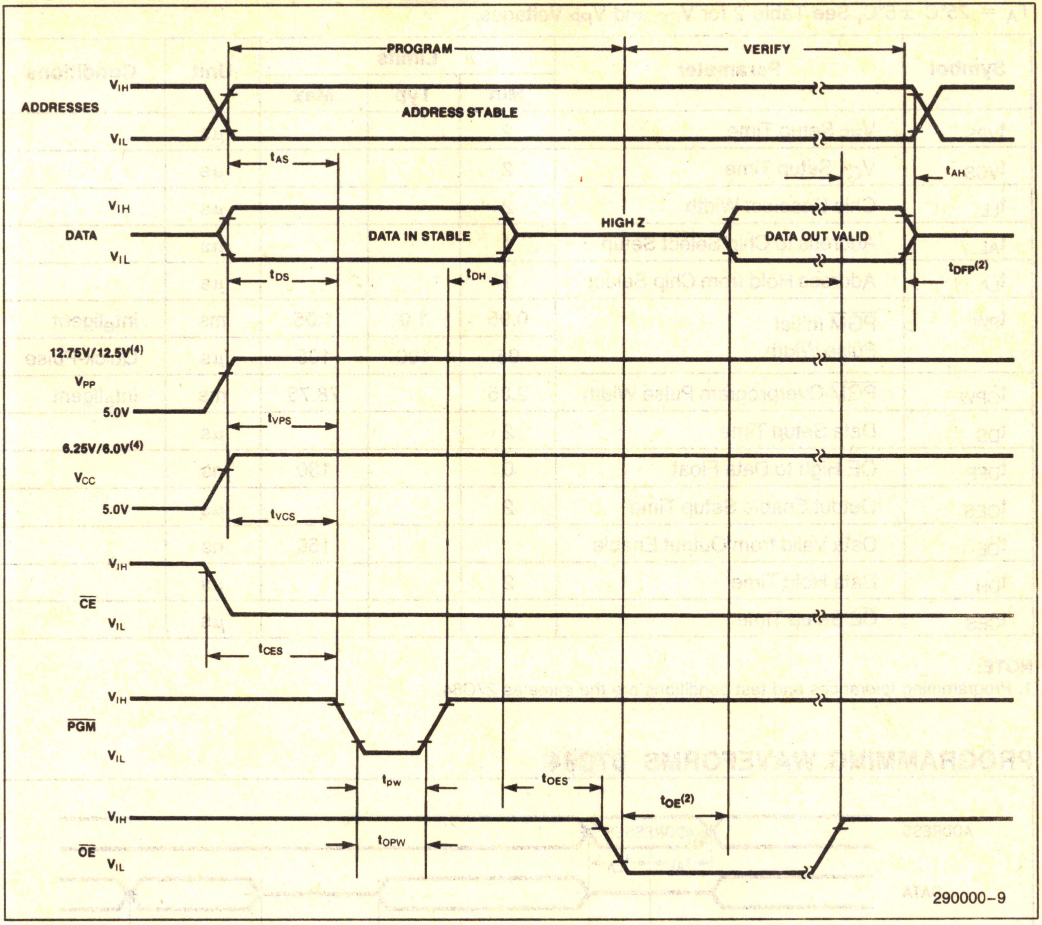
A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 3.5V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 Unloaded.

PROGRAMMING WAVEFORMS 27C64


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
V_{IH}
V_{IL}
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}(2)
12.75V/12.5V(4)
V_{PP}
5.0V
t_{VPS}
6.25V/6.0V(4)
V_{CC}
5.0V
t_{VCS}
CE
V_{IH}
V_{IL}
t_{CES}
PGM
V_{IH}
V_{IL}
t_{PW}
t_{OES}
t_{OE}(2)
OE
V_{IH}
V_{IL}
t_{OPW}

290000-9

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP}/6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP}/6.0V V_{CC} for inteligent Programming Algorithm.

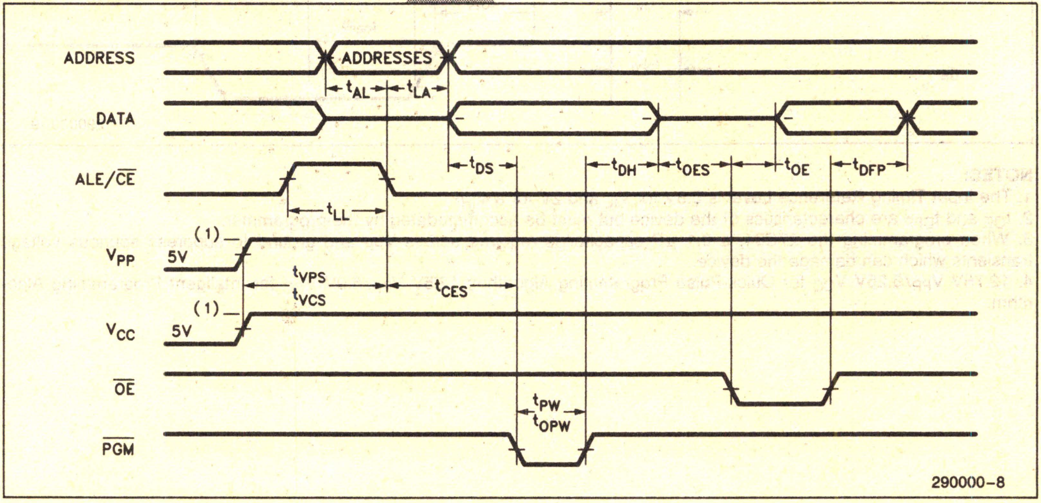
A.C. PROGRAMMING CHARACTERISTICS 87C64

T_A = 25°C ±5°C, See Table 2 for V_{CC} and V_{PP} Voltages.

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typ	Max		
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{LL}	Chip Deselect Width	2			µs	
t_{AL}	Address to Chip Select Setup	1			µs	
t_{LA}	Address Hold from Chip Select	1			µs	
t_{PW}	$\overline{PGM}$ Initial Pulse Width	0.95	1.0	1.05	ms	$int_e ligent$
		95	100	105	µs	Quick-Pulse
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	$int_e ligent$
t_{DS}	Data Setup Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Data Float	0		130	ns	
t_{OES}	Output Enable Setup Time	2			µs	
t_{OE}	Data Valid from Output Enable			150	ns	
t_{DH}	Data Hold Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	

NOTE:
1. Programming tolerances and test conditions are the same as 27C64.

PROGRAMMING WAVEFORMS 87C64


ADDRESS
ADDRESSES
t_{AL}
t_{LA}
DATA
ALE/$\overline{CE}$
t_{DS}
t_{DH}
t_{OES}
t_{OE}
t_{DFP}
t_{LL}
(1)
V_{PP}
5V
t_{VPS}
t_{VCS}
t_{CES}
(1)
V_{CC}
5V
$\overline{OE}$
t_{PW}
t_{OPW}
$\overline{PGM}$

290000-8

NOTE:
1. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for $int_e ligent$ Programming Algorithm.

27128A
ADVANCED 128K (16K x 8) PRODUCTION AND UV ERASABLE PROMs

- **Fast 200 nsec Access Time**
  - **HMOS* II-E Technology**
- **Low Power**
  - **100 mA Maximum Active**
  - **40 mA Maximum Standby**
- **int$_e$ligent Identifier™ Mode**
  - **Automated Programming Operations**
- **Compatible with 2764A, 27128, 27256**
- **New Quick-Pulse Programming™ Algorithm**
  - **Used on Plastic DIP**
  - **int$_e$ligent Programming™ Algorithm Compatible**
- **±10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip and Plastic Packages**
  (See Packaging Spec, Order #231369)

The Intel 27128A is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128A is an advanced high speed version of the 27128 and is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

The 27128A is currently available in two different package types. CERDIP packages provide flexibility in prototyping and R&D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments.

Intel's new Quick-Pulse Programming Algorithm enables these Plastic EPROMs to be programmed within two seconds. Programming equipment that takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment and is used to program CERDIP devices.

The 27128A is available in fast access times including 200 ns (27128A-2). This ensures compatibility with high-performance microprocessors, such as Intel's 8 MHz 80186 allowing full speed operation without the addition of WAIT states. The 27128A is also directly compatible with the 12 MHz 8051 family. For access times down to 110 ns, refer to the 27128B data sheet.

*HMOS is a patented process of Intel Corporation.

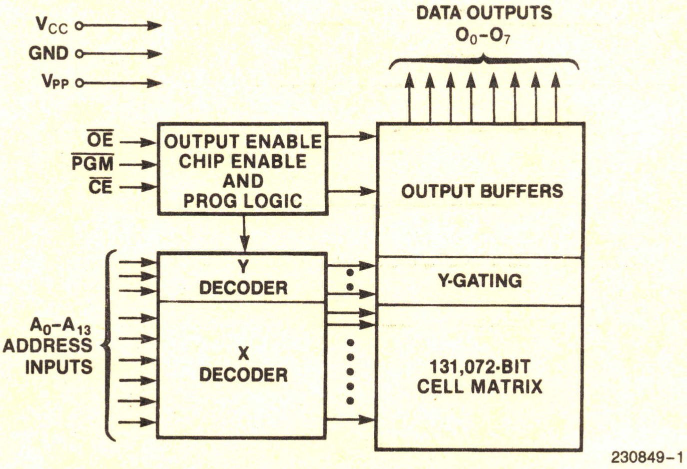


Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

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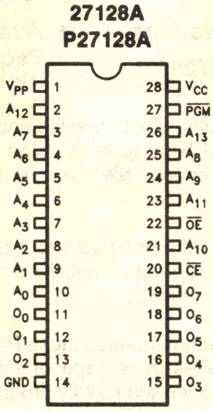
Pin Names

A_0–A_{13}	ADDRESSES
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{\text{PGM}}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE
$\overline{\text{WE}}$	WRITE ENABLE

27916	27513	27512	27256 87C256 27C256	2764 2764A 27C64 87C64	2732 2732A	2716	27128A pin
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}			V_{PP} 1
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}			A_{12} 2
A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7 3
A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6 4
A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5 5
A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4 6
A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3 7
A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2 8
A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1 9
A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0 10
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0	O_0 11
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1	O_1 12
O_2	O_2	O_2	O_2	O_2	O_2	O_2	O_2 13
GND	GND	GND	GND	GND	GND	GND	GND 14


27128A
P27128A
V_{PP} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{\text{PGM}}$
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{\text{OE}}$
21 A_{10}
20 $\overline{\text{CE}}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

27128A pin	2716	2732 2732A	2764 2764A 27C64 87C64	27256 87C256 27C256	27512	27513	27916
28 V_{CC}			V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
27 $\overline{\text{PGM}}$			$\overline{\text{PGM}}$	A_{14}	A_{14}	$\overline{\text{WE}}$	$\overline{\text{PGM/WE}}$
26 A_{13}	V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
25 A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8
24 A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9
23 A_{11}	V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
22 $\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}/V_{PP}$	$\overline{\text{OE}}$
21 A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
20 $\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$ ALE/$\overline{\text{CE}}$	$\overline{\text{CE}}$ ALE/$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$
19 O_7	O_7	O_7	O_7	O_7	O_7	O_7	O_7
18 O_6	O_6	O_6	O_6	O_6	O_6	O_6	O_6
17 O_5	O_5	O_5	O_5	O_5	O_5	O_5	O_5
16 O_4	O_4	O_4	O_4	O_4	O_4	O_4	O_4
15 O_3	O_3	O_3	O_3	O_3	O_3	O_3	O_3

230849-2

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128A Pins

Figure 2. Cerdip(D)/Plastic(P) DIP Pin Configurations

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8
A	−40°C to +125°C	None
B	−40°C to +125°C	168 ±8

EXPRESS OPTIONS

27128A Versions

	Packaging Options	
Speed Versions	**Cerdip**	**Plastic**
-2	T, L, Q, A, B	
-20	T, L, Q,	
-STD	T, L, Q, A, B	
-25	T, L, Q, A, B	
-3	T, L, Q, A, B	
-30	Q	

READ OPERATION

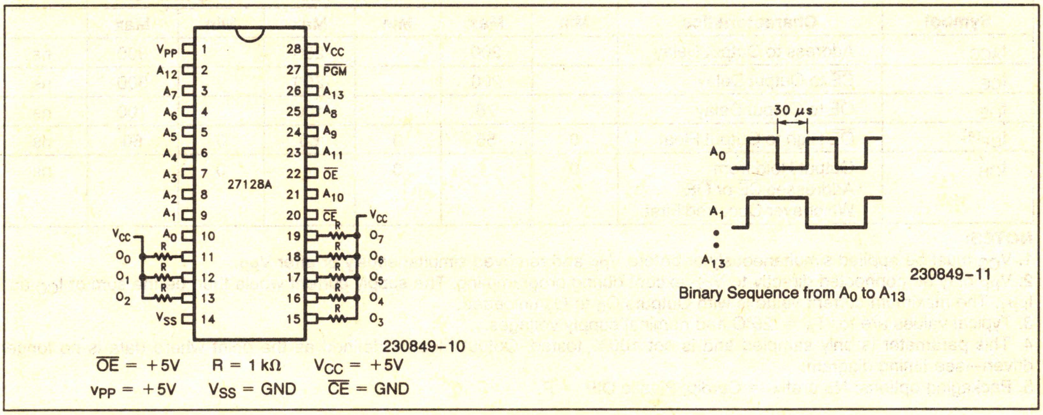
D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27128A, LD27128A TP27128A, TN27128A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}, V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:

1. The maximum current value is with Outputs O_0 to O_7 unloaded.



230849-10

$\overline{OE}$ = +5V R = 1 kΩ V_{CC} = +5V

V_{PP} = +5V V_{SS} = GND $\overline{CE}$ = GND

Binary Sequence from A_0 to A_{13}

230849-11

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read .... 0°C to +70°C
Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Input or Output Voltages with Respect to Ground .... −0.6V to +6.25V
Voltage on A_9 with Respect to Ground .... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground .... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			10	μA	$V_{IN}=5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT}=5.5V$
I_{PP1}(2)	V_{PP} Current Read			5	mA	$V_{PP}=5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE}=V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			100	mA	$\overline{CE}=\overline{OE}=V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL}=2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-400$ μA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	V	$V_{CC}=5.0V\pm0.25$

A.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Versions(5)	$V_{CC}\pm5\%$	27128A-2 P27128A-2		27128A P27128A		27128A-3 P27128A-3		Unit
	$V_{CC}\pm10\%$	27128A-20		27128A-25 P27128A-25		27128A-30 P27128A-30		
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100		100	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	55	0	60	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

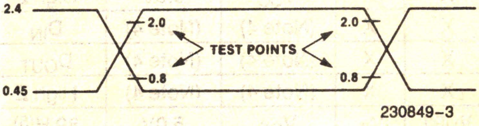
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging options: No prefix = Cerdip; Plastic DIP = P.

CAPACITANCE(2) $T_A = 25°C, f = 1MHz$

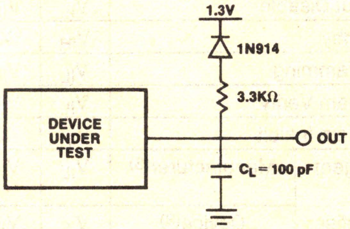
Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
2.0
2.0
TEST POINTS
0.8
0.8
0.45
230849-3

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

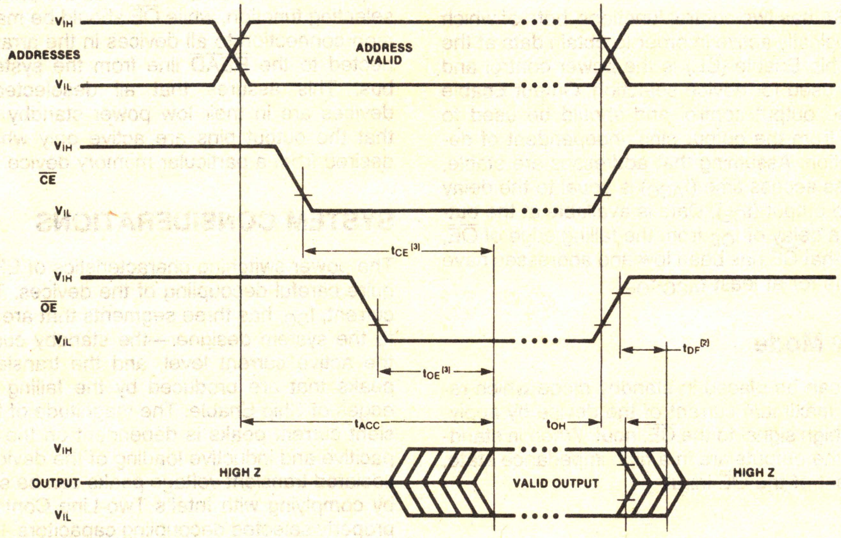
A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

C_L = 100 pF
C_L Includes Jig Capacitance

230849-4

A.C. WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE} (3)
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} (2)
t_{OE} (3)
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z

230849-5

NOTES:

1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
inteligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89 H(5) 88 H(5)
	Device(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	89 H

NOTES:

1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. $A_1 - A_8$, $A_{10} - A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturer's Identifier reads 89H for Cerdip EPROMs: 88H for Plastic EPROMs.

Read Mode

The 27128A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

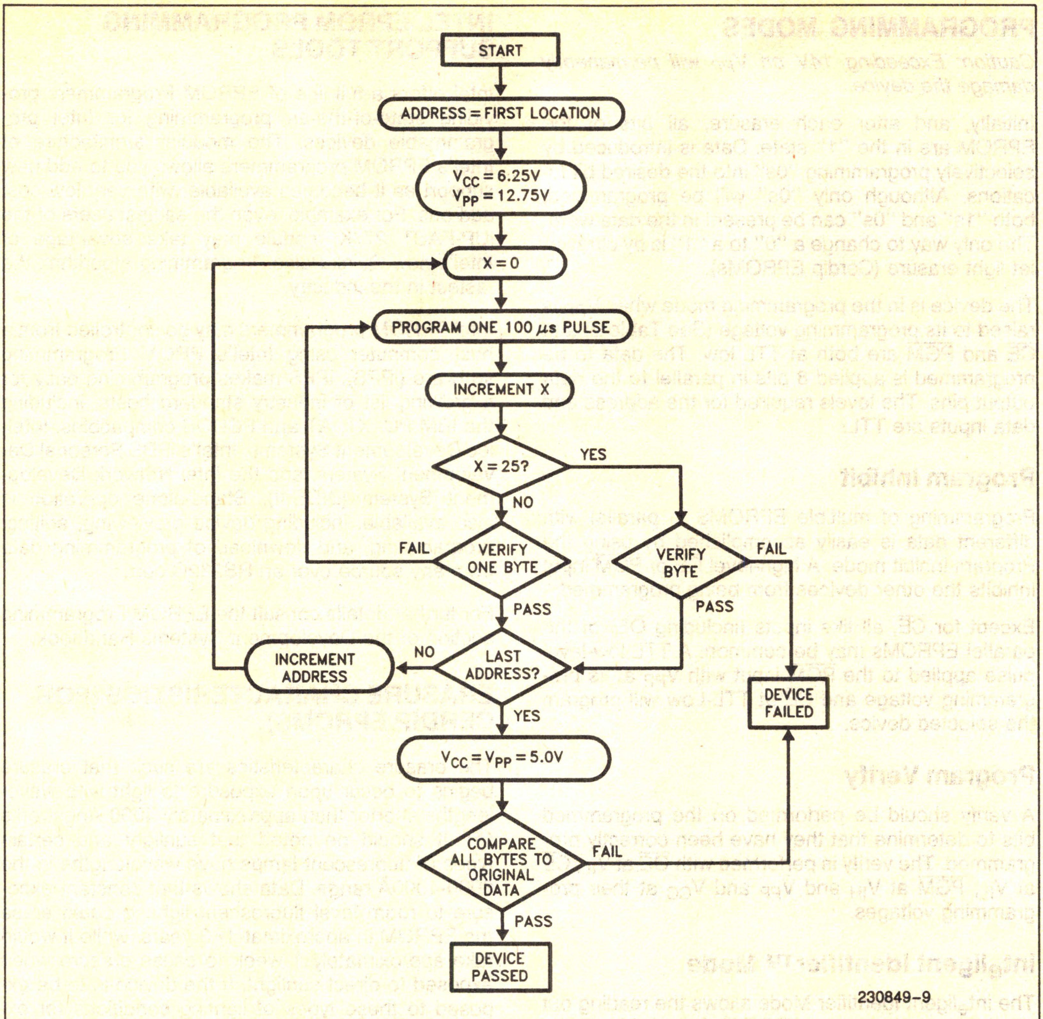

START
ADDRESS = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
VERIFY BYTE
FAIL
PASS
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
DEVICE FAILED
YES
V_{CC} = V_{PP} = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
230849–9

Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic EPROMs)

Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic devices to be programmed in under two seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic EPROMs are also compatible with Intel's int$_{e}$ligent Programming Algorithm.

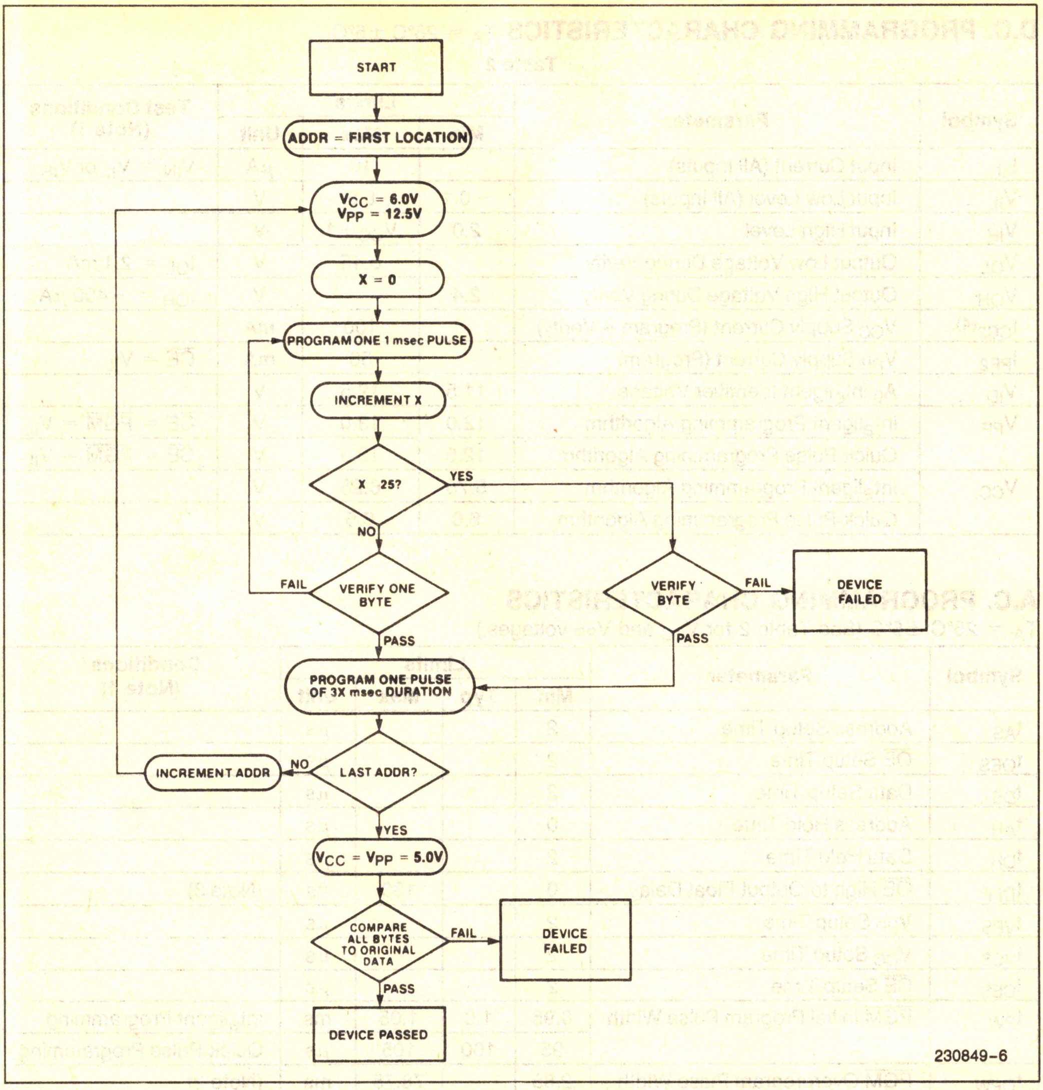

START
ADDR = FIRST LOCATION
VCC = 6.0V
VPP = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
230849-6

Figure 5. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, is required for all of Intels 12.5V V_{PP} Cerdip EPROMs. Plastic EPROMs may also be programmed using this method. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 5.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS T_A = 25°C ±5°C

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
$I_{CC2}^{(4)}$	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_{e}$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_{e}$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_{e}$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C (See Table 2 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_{e}$ligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

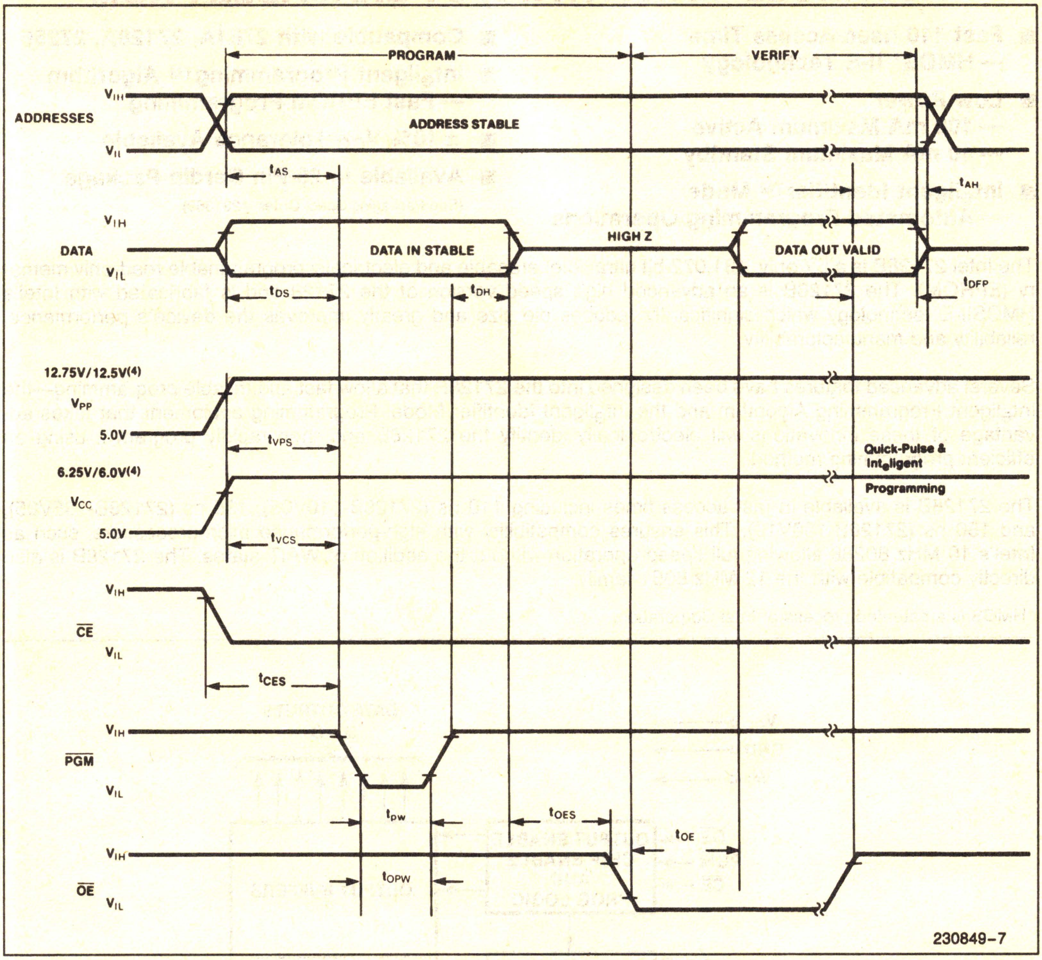
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (int$_{e}$ligent Programming Algorithm only) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
12.75V/12.5V(4)
V_{PP}
5.0V
t_{VPS}
6.25V/6.0V(4)
V_{CC}
5.0V
t_{VCS}
Quick-Pulse & Int$_e$ligent Programming
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
t_{OPW}
230849-7

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

PRELIMINARY

27128B
ADVANCED 128K (16K x 8) UV ERASABLE PROM

- **Fast 110 nsec Access Time**
  — HMOS* II-E Technology
- **Low Power**
  — 100 mA Maximum Active
  — 40 mA Maximum Standby
- **inteligent Identifier™ Mode**
  — Automated Programming Operations
- **Compatible with 2764A, 27128A, 27256**
- **inteligent Programming™ Algorithm**
  — Fast EPROM Programming
- **± 10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec, Order #231369)

The Intel 27128B is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128B is an advanced high speed version of the 27128 and is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

Several advanced features have been designed into the 27128B that allow fast and reliable programming—the inteligent Programming Algorithm and the inteligent Identifier Mode. Programming equipment that takes advantage of these innovations will electronically identify the 27128B and then rapidly program it using an efficient programming method.

The 27128B is available in fast access times including 110 ns (27128B-110V05), 135 ns (27128B-135V05), and 150 ns (27128B-150V10). This ensures compatibility with high-performance microprocessors, such as Intel's 10 MHz 80286 allowing full speed operation without the addition of WAIT states. The 27128B is also directly compatible with the 12 MHz 8051 family.

*HMOS is a patented process of Intel Corporation.

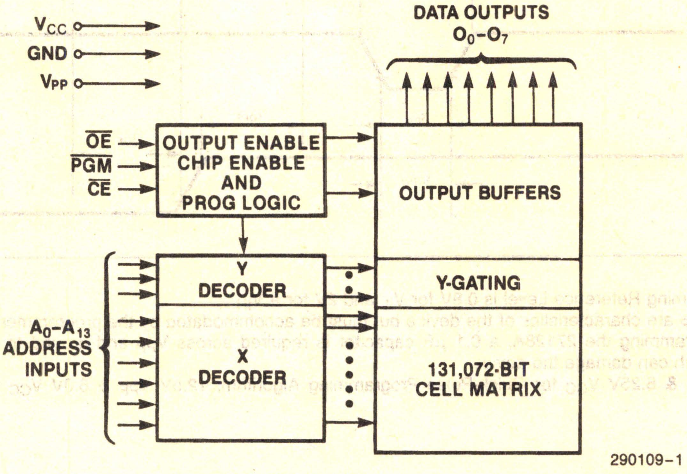


Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.
February 1986
Order Number: 290109-001
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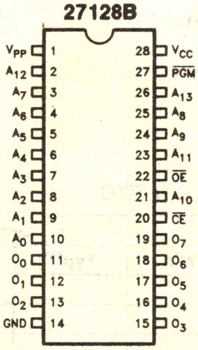
Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE
$\overline{WE}$	WRITE ENABLE

27916	27513	27512	27256 87C256 27C256	2764 2764A 27C64 87C64	2732 2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND	GND	GND


27128B
V_{PP} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}$
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

2716	2732 2732A	2764 2764A 27C64 87C64	27256 87C256 27C256	27512	27513	27916
		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}	$\overline{WE}$	$\overline{PGM}/\overline{WE}$
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

290109-2

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128B Pins

Figure 2. Cerdip(D) Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read . . . . 0°C to +70°C

Temperature Under Bias . . . . −10°C to +80°C

Storage Temperature . . . . −65°C to +125°C

All Input or Output Voltages with Respect to Ground . . . . −0.6V to +6.25V

Voltage on A_9 with Respect to Ground . . . . −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming . . . . −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground . . . . −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			10	µA	$V_{IN}=5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT}=5.5V$
I_{PP1}(2)	V_{PP} Current Read			5	mA	$V_{PP}=5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE}=V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			100	mA	$\overline{CE}=\overline{OE}=V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL}=2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-400$ µA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	V	$V_{CC}=5.0V\pm0.25$

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions	$V_{CC}\pm5\%$	27128B-110V05		27128B-135V05		27128B-150V10		Unit
	$V_{CC}\pm10\%$							
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		110		135		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		110		135		150	ns
t_{OE}	$\overline{OE}$ to Output Delay		55		65		65	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	45	0	55	0	55	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

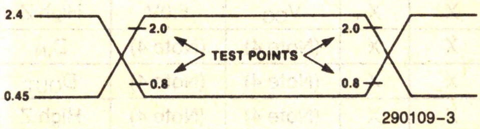
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE[2] $T_A = 25°C, f = 1MHz$

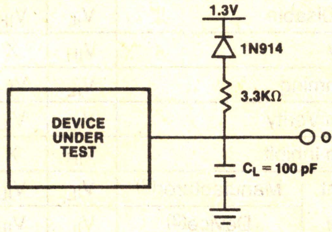
Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
290109-3

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

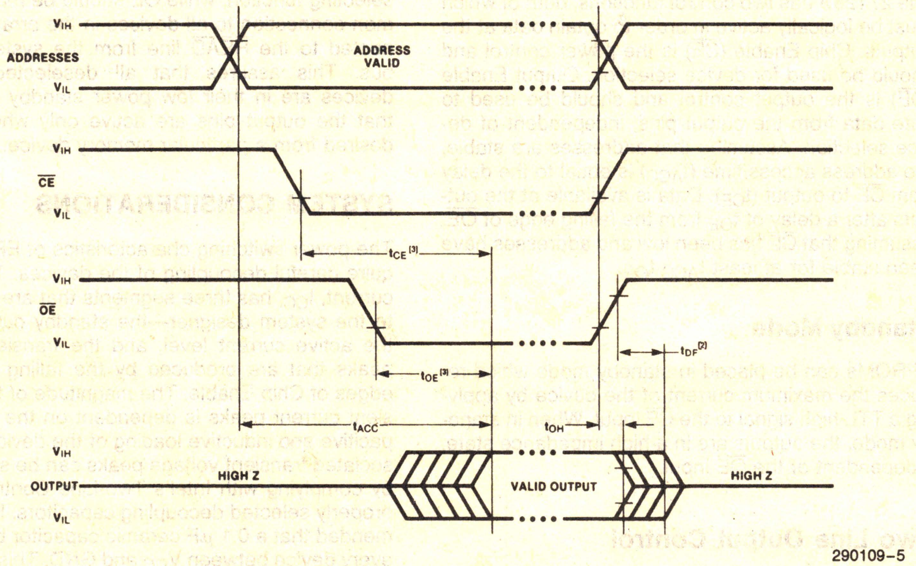
A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
$C_L = 100$ pF

$C_L = 100$ pF
C_L Includes Jig Capacitance

290109-4

A.C. WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE} [3]
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} [2]
t_{OE} [3]
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z
290109-5

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128B are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Pins Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89 H
	Device(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	89 H

NOTES:

1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1-A_8, $A_{10}-A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27128B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

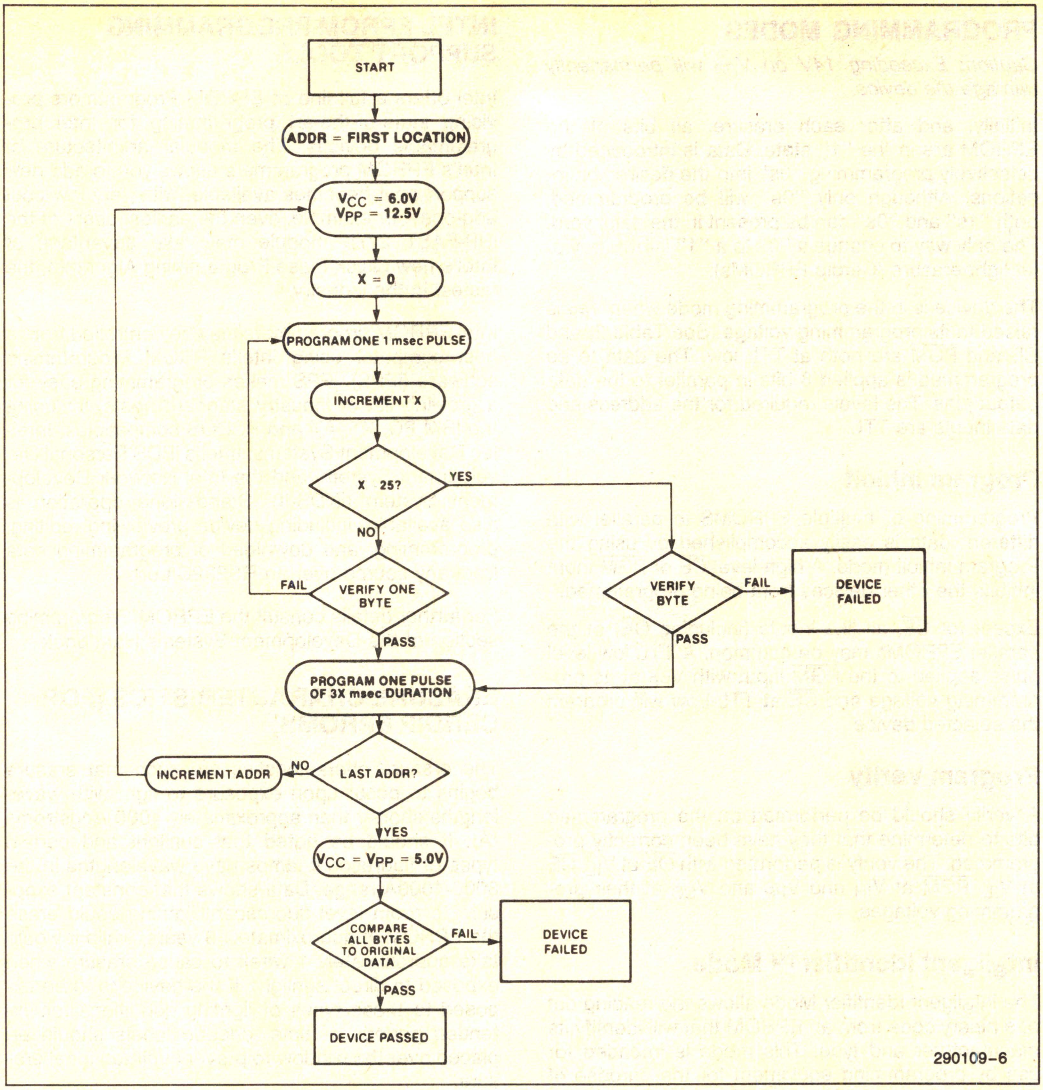

START
ADDR = FIRST LOCATION
V_{CC} = 6.0V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
V_{CC} = V_{PP} = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
290109–6

Figure 5. int$_{e}$ligent Programming™ Flowchart

int$_{e}$ligent Programming™ Algorithm

The int$_{e}$ligent Programming Algorithm, a standard in the industry for the past few years, can be used to program all of Intels 12.5V V_{PP} EPROMs. A flowchart of the int$_{e}$ligent Programming Algorithm is shown in Figure 5.

The int$_{e}$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_{e}$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

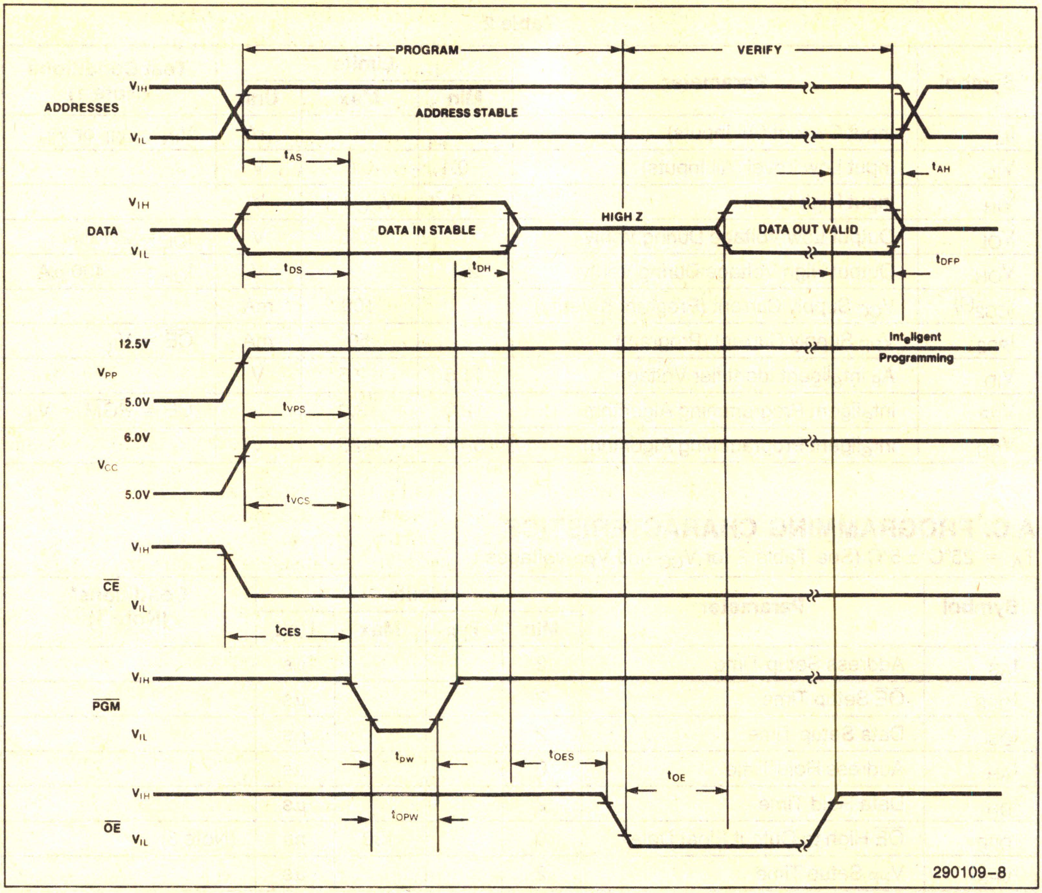
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_IH
V_IL
ADDRESS STABLE
t_AS
t_AH
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DFP
12.5V
V_PP
5.0V
Intelligent Programming
t_VPS
6.0V
V_CC
5.0V
t_VCS
CE
t_CES
PGM
t_PW
t_OES
t_OE
t_OPW
OE
290109-8

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128B, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27256
256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
  - **4 Second Programming**
  - **int$_e$ligent Programming™ Algorithm Compatible**
- **Fast Access Time**
  - **170 ns D27256-1**
  - **200 ns P27256-2**
- **int$_e$ligent Identifier™ Mode**
- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package**
  (See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and elminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.

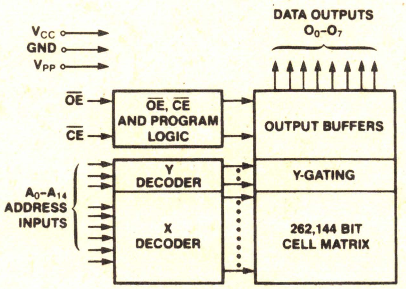


Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

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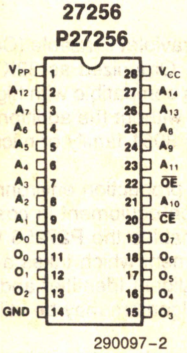
Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
D.U.	Don't Use
$\overline{WE}$	Write Enable

27916	27513	27512	27128A	2764A 27C64	2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd


27256
P27256
V_{PP} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 A_{14}
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3
290097-2

2716	2732A	2764A 27C64	27128A	27512	27513	27916
		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A_{14}	$\overline{WE}$	$\overline{PGM}/\overline{WE}$
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

NOTE:
Intel"Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27256 VERSIONS

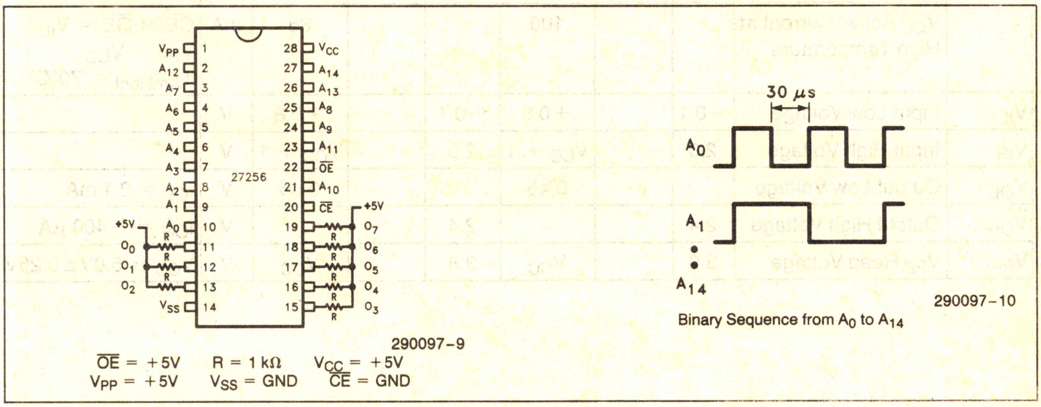
Speed Versions	Packaging Options	
	Cerdip	Plastic
-1	Q, T, L	
-2	Q, T, L	
STD	Q, T, L	
-3	Q, T, L	
-20	Q, T, L	
-25	Q, T, L	
-30	Q, T, L	

READ OPERATION
D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27256 LD27256		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I_{CC}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}, T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
11
12
13
VSS 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19
18
17
16
15
27256
+5V
O0
O1
O2
R
O7
O6
O5
O4
O3
290097-9
OE = +5V
VPP = +5V
R = 1 kΩ
VSS = GND
VCC = +5V
CE = GND
30 μs
A0
A1
A14
290097-10
Binary Sequence from A0 to A14

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .... 0°C to +70°C
Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground .... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground .... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect
to Ground .... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground .... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	27256-1, 27256-2, 27256-20, P27256-2 & P27256-5 Limits			27256L-20, 27256-25, 27256-30, 27256L-1, 27256L-2, 27256, 27256-3 P27256-25, P27256-30, P27256 & P27256-3 Limits			Unit	Test Conditions
		Min	Typ (3)	Max	Min	Typ (3)	Max		
I_{LI}	Input Load Current			10			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10			10	μA	$V_{OUT} = 5.5V$
I_{PP_1}(2)	V_{PP} Current Read/Standby			5			5	mA	$V_{PP} = 5.5V$
I_{SB}(2)	V_{CC} Current Standby		25	50		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active		55	125		45	100	mA	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$
	V_{CC} Active Current at High Temperature			100			85	mA	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ $T_{Ambient} = 70°C$
V_{IL}	Input Low Voltage	−0.1		+0.8	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			2.4			V	$I_{OH} = -400$ μA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25V$

READ OPERATION

A.C. CHARACTERISTICS $0^\circ C \le T_A \le +70^\circ C$

Versions(5)	$V_{CC} \pm 5\%$	27256-1 27256L-1		27256L-2 27256-2 P27256-2		27256 P27256 P27256-5		27256-3 P27256-3		Unit	Test Conditions
	$V_{CC} \pm 10\%$			27256L-20 27256-20		27256-25 P27256-25		27256-30 P27256-30			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
t_{ACC}	Address to Output Delay		170		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250		300	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		70		75		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	35	0	55	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns	

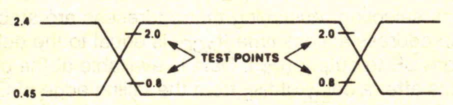
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $t_A = 25^\circ C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP.

CAPACITANCE(2) ($T_A = 25^\circ C$, f = 1 MHz)

Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

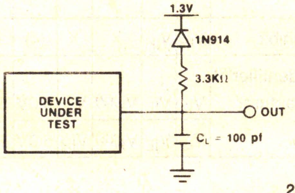
A.C. TESTING INPUT/OUTPUT WAVEFORM



290097-3

A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

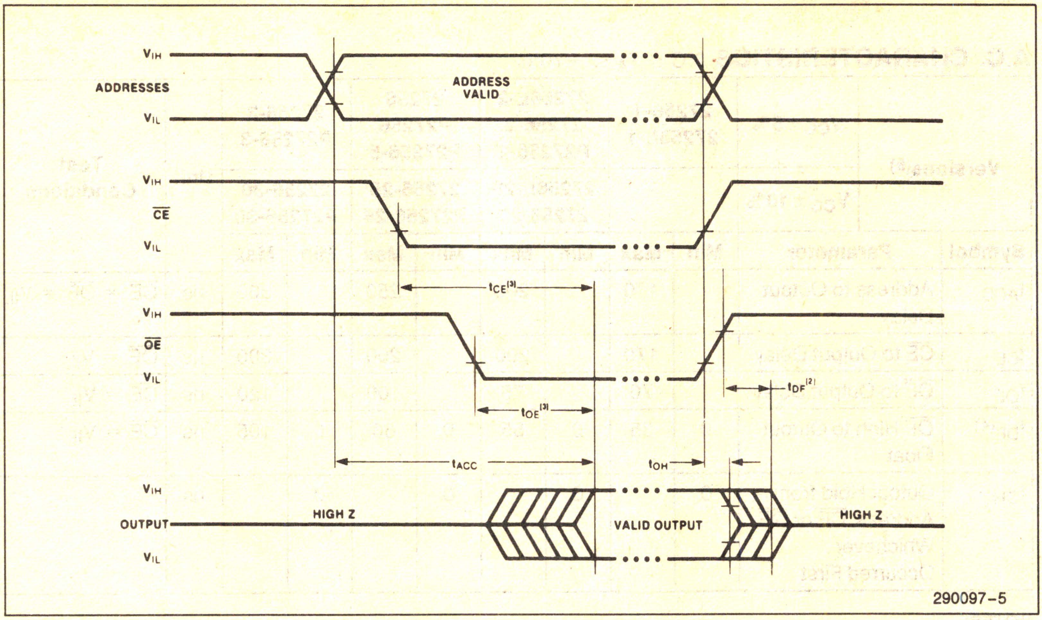
A.C. TESTING LOAD CIRCUIT



290097-4

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

Table 1. Operating Modes

Pins Mode	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	(4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(4)	(4)	High Z
int$_e$ligent Identifier(3) —manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	5.0V	5.0V	89H(5) 88H(5)
—device	V_{IL}	V_{IL}	V_H(2)	V_{IH}	5.0V	5.0V	04H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1-A_8, $A_{10}-A_{13} = V_{IL}$, $A_{14} = V_{IH}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturers identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

DEVICE OPERATION

The modes of operation of the 27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for int$_e$ligent identifier mode.

Read Mode

The P27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1"is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} and V_{CC} at their programming voltages.

Optional Program Verify

The optional verify may be performed in place of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at its programming voltage. The outputs will tri-state according to the signal presented to $\overline{OE}$. Therefore, all devices with V_{PP} = 12.75V (12.5V int$_{e}$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share a common bus, V_{PP} should be lowered to V_{CC} (= 6.25/6.0V—see Table 2) and the normal read mode used to execute a program verify.

int$_{e}$ligent Identifier™ Mode

The int$_{e}$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

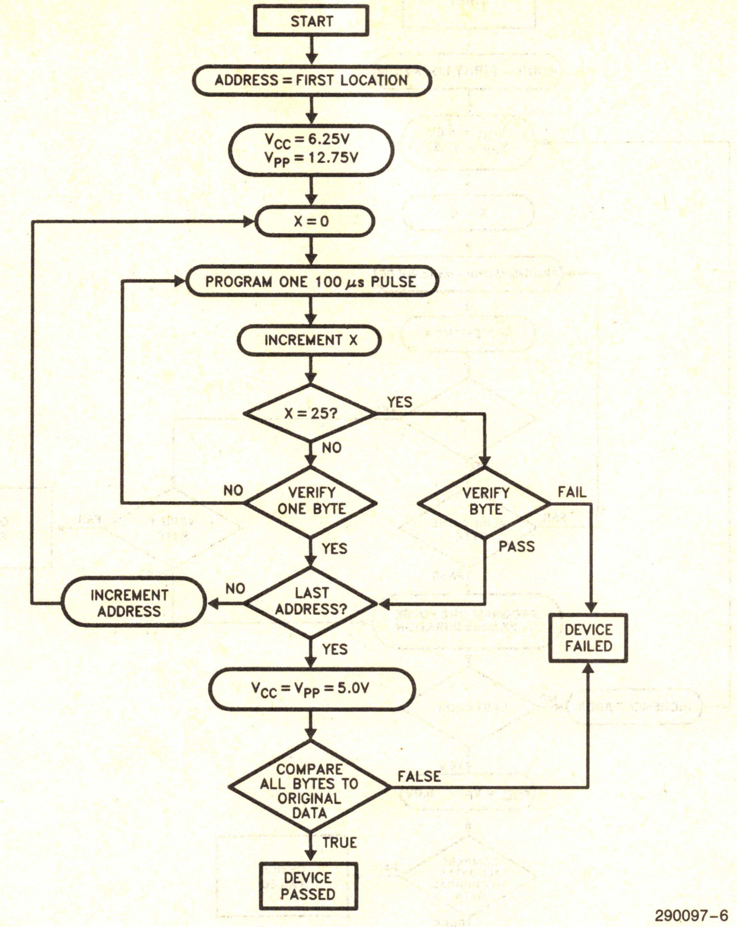

START
ADDRESS = FIRST LOCATION
$V_{CC} = 6.25V$
$V_{PP} = 12.75V$
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
NO
YES
VERIFY BYTE
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
$V_{CC} = V_{PP} = 5.0V$
COMPARE ALL BYTES TO ORIGINAL DATA
FALSE
TRUE
DEVICE PASSED
290097-6

Figure 3. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic and PLCC EPROMs)

Intel's Plastic and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows both Plastic and PLCC devices to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{CC} = 6.25V$ and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

In addition to the Quick-Pulse Programming Algorithm, Plastic and PLCC EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

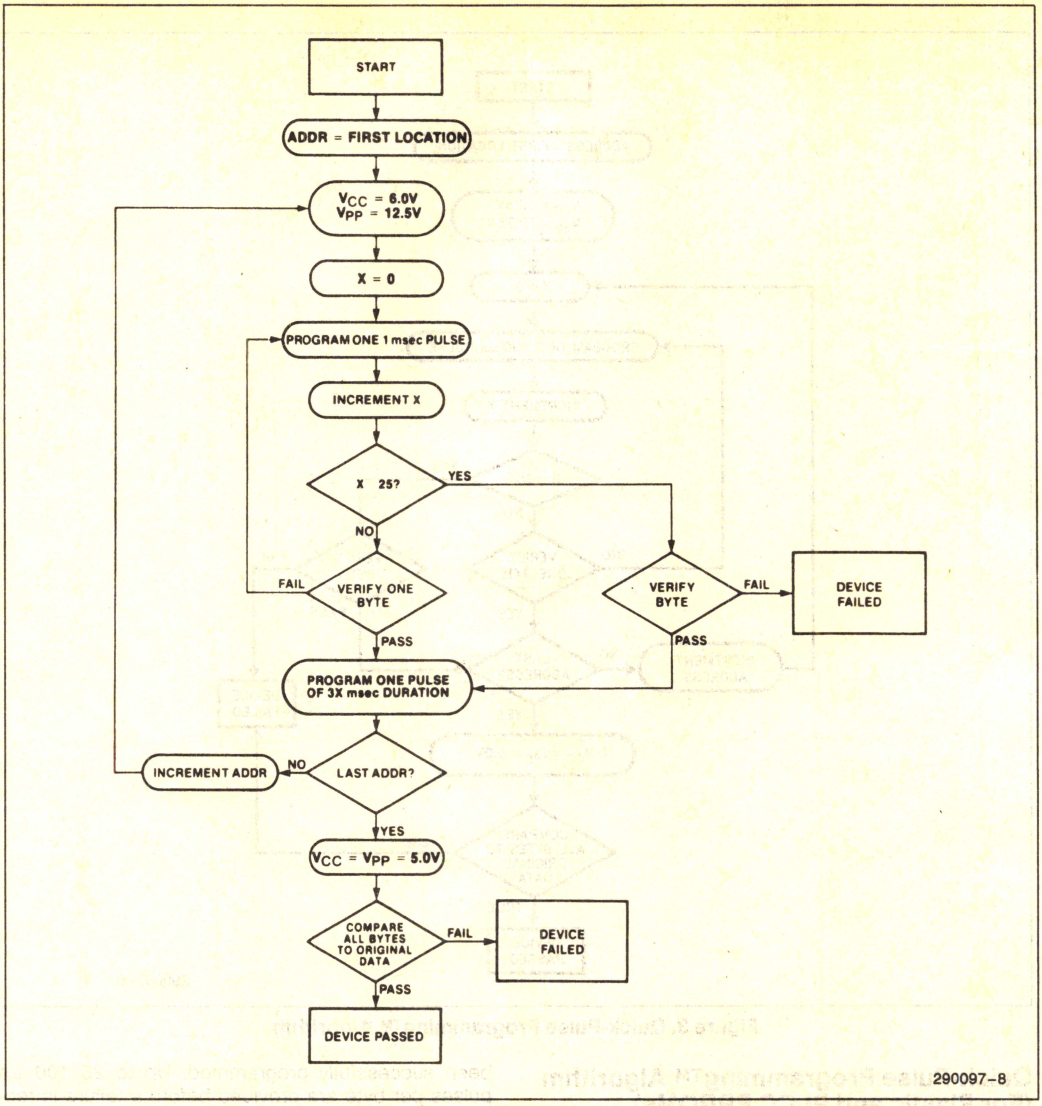

START
ADDR = FIRST LOCATION
VCC = 6.0V
VPP = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
290097-8

Figure 4. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\ \mu A$
$I_{CC2}^{(4)}$	V_{CC} Supply Current (Program & Verify)		125	mA	
$I_{PP2}^{(4)}$	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

Symbol	Parameter	Limits				Test Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Data Float Delay	0		130	μs	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) .... 20 ns

Input Pulse Levels .... 0.45V to 2.4V

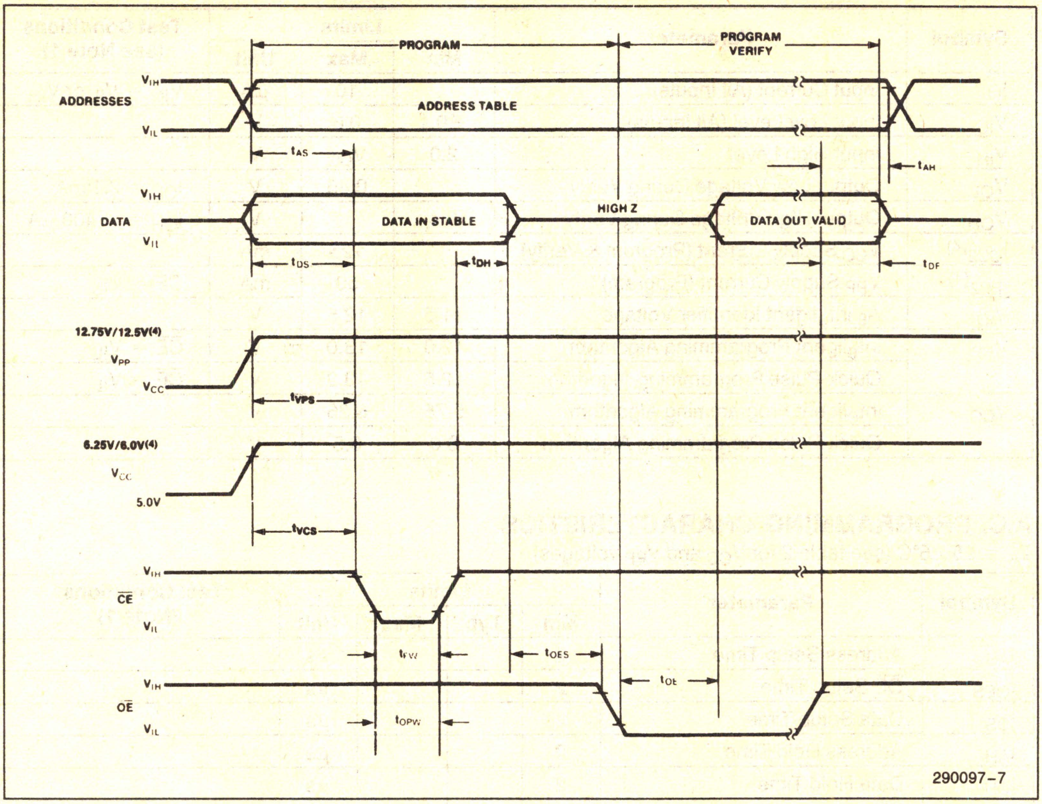
Input Timing Reference Level .... 0.8V and 2.0V

Output Timing Reference Level ...... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (int$_e$ligent Programming Algorithm only).
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
PROGRAM VERIFY
ADDRESSES
V_IH
V_IL
ADDRESS TABLE
t_AS
t_AH
DATA
V_IH
V_IL
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DF
12.75V/12.5V(4)
V_PP
V_CC
t_VPS
6.25V/6.0V(4)
V_CC
5.0V
t_VCS
V_IH
CE
V_IL
t_PW
t_OES
t_OE
V_IH
OE
V_IL
t_OPW

290097-7

NOTES:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27256 a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm. 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27C256/87C256
256K (32K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **CHMOS/NMOS Microcontroller and Microprocessor Compatible**
  - **87C256-Integrated Address Latch**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current**
- **High Performance Speeds**
  - **170 ns Maximum Access Time**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **New Quick-Pulse Programming™ Algorithm**
  - **4 Second Programming**
- **Available in 28-Pin Cerdip and Plastic DIP Package and 32-Lead PLCC Package.**

  (See Packaging Spec., Order #231369)

Intel's 27C256 and 87C256 CHMOS EPROMs are 256K bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C256 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C256 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 27256 (HMOS II-E).

The 27C256 and 87C256(1) are offered in ceramic DIP, Plastic DIP(2) and plastic leaded chip carrier (PLCC) package. Cerdip packages provide flexibility in prototyping and R&D environments, whereas, Plastic DIP and PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming Algorithm is employed on these devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse Compatible programming equipment, the int$_e$ligent Programming™ Algorithm may be utilized.

The 87C256 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate the address latch by tieing address and data pins of the 87C256 directly to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs (A_0–A_{14}) is latched internally. The address inputs are then ignored as data information is passed on the same bus from the EPROM O_0–O_7 Pins (ALE/$\overline{CE}$ remains low).

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.

NOTE:
1. The 87C256 will be available in 1987.
2. Plastic DIP versions will be available 2nd quarter, 1987.

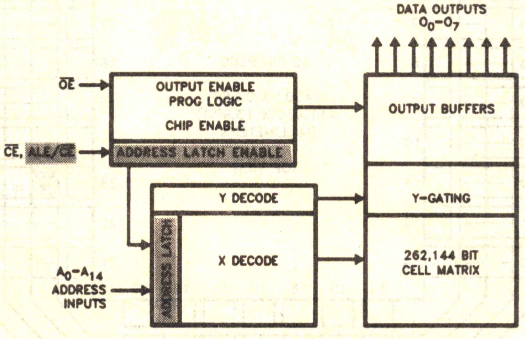


Figure 1. Block Diagram

Shaded areas ▨ represent the 87C256 version

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986
Order Number: 290044-005

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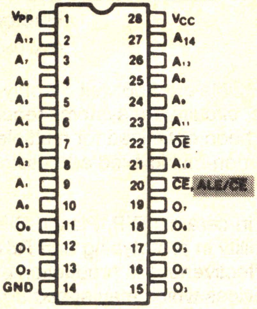
Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/$\overline{CE}$	ADDRESS LATCH ENABLE /CHIP ENABLE
N.C.	NO CONNECT
D.U.	DON'T USE

27128	2764A	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

27C256/87C256
P27C256/P87C256


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE, ALE/CE
19 O7
18 O6
17 O5
16 O4
15 O3

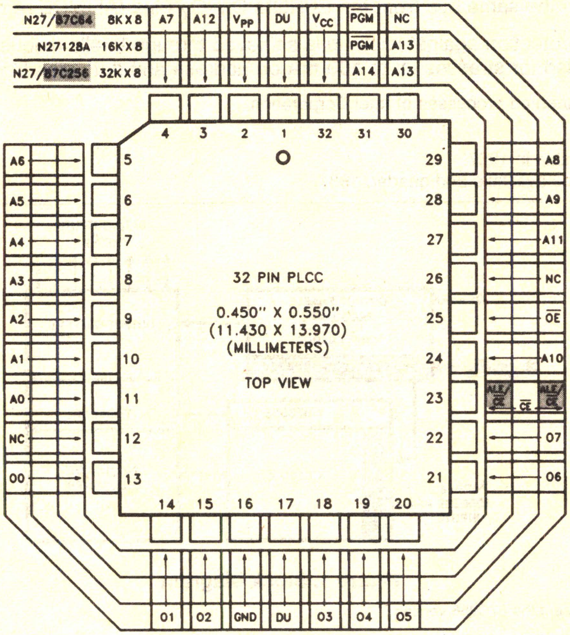
2716	2732A	2764A	27128
		V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$
V_{CC}	V_{CC}	N.C.	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

290044-2

Figure 2. Pin Configuration

NOTE:
Intel "Universal Site" -Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.

Shaded Areas ▨ represent the 87C256 version


N27/87C64 8KX8
N27128A 16KX8
N27/87C256 32KX8
A7
A12
VPP
DU
VCC
PGM
NC
PGM
A13
A14
A13
4
3
2
1
32
31
30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
O0 13
29 A8
28 A9
27 A11
26 NC
25 OE
24 A10
23 ALE/CE CE ALE/CE
22 O7
21 O6
14
15
16
17
18
19
20
O1
O2
GND
DU
O3
O4
O5
32 PIN PLCC
0.450" X 0.550"
(11.430 X 13.970)
(MILLIMETERS)
TOP VIEW

290044-10

Figure 3. PLCC Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS Options

27C256/87C256 Versions

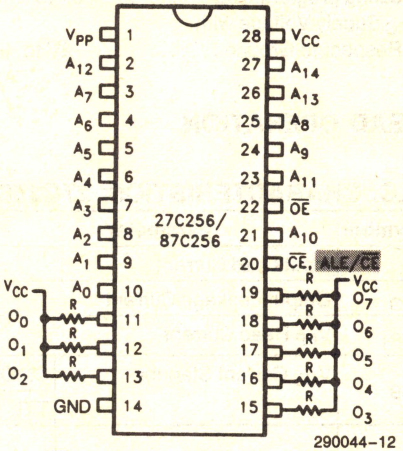
Speed Versions	Packaging Options	
	Cerdip	PLCC
−1		
−17		
−2	T, L, Q, A, B	T
−20	T, L, Q, A*	T
STD	T, L, Q, A, B	T
−25	T, L, Q, A*	T
−3	T, L, Q, A, B	T
−30	T, L, Q, A*	T

*Available in 27C256 only.

EPROM Product Family

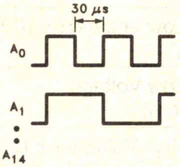
PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A(2)	−40°C to +125°C	NONE
B(2)	−40°C to +125°C	168 ±8



290044-12

$\overline{OE}$ = 5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = 33.3 KHz



290044-13

Binary Sequence from A_0 to A_{14}

Burn-In Bias and Timing Diagrams

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter		27C256		Test Conditions
			Min	Max	
I_{SB}	V_{CC} Standby Current (ma)	CMOS		0.1	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
		TTL		1.0	
I_{CC_1}(1)	V_{CC} Active Current (ma)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (ma)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient}$ = 85°C

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.
2. See Automotive data sheets for current and timing parameters.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During
Read .... 0°C to +70°C(2)
Temperature Under Bias .... −10°C to +80°C(2)
Storage Temperature .... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground .... −2V to +7V(1)
Voltage on A_9 with
Respect to Ground .... −2V to +13.5V(1)
V_{PP} supply Voltage with Respect to Ground
during programming .... −2V to +14.0V(1)
V_{CC} Supply Voltage with
Respect to Ground .... −2V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS: 27C256/87C256

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current				0.01	1.0	μA	$V_{OUT} = 5.5V$
I_{PP_1}	V_{PP} Read Current		5			200	μA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby	CMOS	4			100	μA	$\overline{CE} = V_{CC}$
		TTL	8			1.0	mA	$\overline{CE} = V_{IH}$
I_{CC_1}	V_{CC} Current Active		5, 8			30	mA	$\overline{CE} = V_{IL}$ f = 5 MHz, $I_{OUT} = 0$ mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		$V_{CC} + 0.5$	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			$V_{CC} - 0.2$		$V_{CC} + 0.2$		
V_{OL}	Output Low Voltage					0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage			3.5			V	$I_{OH} = -2.5$ mA
I_{OS}	Output Short Circuit Current		6			100	mA	
V_{PP}	V_{PP} Read Voltage		7	$V_{CC} - 0.7$		V_{CC}	V	

NOTES:

1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$.
4. ALE/$\overline{CE}$ or $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum $I_{PP} + I_{CC}$. The maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
8. V_{IL}, V_{IH} levels at TTL inputs.

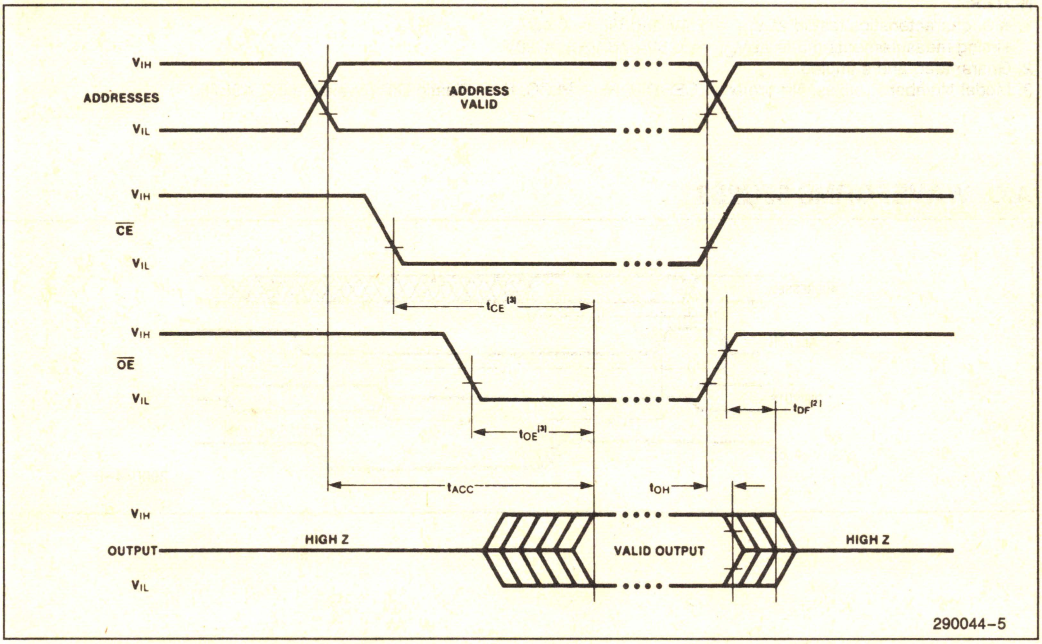
READ OPERATION

A.C. CHARACTERISTICS 27C256(1) 0°C ≤ T_A ≤ +70°C

Versions(3)	V_{CC} ±5%	27C256-1 N27C256-1 P27C256-1		27C256-2 N27C256-2 P27C256-2		27C256 N27C256 P27C256		27C256-3 N27C256-3 P27C256-3		Unit
	V_{CC} ±10%			27C256-20 N27C256-20 P27C256-20		27C256-25 N27C256-25 P27C256-25		27C256-30 N27C256-30 P27C256-30		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		70		75		100		120	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z		55		55		60		75	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V.
   Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed and sampled.
3. Model Number Prefixes: No Prefix = CERDIP; N = PLCC; P = Plastic DIP (available Q2, 1987).

A.C. WAVEFORMS 27C256


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE(3)
VIH
OE
VIL
tDF(2)
tOE(3)
tACC
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
290044-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

READ OPERATION

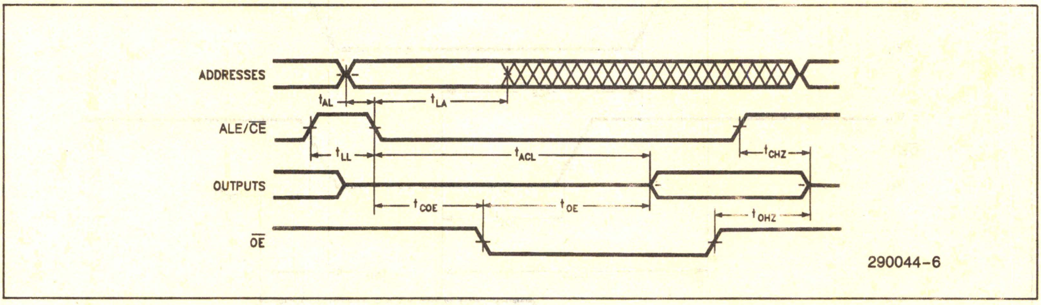
A.C. CHARACTERISTICS 87C256

Versions(3)								
	V_{CC} ±5%	87C256-2 N87C256-2 P87C256-2		87C256 N87C256 P87C256		87C256-3 N87C256-3 P87C256-3		Unit
	V_{CC} ±10%	87C256-20 N87C256-20 P87C256-20		87C256-25 N87C256-25 P87C256-25		87C256-30 N87C256-30 P87C256-30		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LL}	Chip Deselect Width	50		60		75		ns
t_{AL}	Address to CE-Latch Set-up	20		25		30		ns
t_{LA}	Address Hold from CE-LATCH	45		50		60		ns
t_{ACL}	CE-Latch Access Time		200		250		300	ns
t_{OE}	Output Enable to Output Valid		75		100		120	ns
t_{COE}	ALE/$\overline{CE}$ to Output Enable	45		50		60		ns
t_{CHZ}(2)	Chip Deselect to Output in High Z		55		60		75	ns
t_{OHZ}(2)	Output Disable to Output in High Z		55		60		75	ns

NOTES:

1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = CERDIP; N = PLCC; P = Plastic DIP (Available Q2, 1987).

A.C. WAVEFORMS 87C256

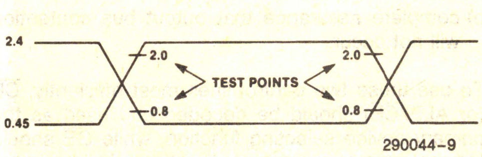


CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/control capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

NOTE:
1. Sampled. Not 100% tested.

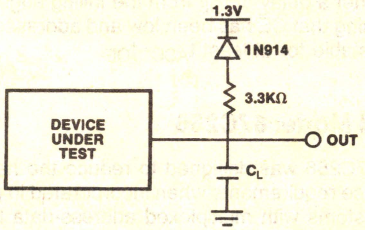
A.C. TESTING INPUT/OUTPUT WAVEFORM



290044-9

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



290044-3

C_L = 100 pF
C_L Includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C256/87C256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier™ mode.

Table 1. Mode Selection for 27C256 and 87C256

Pins Mode	ALE/$\overline{CE}$ $\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC} (Note 4)	(Note 4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	HIGH Z
int$_e$ligent Identifier (3) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier (3) -27C256	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	8C H
int$_e$ligent Identifier (3, 5) -87C256	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	80 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1-A_8, $A_{10-12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages during programming.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.

Read Mode: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Read Mode: 87C256

The 87C256 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C256 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C256. All address inputs of the 87C256 are latched when ALE/$\overline{CE}$ is brought low thus eliminating the need for a seperate address latch.

The 87C256 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the $\overline{OE}$ pin.

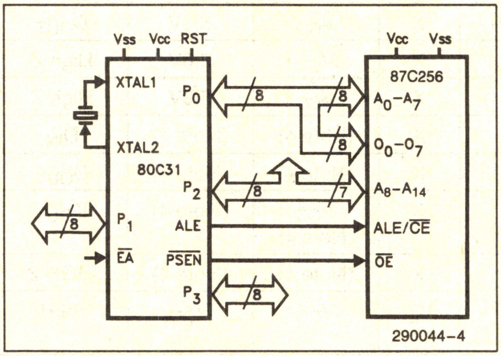


Figure 4. 80C31 with 87C256 System Configuration

Standby Mode

The 27C256 and 87C256 have Standby modes which reduce the maximum V_{CC} current to 100 μA. Both are placed in the Standby mode when $\overline{CE}$ or ALE/$\overline{CE}$ is in the CMOS-high state. When in Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (or ALE/$\overline{CE}$) should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus, This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ (or ALE/$\overline{CE}$) is pulsed to TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ (or ALE/$\overline{CE}$) input inhibits the other devices from being programmed.

Except for $\overline{CE}$ (or ALE/$\overline{CE}$) and $\overline{OE}$ all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ (or ALE/$\overline{CE}$) input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL} and $\overline{CE}$ (or ALE/$\overline{CE}$) at V_{IH}, and V_{PP} and V_{CC} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

Optional Program Verify

All 27C256s with V_{PP} = 12.75V (12.5V int$_e$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. The optional verify may be used in place of the verify mode to allow parallel programming where several devices share a common bus. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ = V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} = V_{CC} = 6.25V (6.0V int$_e$ligent programming). The outputs will then tri-state according to the signals presented to $\overline{OE}$ and $\overline{CE}$. With V_{PP} lowered to V_{CC} (= 6.25V/6.0V—See Table 2), the normal read mode may be used to execute a program verify.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code and byte 1 (A_0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1. ALE/$\overline{CE}$ of the 87C256 has to be toggled in order to latch in the addresses and read the signature codes.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new suport as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development Systems, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

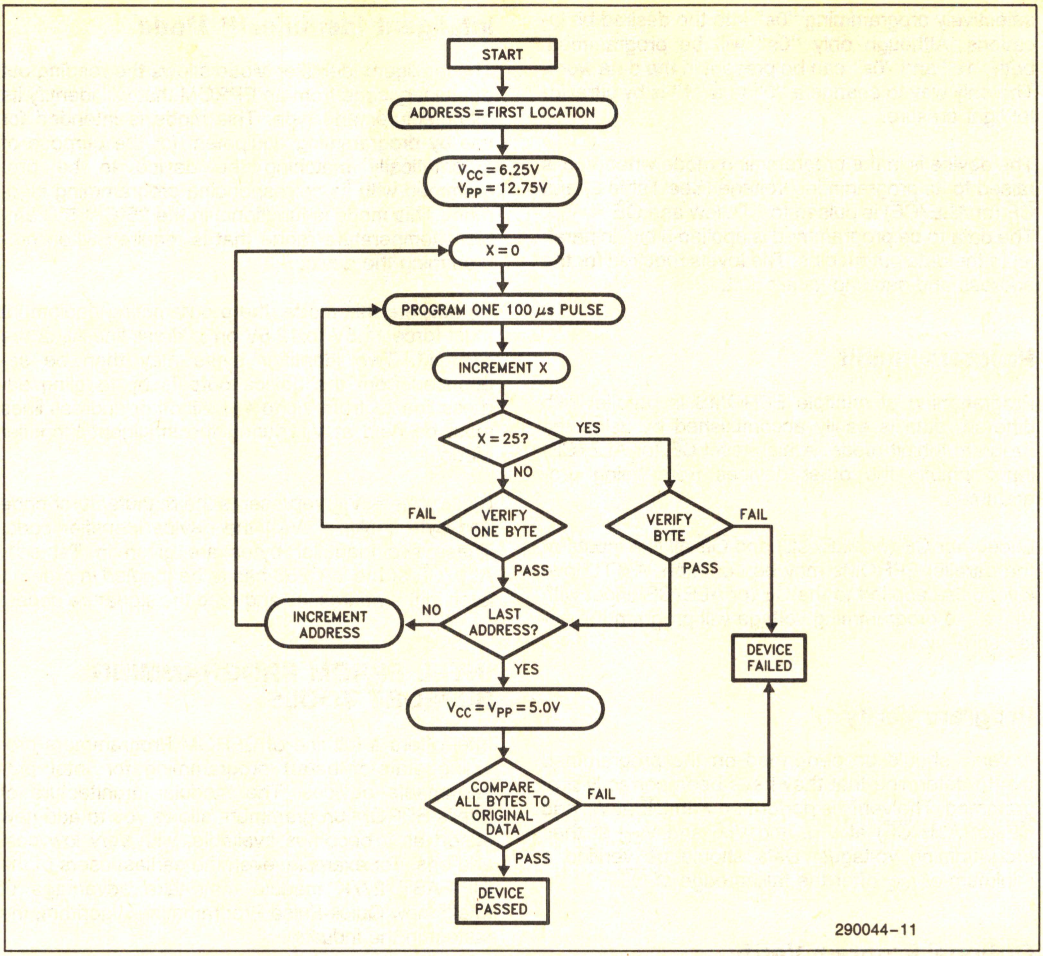

START
ADDRESS = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
VERIFY BYTE
FAIL
PASS
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
DEVICE FAILED
YES
V_{CC} = V_{PP} = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
290044-11

Figure 5. Quick-Pulse Programming™ Algorithm

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum inte-

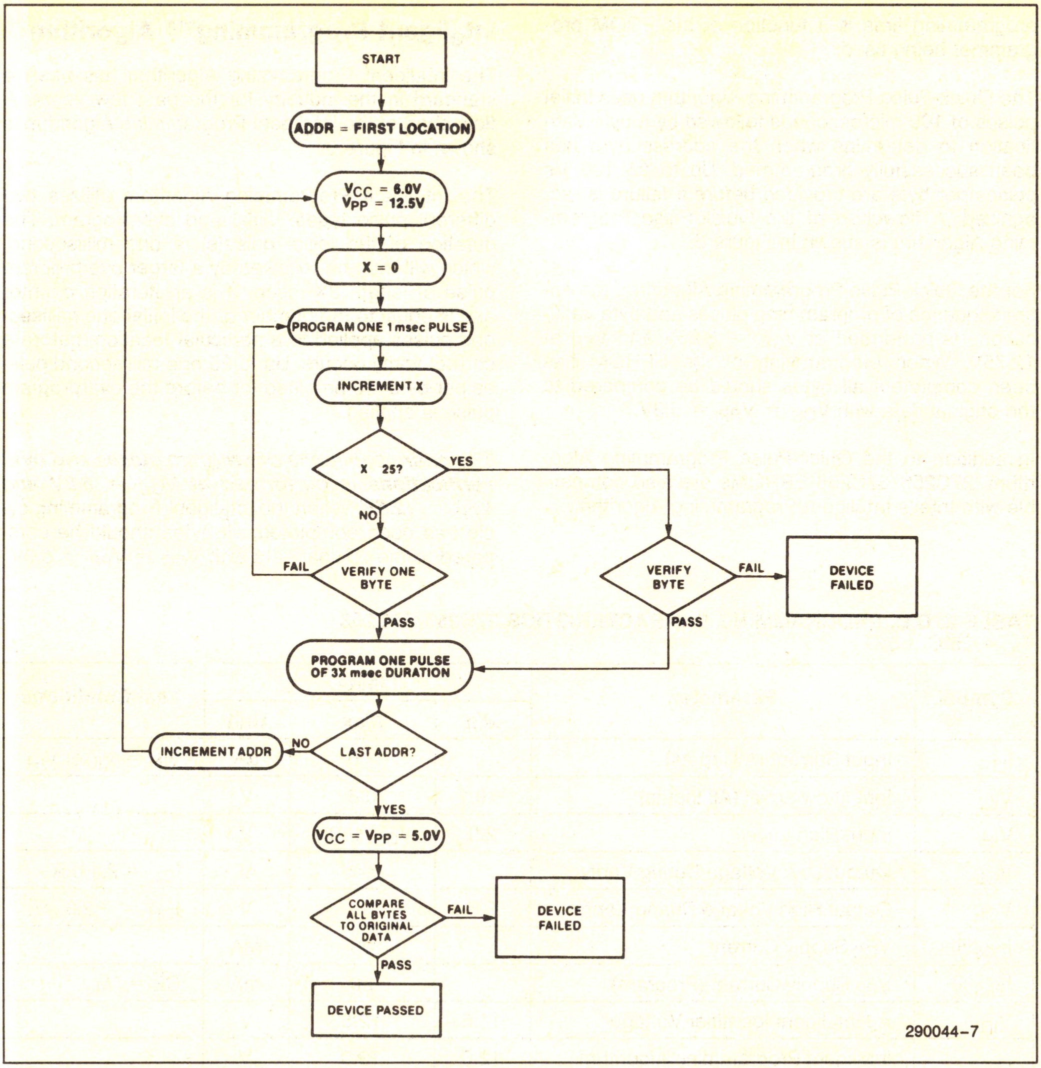

START
ADDR = FIRST LOCATION
V_{CC} = 6.0V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
V_{CC} = V_{PP} = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
290044–7

Figure 6. int$_e$ligent Programming™ Flowchart

grated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from -1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

Quick-Pulse Programming™ Algorithm

Intel's 27C256 EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is preformed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, 27C256/87C256 EPROMs are also compatible with Intel's Int$_e$ligent Programming Algorithm.

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 6.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS 27C256/87C256
T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	3.5		V	I_{OH} = −2.5 mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 Int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 27C256/87C256

T_A = 25°C ±5°C; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse
		0.95	1.0	1.05	ms	int$_e$ligent
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(See Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	
t_{CE}	$\overline{CE}$ to Output Delay			500	ns	Optional Verify
t_{VR}	V_{PP} Recovery Time	2			μs	Optional Verify
t_{VPH}	V_{PP} Hold Time	2			μs	Optional Verify

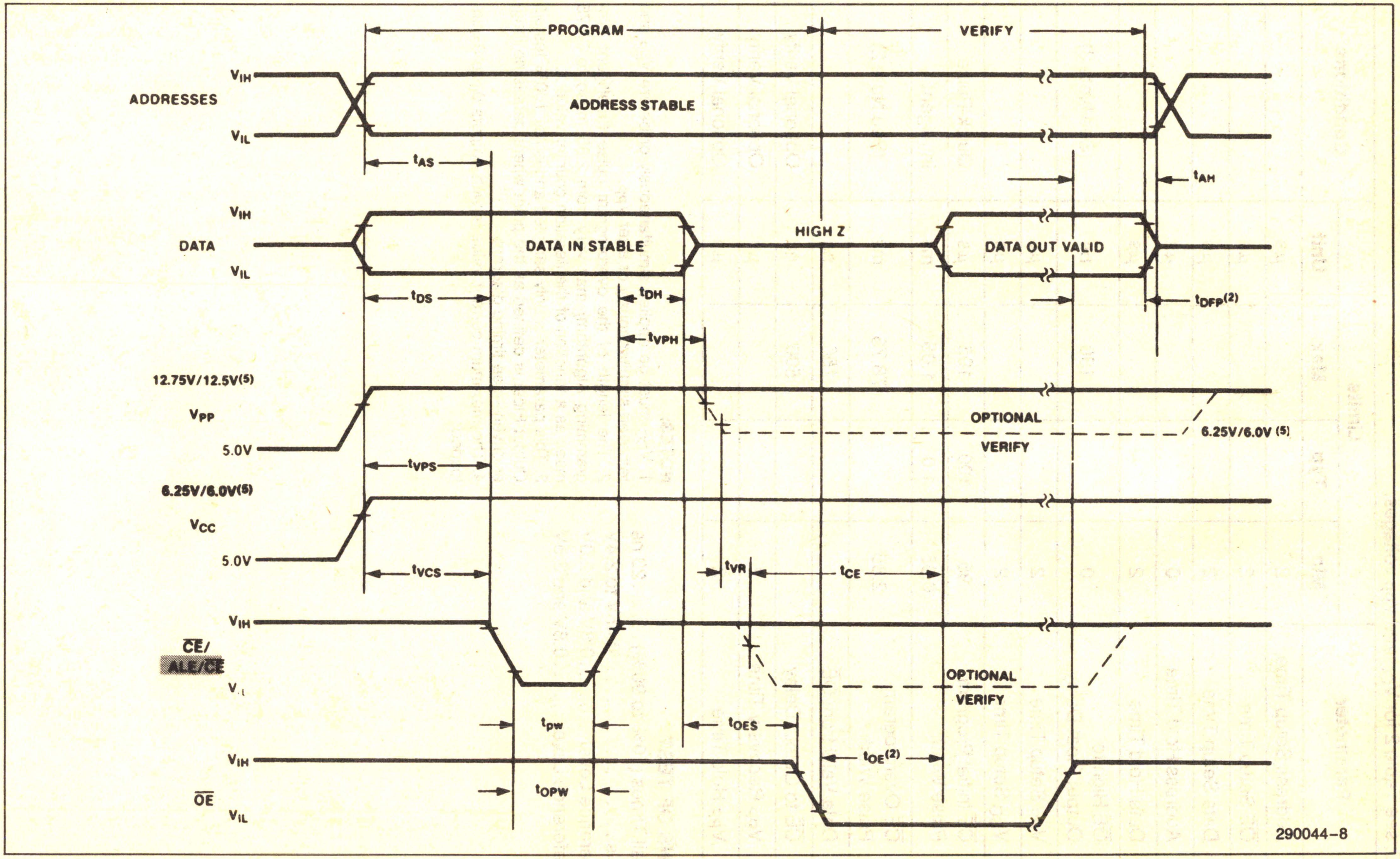
A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 3.5V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (Intelligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS 27C256/87C256


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
$t_{DFP}^{(2)}$
t_{VPH}
12.75V/12.5V(5)
V_{PP}
5.0V
OPTIONAL VERIFY
6.25V/6.0V (5)
t_{VPS}
6.25V/6.0V(5)
V_{CC}
5.0V
t_{VCS}
t_{VR}
t_{CE}
$\overline{CE}$/ ALE/$\overline{CE}$
OPTIONAL VERIFY
t_{PW}
t_{OES}
$t_{OE}^{(2)}$
$\overline{OE}$
t_{OPW}

290044–8

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C256/87C256, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. When programming the 87C256, the address latch function is bypassed with V_{PP} at 12.5V. The device will function just like the 27C256 during read or write. When V_{PP} is at 5.0V during the read mode, the address latch function is enabled and $\overline{CE}$ needs to be toggled to latch in the addresses.
5. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27512

512K (64K x 8) PRODUCTION AND UV ERASABLE PROM

- **Software Carrier Capability**
- **170 ns Maximum Access Time**
- **Two-Line Control**
- **inteligent Identifier™ Mode**
  - **— Automated Programming Operations**
- **TTL Compatible**
- **Low Power**
  - **— 125 mA max. Active**
  - **— 40 mA max. Standby**
- **New Quick-Pulse Programming™ Algorithm**
  - **— 8 Second Programming**
  - **— inteligent Programming™ Algorithm Compatible**
- **Available in 28-Pin Cerdip, Plastic DIP and 32-Lead PLCC Packages**

  (See packaging spec order #231369)

The Intel 27512 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 64K words by 8 bits, individual bytes are accessed in under 170 ns. This ensures compatibility with high-performance microprocessors, such as the Intel 8 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27512 is also directly compatible with Intel's 8051 family of microcontrollers.

The 27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

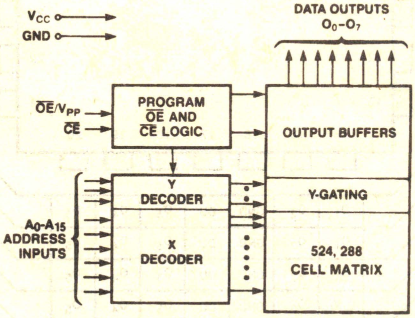
The 27512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27512 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The Plastic P27512 and PLCC N27512 are ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27512 and the N27512 to be programmed within eight seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the inteligent Identifier and rapidly program it using a superior programming method. The inteligent Programming Algorithm may be utilized in the absence of such equipment.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27512 is manufactured using Intel's advanced HMOS *II-E technology.

*HMOS is a patented process of Intel Corporation.



231088-1

Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986

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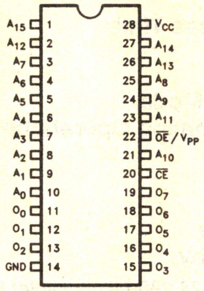
Order Number: 231088-005

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Outputs Enable/V_{PP}
O_0–O_7	Outputs
D.U.	Don't Use

27513	27256 27C256 87C256	27128 27128A	2764 2764A 27C64 87C64
D.U.	V_{PP}	V_{PP}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	O_0	O_0	O_0
D_1/O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

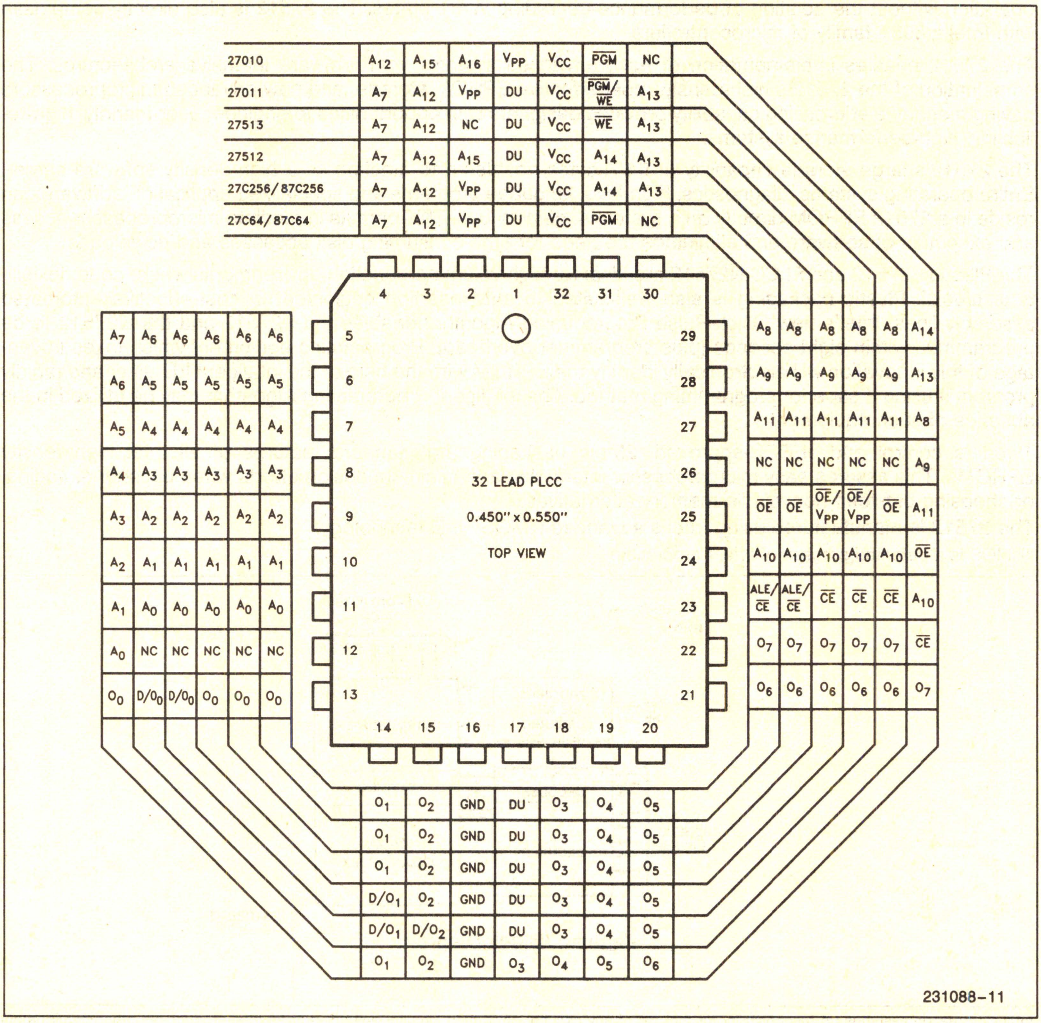
27512
P27512


A_{15} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
GND 14
28 V_{CC}
27 A_{14}
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}/V_{PP}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

2764 2764A 27C64 87C64	27128 27128A	27256 27C256 87C256	27513
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$	A_{14}	$\overline{WE}$
N.C.	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

231088–2

Figure 2. Pin Configurations


32 LEAD PLCC
0.450" x 0.550"
TOP VIEW

	4	3	2	1	32	31	30
27010	A_{12}	A_{15}	A_{16}	V_{PP}	V_{CC}	$\overline{PGM}$	NC
27011	A_7	A_{12}	V_{PP}	DU	V_{CC}	$\overline{PGM}/\overline{WE}$	A_{13}
27513	A_7	A_{12}	NC	DU	V_{CC}	$\overline{WE}$	A_{13}
27512	A_7	A_{12}	A_{15}	DU	V_{CC}	A_{14}	A_{13}
27C256/87C256	A_7	A_{12}	V_{PP}	DU	V_{CC}	A_{14}	A_{13}
27C64/87C64	A_7	A_{12}	V_{PP}	DU	V_{CC}	$\overline{PGM}$	NC

A_7	A_6	A_6	A_6	A_6	A_6	5
A_6	A_5	A_5	A_5	A_5	A_5	6
A_5	A_4	A_4	A_4	A_4	A_4	7
A_4	A_3	A_3	A_3	A_3	A_3	8
A_3	A_2	A_2	A_2	A_2	A_2	9
A_2	A_1	A_1	A_1	A_1	A_1	10
A_1	A_0	A_0	A_0	A_0	A_0	11
A_0	NC	NC	NC	NC	NC	12
O_0	D/O_0	D/O_0	O_0	O_0	O_0	13

29	A_8	A_8	A_8	A_8	A_8	A_{14}
28	A_9	A_9	A_9	A_9	A_9	A_{13}
27	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_8
26	NC	NC	NC	NC	NC	A_9
25	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	A_{11}
24	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	$\overline{OE}$
23	ALE/$\overline{CE}$	ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	A_{10}
22	O_7	O_7	O_7	O_7	O_7	$\overline{CE}$
21	O_6	O_6	O_6	O_6	O_6	O_7

14	15	16	17	18	19	20
O_1	O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	DU	O_3	O_4	O_5
D/O_1	O_2	GND	DU	O_3	O_4	O_5
D/O_1	D/O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	O_3	O_4	O_5	O_6

231088–11

Figure 3. PLCC (N) Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hours, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27512 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-170V05, -170V10	Q, L
-200V05, -200V10	Q, L
-STD, -25	Q, T, L
-3, -30	Q, T, L

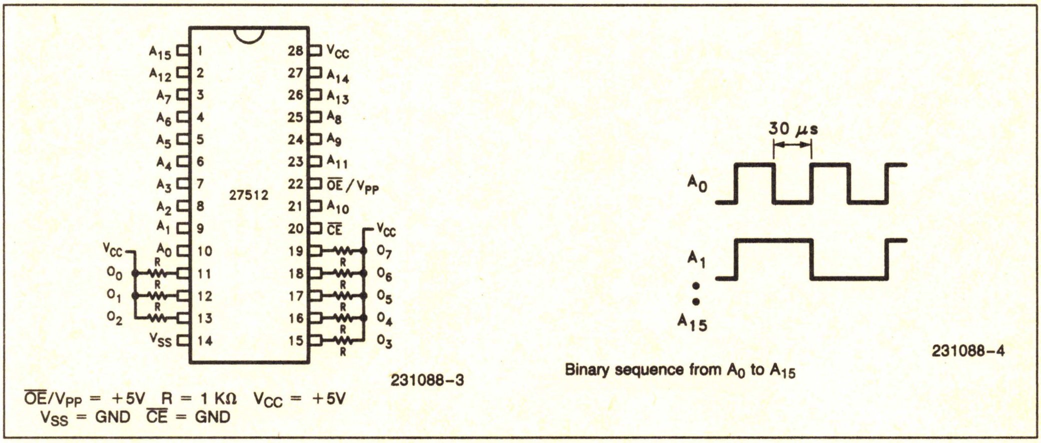
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27512 LD27512		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



A_{15} 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
O_0 11
O_1 12
O_2 13
V_{SS} 14
28 V_{CC}
27 A_{14}
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}/V_{PP}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3
27512
V_{CC}
R
231088-3
$\overline{OE}/V_{PP}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{SS} = GND $\overline{CE}$ = GND
30 μs
A_0
A_1
A_{15}
Binary sequence from A_0 to A_{15}
231088-4

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature during Read . . . . 0°C to 70°C

Temperature Under Bias . . . . −10°C to +80°C

Storage Temperature . . . . −65°C to +125°C

All Input or Output Voltages with Respect to Ground . . . . −0.6V to +6.5V

Voltage on Pin 24 with Respect to Ground . . . . −0.6V to +13.5V

$\overline{OE}/V_{PP}$ Supply Voltage with Respect to Ground . . . . −0.6V to +14.0V

V_{CC} Supply Voltage with Respect to Ground . . . . −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC_1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(5, 6)	V_{CC} ±5%	27512-170V05		27512-2 27512-200V05 P27512-200V05 N27512-200V05		27512 P27512 27512-250V05 P27512-250V05		27512-3 P27512-3 N27512-3		Units	Test Conditions
	V_{CC} ±10%	27512-170V10		27512-20 27512-200V10 P27512-200V10 N27512-200V10		27512-25 P27512-25 N27512-25		27512-30 P27512-30 N27512-30			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
t_{ACC}	Address to Output Delay		170		200		250		300	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250		300	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		60		75		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float	0	50	0	55	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$ Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

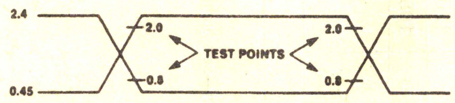
NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging options: No prefix = Cerdip; P = Plastic DIP; N = PLCC.
6. All products with the 6-digit speed identifier are produced on compacted HMOS II-E technology.

CAPACITANCE[2] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ[1]	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{\overline{OE}}/V_{PP}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	$V_{IN} = 0V$

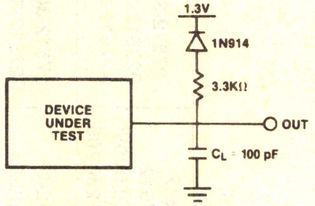
A.C. TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8

231088-5

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

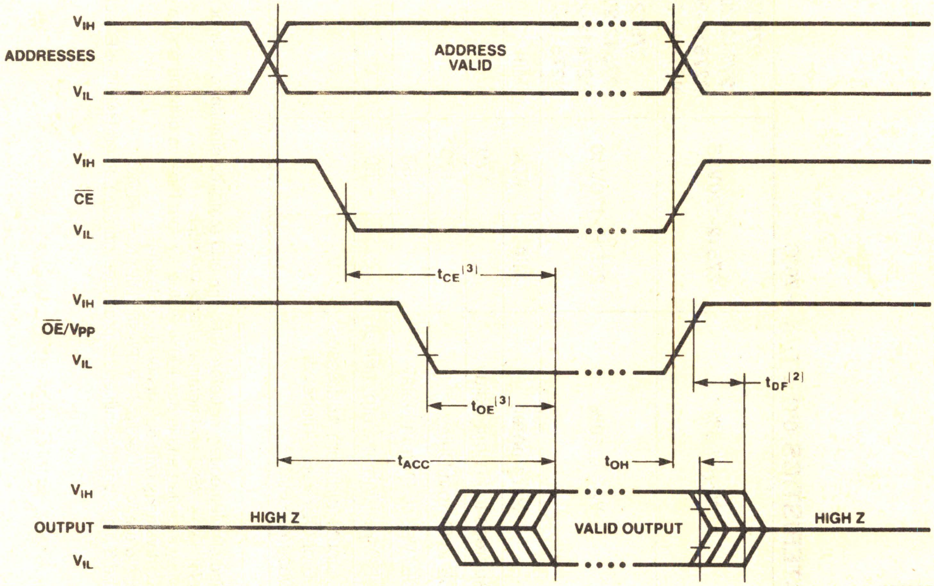
A.C. TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

C_L = 100 pF
C_L Includes Jig Capacitance

231088-6

A.C. WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}(3)
V_{IH}
$\overline{OE}/V_{PP}$
V_{IL}
t_{DF}(2)
t_{OE}(3)
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z

231088-7

NOTES:

1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27512 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for OE/V_{PP} and 12V on A9 for int$_{e}$ligent identifier mode.

Read Mode

The 27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$/V_{PP}) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 27512 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27512 is placed in the standby mode by applying a TTL-high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$/V_{PP} input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{\text{CE}}$ should be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$/V_{PP} should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

Table 1. Operating Modes

Pins	$\overline{\text{CE}}$	$\overline{\text{OE}}$/V_{PP}	A_9	A_0	V_{CC}	Outputs
Mode						
Read	V_{IL}	V_{IL}	X(1)	X	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}(3)	X	X	6.0V	D_{IN}
Verify	V_{IL}	V_{IL}	X	X	6.0V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	X	X	6.0V	High Z
Int$_{e}$ligent —Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	5.0V	89H
Identifier(4) —Device	V_{IL}	V_{IL}	V_H(2)	V_{IH}	5.0V	0DH

NOTES:

1. X can be V_{IH} or V_{IL}.
2. V_H = 12.0V ±0.5V.
3. V_{PP} = 12.5 ±0.5V.
4. A_1–A_8, A_{10}–A_{13} = V_{IL}; A_{14}, A_{15} = V_{IH}.

PROGRAMMING MODES

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 25712s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27512s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27512s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27512.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode, except for A14 and A15 which should be held high.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm (for Plastic and PLCC EPROMs), the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intelec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using

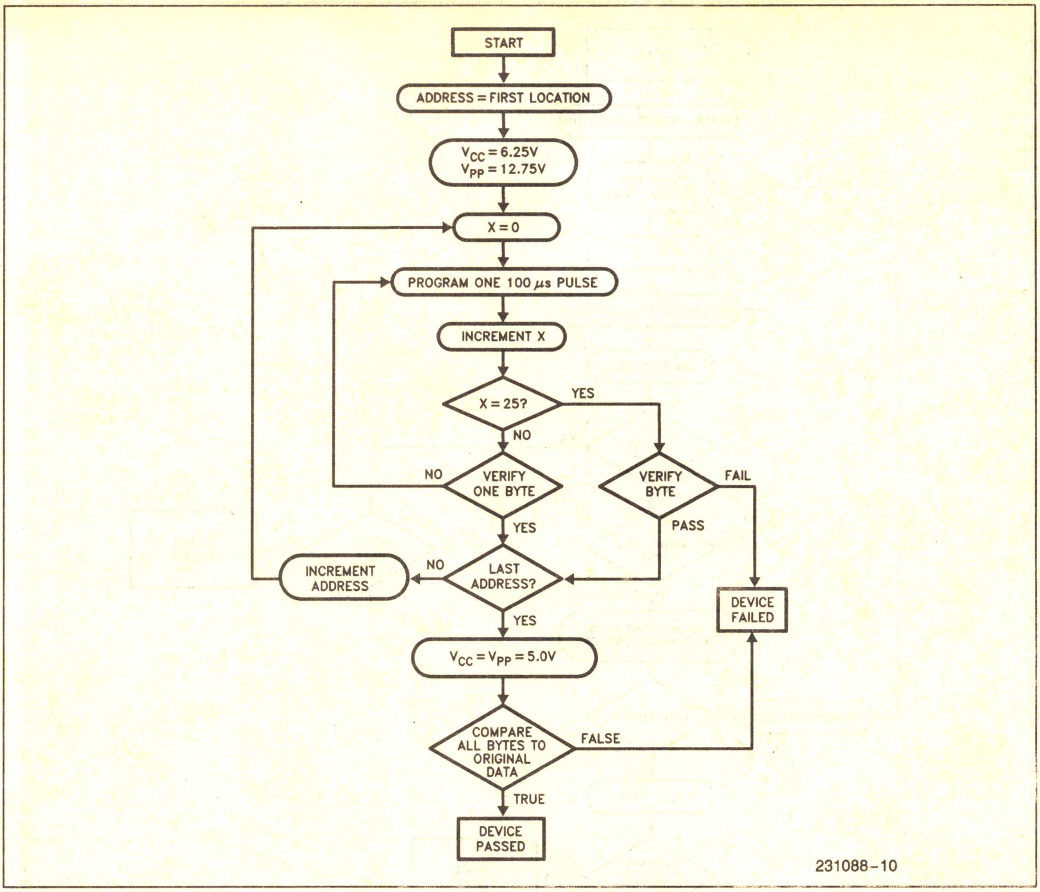

START
ADDRESS = FIRST LOCATION
VCC = 6.25V
VPP = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
NO
YES
VERIFY BYTE
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FALSE
TRUE
DEVICE PASSED
231088-10

Figure 4. Quick-Pulse Programming™ Algorithm

an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

Quick-Pulse Programming™ Algorithm (For Plastic and PLCC EPROMs)

Intel's Plastic and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows both Plastic and PLCC devices to be programmed in under eight seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses fo 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP}$ = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic and PLCC EPROMs are also compatible with Intel's int$_{e}$ligent Programming Algorithm.

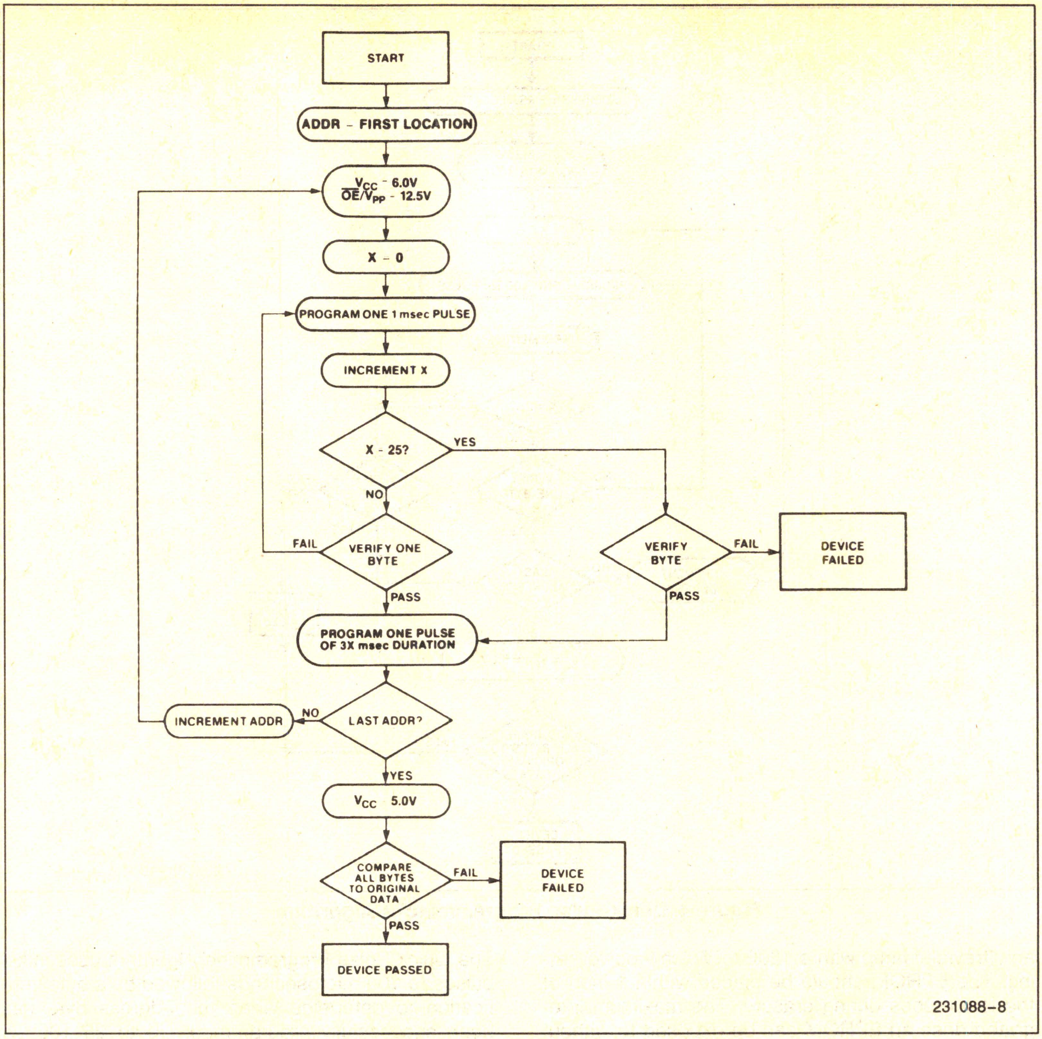

START
ADDR - FIRST LOCATION
V_{CC} - 6.0V
$\overline{OE}/V_{PP}$ - 12.5V
X - 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X - 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
V_{CC} 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
231088-8

Figure 5. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm rapidly programs Intel EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming time for individual devices are on the order of six minutes. Actual programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		125	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			μs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
		0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

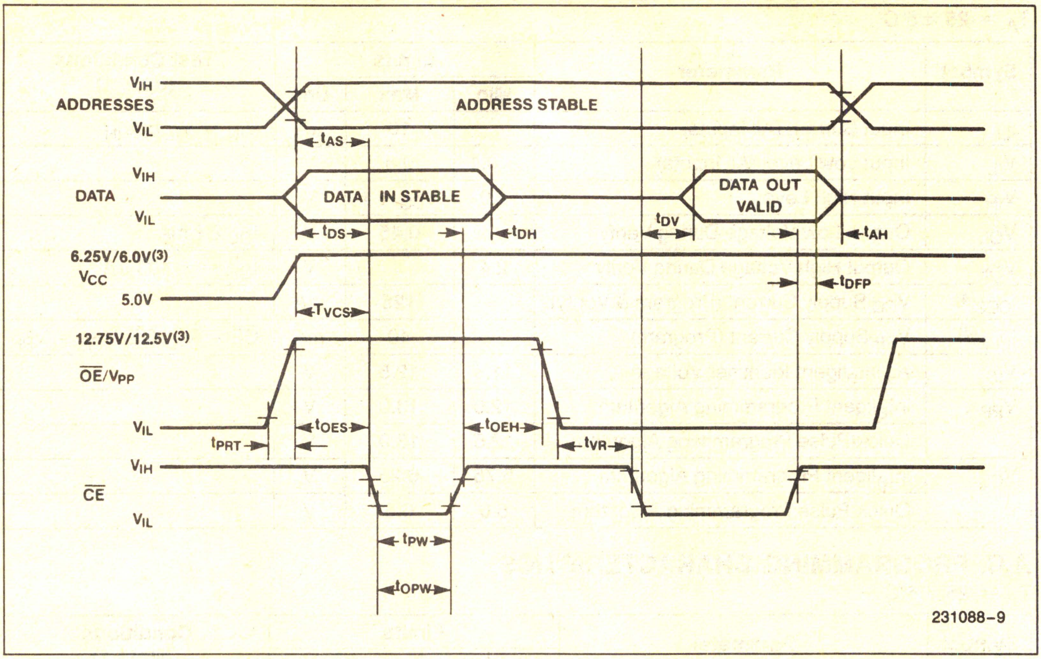
***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ...... 20 ns
Input Pulse Levels .... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V and 2.0V
Output Timing Reference Level ...... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
V_{IH}
DATA
V_{IL}
DATA IN STABLE
DATA OUT VALID
t_{DS}
t_{DH}
t_{DV}
t_{AH}
6.25V/6.0V(3)
V_{CC}
5.0V
t_{DFP}
T_{VCS}
12.75V/12.5V(3)
$\overline{OE}/V_{PP}$
V_{IL}
t_{PRT}
t_{OES}
t_{OEH}
t_{VR}
V_{IH}
$\overline{CE}$
V_{IL}
t_{PW}
t_{OPW}
231088–9

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27513
PAGE-ADDRESSED 512K (4 x 16K x 8) PRODUCTION AND UV ERASABLE PROM

- **Paged Organization**
  - **Reduced Physical Address Requirement**
  - **No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **Resets to Page 0 on Power Up and On Demand with $\overline{\text{RST}}$ Signal**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **125 mA max. Active**
  - **40 mA max. Standby**
- **New Quick-Pulse Programming™ Algorithm**
  - **8 Second Programming**
  - **int$_e$ligent Programming™ Algorithm Compatible**
- **Compatible with Industry Standard EPROM Pinouts**
  - **Direct 27128A Compatibility**
  - **28-Pin Cerdip and Plastic Packages**
  - **32-Lead PLCC Package**

  (See Packaging Spec, Order #231369)

The Intel 27513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27513's paged organization brings 64 K-byte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 K-byte total addressing capability. The 27513 provides an ideal means of quadrupling current 16 K-byte code space.

The 27513's large storage capability of 64 K-bytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The P27513 and PLCC N27512 are ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. The P27513 and the N27512 enable implementation of new, advanced systems with firmware-intensive architectures. The combination of the P27513's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The 27513 enables firmware-intensive performance upgrades for systems based on microprocessors with 64K physical addressing capability like the 8085AH.

The 27513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

The 27513 has a fast access time. Individual bytes are accessed in under 170 ns. Intel's new Quick-Pulse Programming Algorithm enables the 27513 to be programmed within eight seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27513 is manufactured using Intel's Compacted HMOS* II technology.

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* HMOS is a patented process of Intel Corporation

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

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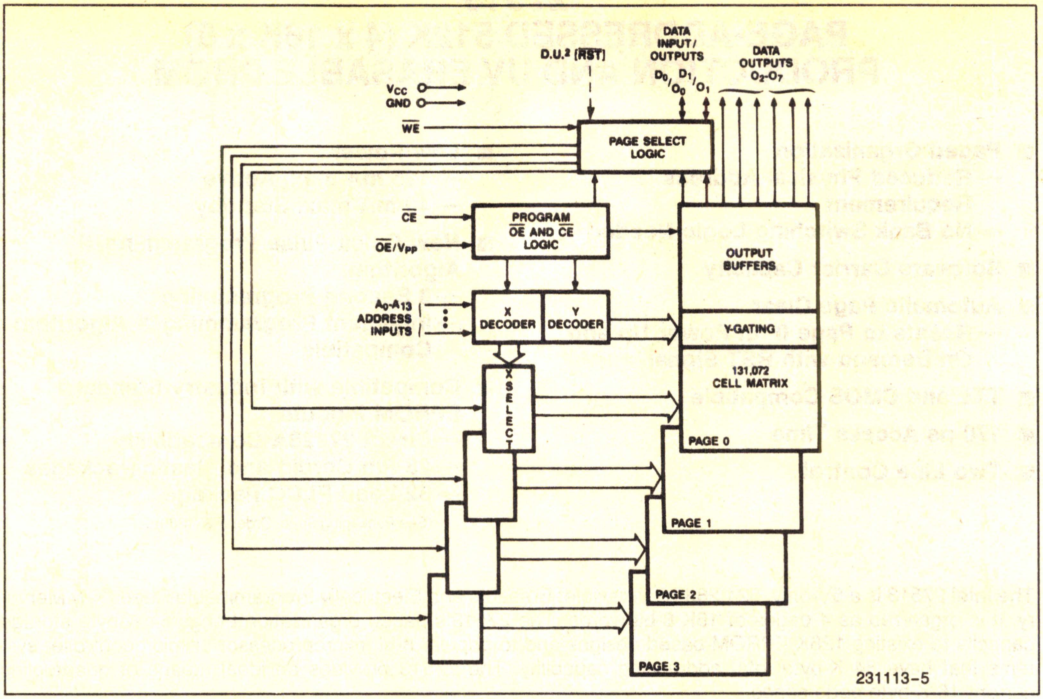
Order Number: 231113-005

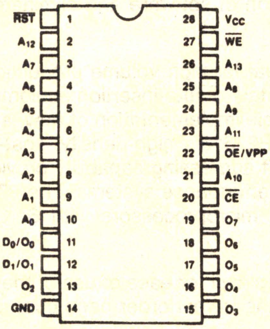

D.U.^{2} ($\overline{RST}$)
DATA INPUT/ OUTPUTS
D_0/O_0
D_1/O_1
DATA OUTPUTS
O_2-O_7
V_{CC}
GND
$\overline{WE}$
PAGE SELECT LOGIC
$\overline{CE}$
$\overline{OE}/V_{PP}$
PROGRAM $\overline{OE}$ AND $\overline{CE}$ LOGIC
OUTPUT BUFFERS
A_0-A_{13} ADDRESS INPUTS
X DECODER
Y DECODER
Y-GATING
131,072 CELL MATRIX
X SELECT
PAGE 0
PAGE 1
PAGE 2
PAGE 3

231113-5

Figure 1. Block Diagram

2732A	2764A	27128A	27256	27512
	V_{PP}	V_{PP}	V_{PP}	A_{15}
	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27513
P27513


$\overline{RST}$
1
A_{12}
2
A_7
3
A_6
4
A_5
5
A_4
6
A_3
7
A_2
8
A_1
9
A_0
10
D_0/O_0
11
D_1/O_1
12
O_2
13
GND
14
28
V_{CC}
27
$\overline{WE}$
26
A_{13}
25
A_8
24
A_9
23
A_{11}
22
$\overline{OE}$/VPP
21
A_{10}
20
$\overline{CE}$
19
O_7
18
O_6
17
O_5
16
O_4
15
O_3

27512	27256	27128A	2764A	2732A
V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$	
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

231113-6

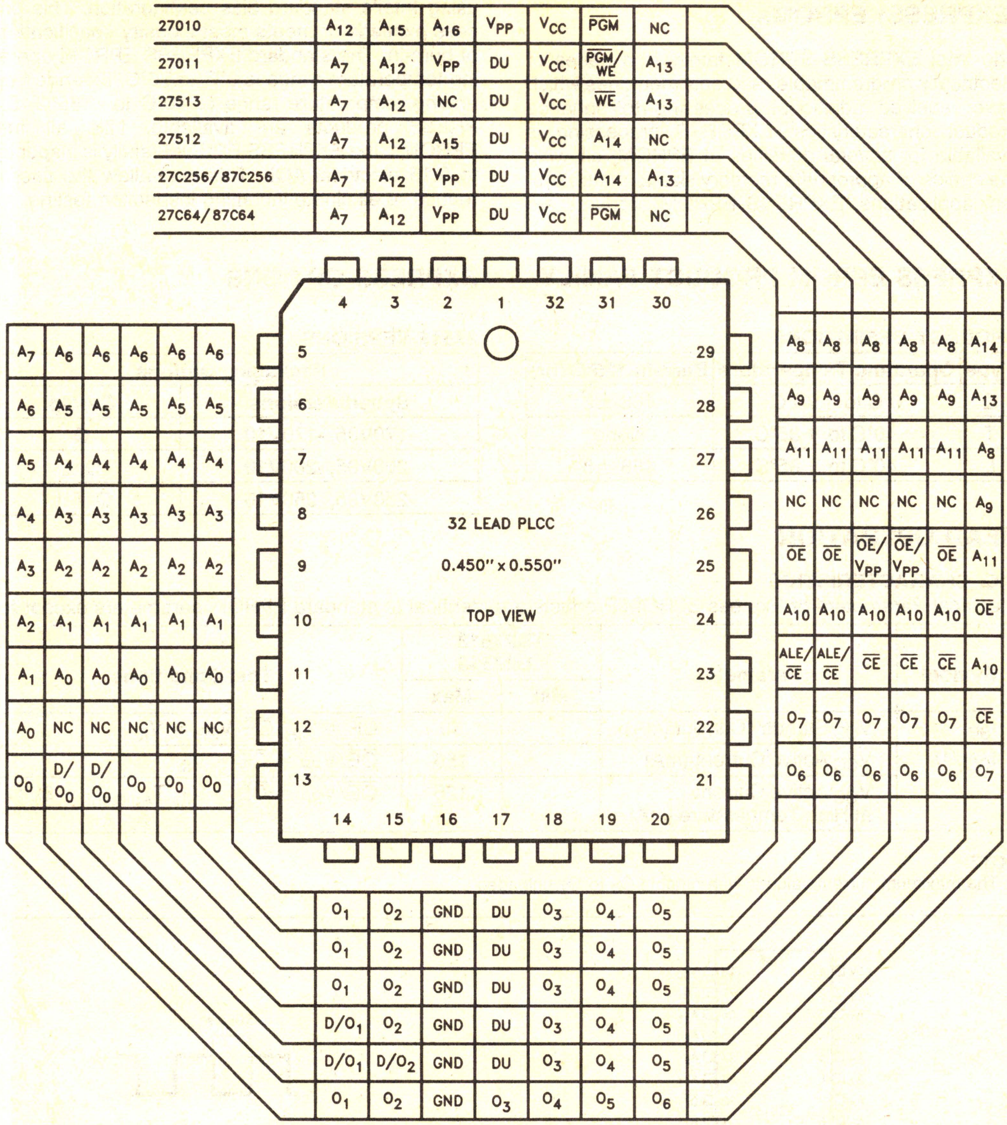
Figure 2. Pin Configuration

NOTES:

1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page-Select Write Enable
O_2–O_7	Outputs
D_0/O_0,D_1/O_1	Input/Outputs
$\overline{RST}$	Page Reset



27010	A_{12}	A_{15}	A_{16}	V_{PP}	V_{CC}	$\overline{PGM}$	NC
27011	A_7	A_{12}	V_{PP}	DU	V_{CC}	$\overline{PGM}/\overline{WE}$	A_{13}
27513	A_7	A_{12}	NC	DU	V_{CC}	$\overline{WE}$	A_{13}
27512	A_7	A_{12}	A_{15}	DU	V_{CC}	A_{14}	NC
27C256/87C256	A_7	A_{12}	V_{PP}	DU	V_{CC}	A_{14}	A_{13}
27C64/87C64	A_7	A_{12}	V_{PP}	DU	V_{CC}	$\overline{PGM}$	NC

A_7	A_6	A_6	A_6	A_6	A_6
A_6	A_5	A_5	A_5	A_5	A_5
A_5	A_4	A_4	A_4	A_4	A_4
A_4	A_3	A_3	A_3	A_3	A_3
A_3	A_2	A_2	A_2	A_2	A_2
A_2	A_1	A_1	A_1	A_1	A_1
A_1	A_0	A_0	A_0	A_0	A_0
A_0	NC	NC	NC	NC	NC
O_0	D/ O_0	D/ O_0	O_0	O_0	O_0

A_8	A_8	A_8	A_8	A_8	A_{14}
A_9	A_9	A_9	A_9	A_9	A_{13}
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_8
NC	NC	NC	NC	NC	A_9
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	A_{11}
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	$\overline{OE}$
ALE/ $\overline{CE}$	ALE/ $\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	A_{10}
O_7	O_7	O_7	O_7	O_7	$\overline{CE}$
O_6	O_6	O_6	O_6	O_6	O_7

O_1	O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	DU	O_3	O_4	O_5
D/O_1	O_2	GND	DU	O_3	O_4	O_5
D/O_1	D/O_2	GND	DU	O_3	O_4	O_5
O_1	O_2	GND	O_3	O_4	O_5	O_6

4
3
2
1
32
31
30
5
6
7
8
9
10
11
12
13
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27
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24
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22
21
14
15
16
17
18
19
20
32 LEAD PLCC
0.450" x 0.550"
TOP VIEW
231113-13

Figure 3. PLCC (N) Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27513 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-170V05, -170V10	Q
-200V05, -200V10	Q, L
-250V05, -250V10	Q, T, L

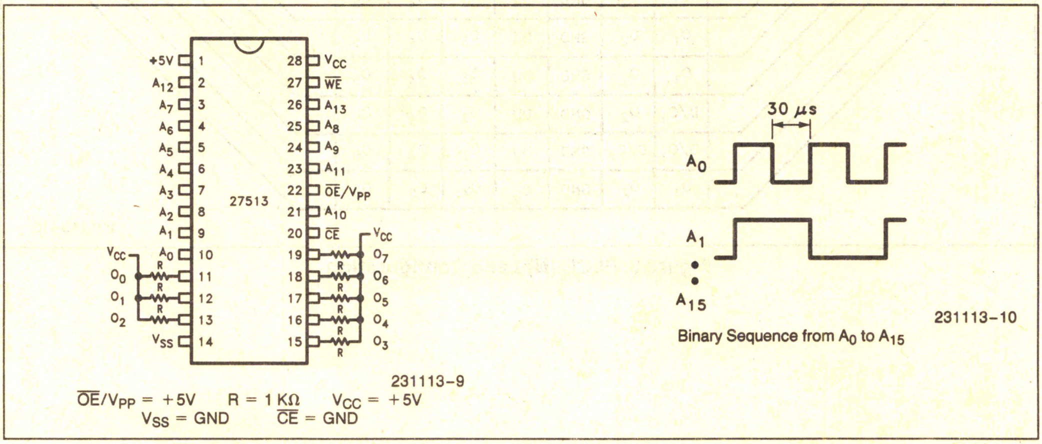
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27513 LD27513		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.


+5V
A12
A7
A6
A5
A4
A3
A2
A1
A0
VSS
VCC
O0
O1
O2
R
1
2
3
4
5
6
7
8
9
10
11
12
13
14
27513
28
27
26
25
24
23
22
21
20
19
18
17
16
15
VCC
WE
A13
A8
A9
A11
OE/VPP
A10
CE
VCC
O7
O6
O5
O4
O3
231113-9
OE/VPP = +5V
R = 1 KΩ
VCC = +5V
VSS = GND
CE = GND
30 μs
A0
A1
A15
231113-10
Binary Sequence from A0 to A15

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .... 0°C to +70°C
Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† .... −0.6V to +6.5V
Voltage on Pin 24 with
Respect to Ground .... −0.6V to +13.5V
$\overline{OE}/V_{PP}$ Supply Voltage with
Respect to Ground .... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground .... −0.6V to +7.0V

† includes Don't Connect (pin 1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ AND PAGE-SELECT WRITE OPERATIONS

D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage		3.5	4.0	V	

READ OPERATION

A.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Versions(5)	V_{CC} ±5%	27512-170V05		27512-200V05 P27512-200V05 N27512-200V05		27512-250V05 P27512-250V05 N27512-250V05		Units	Test Conditions
	V_{CC} ±10%	27512-170V10 P27512-170V10 N27512-170V10		27512-200V10 P27512-200V10 N27512-200V10		27512-250V10 P27512-250V10 N27512-250V10			
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		170		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		60		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float	0	50	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

A.C. CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	250		ns	
t_{RAV}	Reset to Address Valid	250		ns	

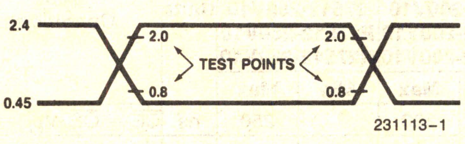
NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

CAPACITANCE(2) $T_A = +25°C$, f = 1 MHz

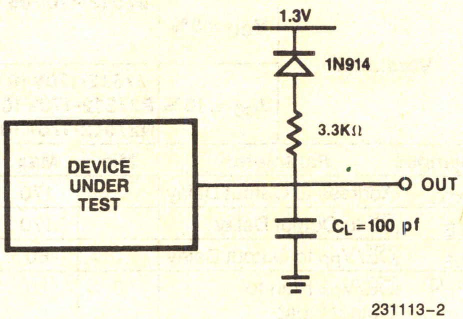
Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	$V_{IN} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM



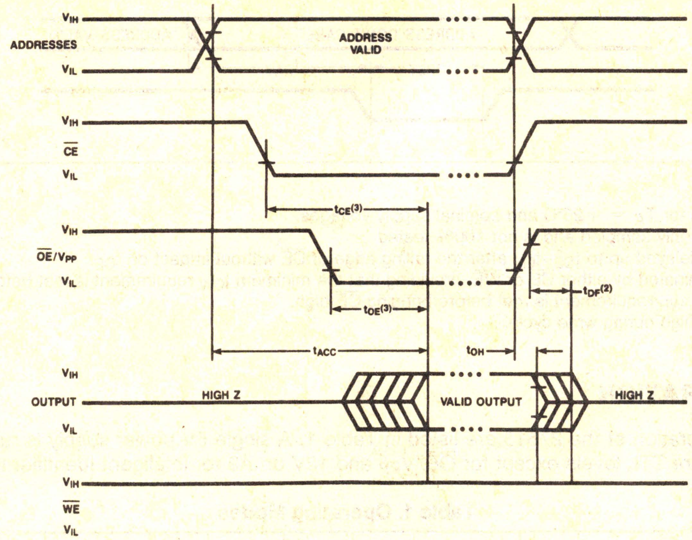
AC Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

A.C. TESTING LOAD CIRCUIT



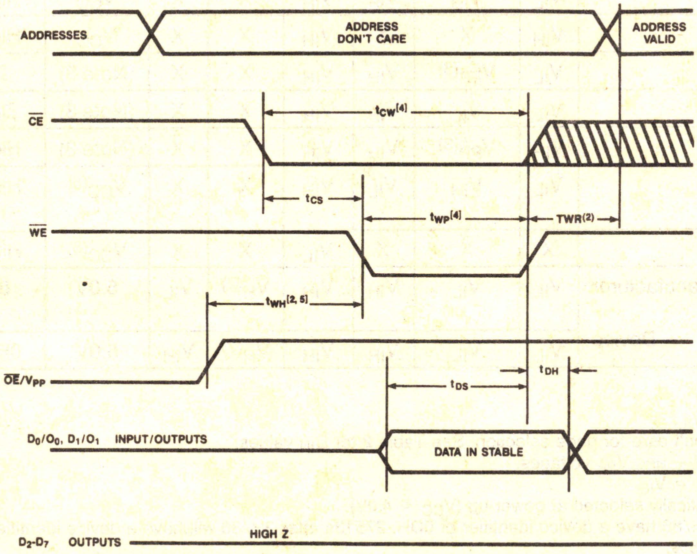
C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE(3)
V_IH
OE/V_PP
V_IL
t_OE(3)
t_DF(2)
t_ACC
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
V_IH
WE
V_IL

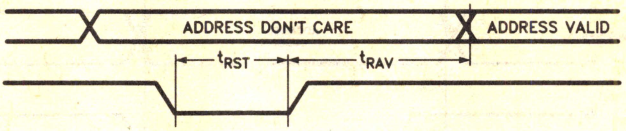
231113-3

A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION


ADDRESSES
ADDRESS DON'T CARE
ADDRESS VALID
CE
t_CW[4]
t_CS
t_WP[4]
TWR(2)
WE
t_WH[2, 5]
OE/V_PP
t_DH
t_DS
D0/O0, D1/O1 INPUT/OUTPUTS
DATA IN STABLE
D2-D7 OUTPUTS
HIGH Z

231113-4

A.C. WAVEFORMS FOR PAGE-RESET OPERATIONS



231113-12

NOTES:

1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}/V_{PP}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for int$_e$ligent Identifier mode.

Table 1. Operating Modes

Pins Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A_9	A_0	V_{CC}	Outputs	Input/Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X(1)	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC}(5)	High Z	Page(2) D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC}(5)	High Z	X
int$_e$ligent(4) —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IL}	5.0V	89H	89H(8) 88H(8)
Identifier —Device	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IH}	5.0V	0FH(6)	0FH(6)

NOTES:

1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. 27513s before 2H/86 have a device identifier of 0DH. 27513s after 2H/86 will have a device identifier of 0FH.
7. $V_H = 12.0V \pm 0.5\%$.
8. The manufacturer's identifier reads 89H for Cerdip devices; 88H for Plastic devices.

Read Mode

The 27513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

The 27513 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27513 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27513 is addressed by first selecting one of four 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case −10% V_{CC} supply condition) against spurious page latch clearing.

The 27513 also has a page reset pin: $\overline{RST}$. This pin should be tied to an active low system reset signal. The 27513 will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27513s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the 27513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27513s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27513s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int_eligent Identifier™ Mode

The int$_{e}$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_{e}$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm (for plastic and PLCC EPROMs), the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPs makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intelec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

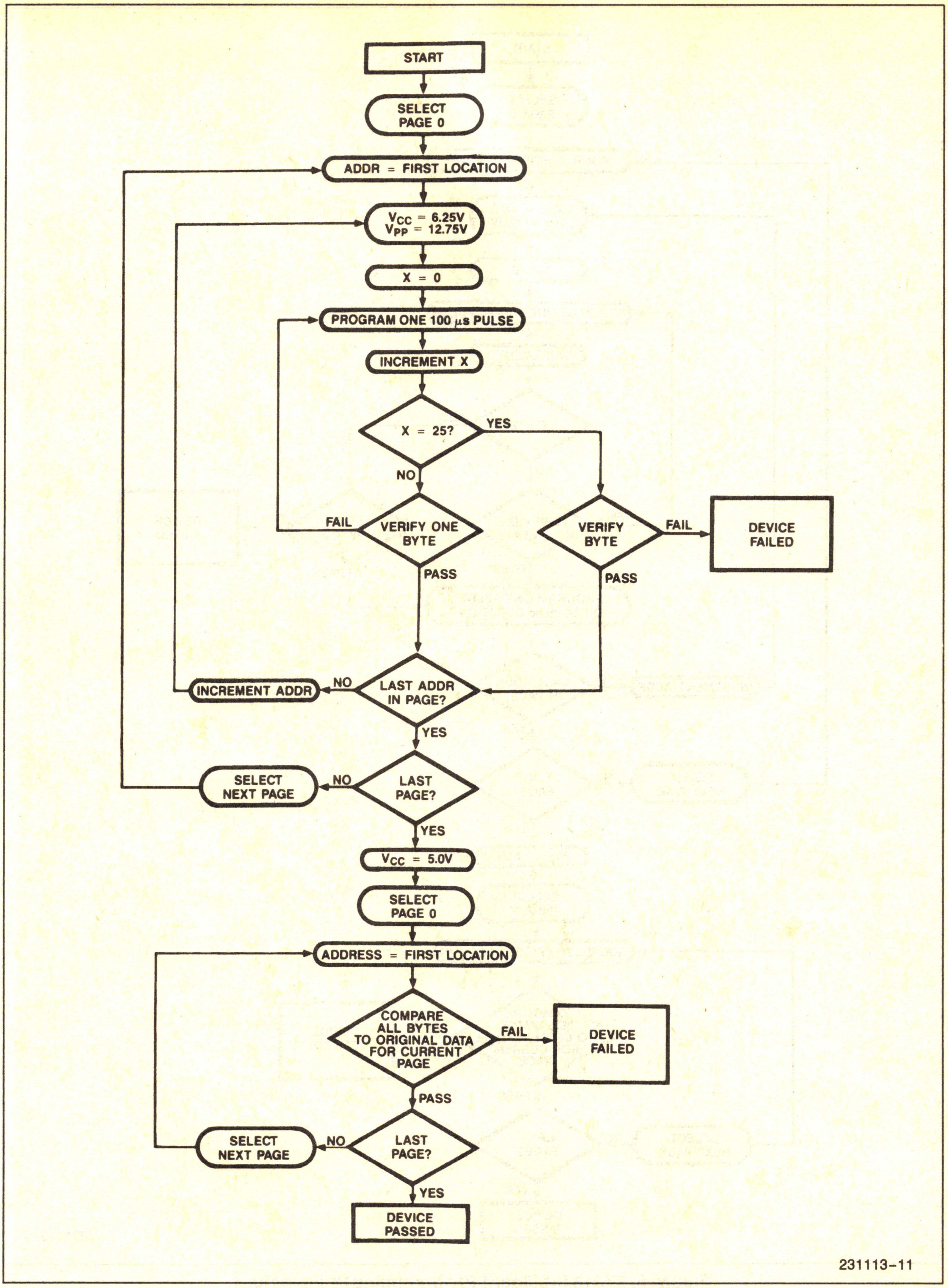

START
SELECT PAGE 0
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
INCREMENT ADDR
NO
LAST ADDR IN PAGE?
YES
SELECT NEXT PAGE
NO
LAST PAGE?
YES
V_{CC} = 5.0V
SELECT PAGE 0
ADDRESS = FIRST LOCATION
COMPARE ALL BYTES TO ORIGINAL DATA FOR CURRENT PAGE
FAIL
DEVICE FAILED
PASS
SELECT NEXT PAGE
NO
LAST PAGE?
YES
DEVICE PASSED
231113-11

Figure 4. 27513 Quick-Pulse Programming™ Flowchart

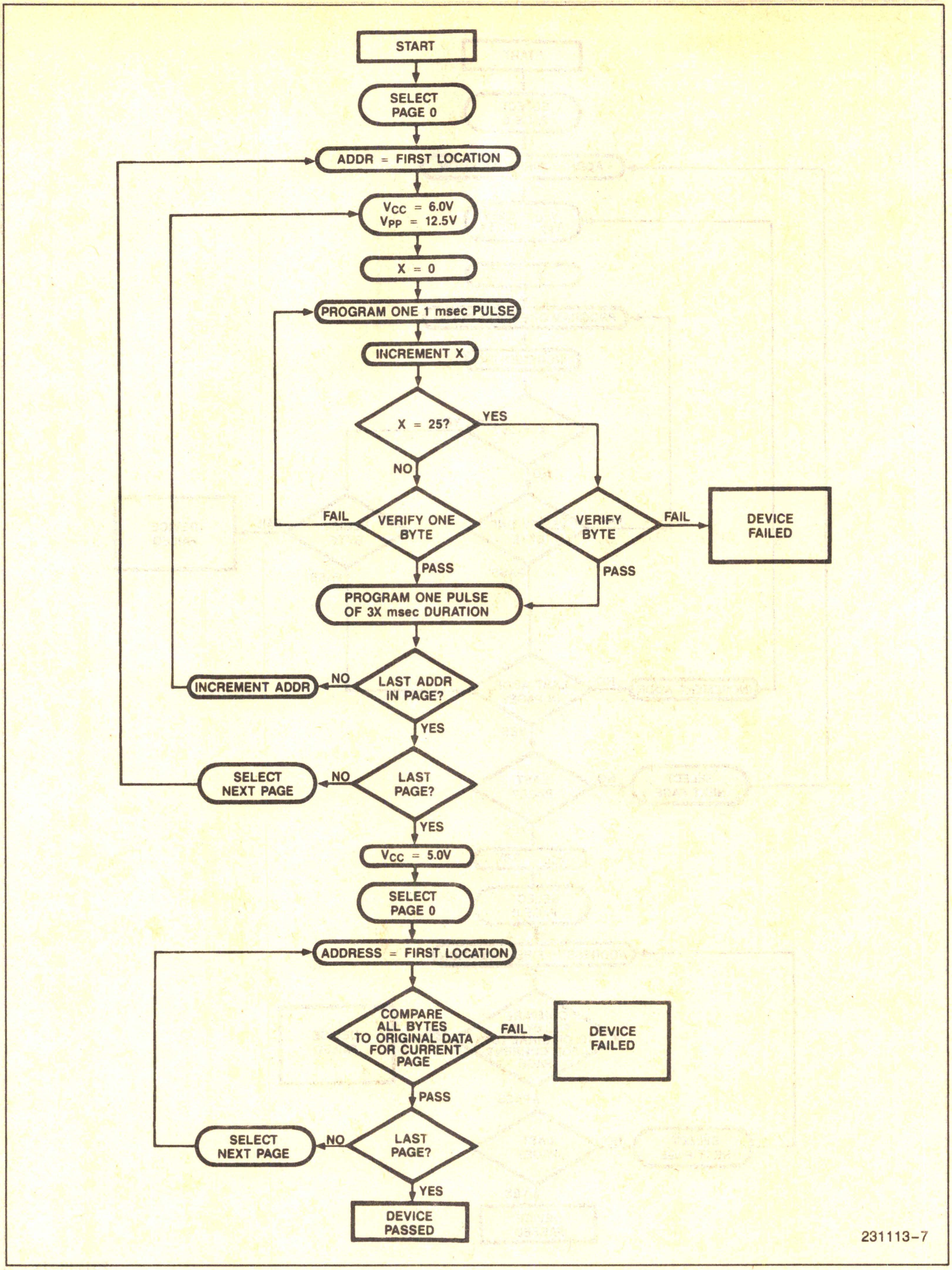

START
SELECT PAGE 0
ADDR = FIRST LOCATION
VCC = 6.0V
VPP = 12.5V
X = 0
PROGRAM ONE 1 msec PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X msec DURATION
INCREMENT ADDR
NO
LAST ADDR IN PAGE?
YES
SELECT NEXT PAGE
NO
LAST PAGE?
YES
VCC = 5.0V
SELECT PAGE 0
ADDRESS = FIRST LOCATION
COMPARE ALL BYTES TO ORIGINAL DATA FOR CURRENT PAGE
FAIL
DEVICE FAILED
PASS
SELECT NEXT PAGE
NO
LAST PAGE?
YES
DEVICE PASSED
231113-7

Figure 5. 27513 int$_e$ligent Programming™ Flowchart

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

Quick Pulse Programming™ Algorithm (For Plastic and PLCC EPROMs)

Intel's Plastic and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows both Plastic and PLCC devices to be programmed in under eight seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

In addition to the Quick-Pulse Programming Algorithm, Plastic and PLCC EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\ \mu$A
I_{CC2}(2)	V_{CC} Supply Current (Program and Verify)		125	mA	
I_{PP2}(2)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0–O_7 unloaded.

inteligent Programming™ ALGORITHM

The inteligent Programming Algorithm rapidly programs Intel EPROMS using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of six minutes. Actual Programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27513 inteligent Programming Algorithm is shown in Figure 3. The only difference between the 27513 and other EPROM inteligent Programming is that the 27513 is programmed one 16 K-byte page at a time.

The inteligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the inteligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = 5.0V$.

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			μs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
		0.95	1.0	1.05	ms	inteligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

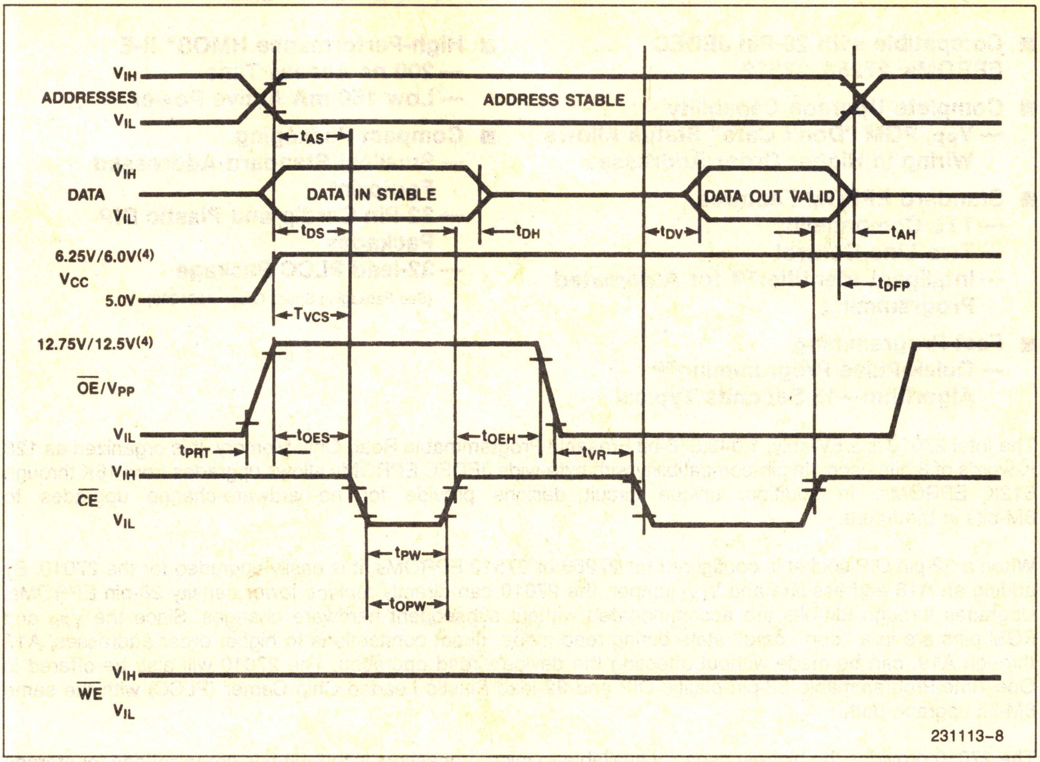
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (inteligent Programming Algorithm only) may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

PROGRAMMING WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
V_{IH}
DATA
V_{IL}
DATA IN STABLE
DATA OUT VALID
t_{DS}
t_{DH}
t_{DV}
t_{AH}
6.25V/6.0V(4)
V_{CC}
5.0V
t_{DFP}
T_{VCS}
12.75V/12.5V(4)
$\overline{OE}/V_{PP}$
V_{IL}
t_{PRT}
t_{OES}
t_{OEH}
t_{VR}
V_{IH}
$\overline{CE}$
V_{IL}
t_{PW}
t_{OPW}
V_{IH}
$\overline{WE}$
V_{IL}
231113-8

NOTES:

1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 K-byte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27010
1M (128K x 8) BYTE-WIDE EPROM

- **Compatible with 28-Pin JEDEC EPROMs: 27256, 27512**
- **Complete Upgrade Capability**
  - **V_{PP}, PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Standard EPROM Features**
  - **TTL Compatibility**
  - **Two Line Control**
  - **int$_e$ligent Identifier™ for Automated Programming**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **High-Performance HMOS* II-E**
  - **200 ns Access Time**
  - **Low 150 mA Active Power**
- **Compact Packaging**
  - **Smallest Standard-Addressed Footprint**
  - **32-Pin Cerdip and Plastic DIP Packages**
  - **32-lead PLCC Package**

  (See Packaging Spec., Order #231369)

The Intel 27010 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 128 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs allows upgrades from 16K through 512K EPROMs. In addition, unique circuit designs provide for no-hardware-change upgrades to 8M-bits in the future.

When a 32-pin DIP socket is configured for 27256 or 27512 EPROMs, it is easily upgraded for the 27010. By adding an A16 address line and V_{CC} jumper, the 27010 can directly replace lower density 28-pin EPROMs. Upgrades through 8M-bits are accommodated without subsequent hardware changes. Since the V_{PP} and PGM pins are in a "don't care" state during read mode, direct connections to higher order addresses, A17 through A19, can be made without affecting the device's read operation. The 27010 will also be offered in One-Time-Programmable 32-pin plastic DIP and 32-lead Plastic Leaded Chip Carrier (PLCC) with the same 8M-bit upgrade path.

The 27010 provides the highest capacity available to microprocessors with 8-bit bus organizations for storage of large portions of operating system and application software. Its 200 ns access time provides no-WAIT-state operation with high-performance CPUs such as the 10 MHz 80188. The 27010 offers a minimal chip solution for code storage needs of 100% firmware-based equipment. And for reprogrammable systems, popular application programs can be made much more "user friendly." Often-used software is silently and quickly executed from reliable EPROM storage, greatly enhancing system utility. When two or more EPROM sockets are used in 16-bit or 32-bit systems, the compact 32-pin DIP package requires the smallest board space of any high density memory without utilizing paged or multiplexed addressing schemes.

The 27010 is part of a three-product megabit EPROM family. Other family members are the 27011 and 27210. The 8 x 16K x 8 27011 utilizes page-addressing, allowing "drop-in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site. The 40-pin packaged 27210 is organized as 64K x 16, for systems in which word-wide memories are preferred.

The 27010 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_e$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27010 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

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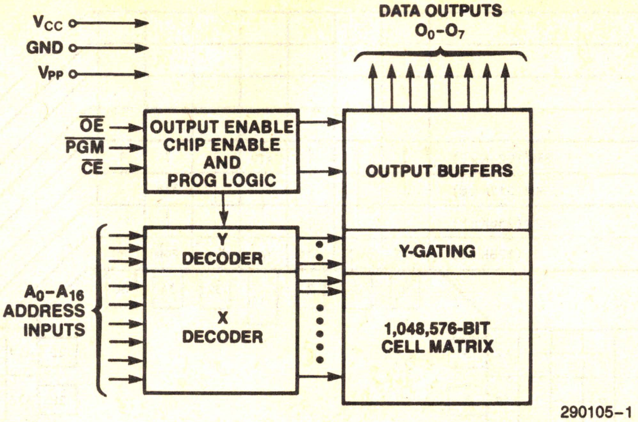
Order Number: 290105-002


V_{CC}
GND
V_{PP}
DATA OUTPUTS
O_0–O_7
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE CHIP ENABLE AND PROG LOGIC
OUTPUT BUFFERS
Y DECODER
Y-GATING
A_0–A_{16} ADDRESS INPUTS
X DECODER
1,048,576-BIT CELL MATRIX

290105–1

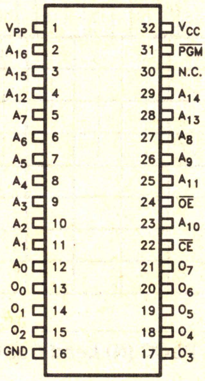
Figure 1. Block Diagram

Pin Names

A_0–A_{19}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT

8Mbit	4Mbit	2Mbit	27512	27256
A_{19}	V_{PP}	V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27010
P27010


V_{PP} 1
A_{16} 2
A_{15} 3
A_{12} 4
A_7 5
A_6 6
A_5 7
A_4 8
A_3 9
A_2 10
A_1 11
A_0 12
O_0 13
O_1 14
O_2 15
GND 16
32 V_{CC}
31 $\overline{PGM}$
30 N.C.
29 A_{14}
28 A_{13}
27 A_8
26 A_9
25 A_{11}
24 $\overline{OE}$
23 A_{10}
22 $\overline{CE}$
21 O_7
20 O_6
19 O_5
18 O_4
17 O_3

27256	27512	2Mbit	4Mbit	8Mbit
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

290105–2

Figure 2. Cerdip/Plastic DIP Pin Configurations

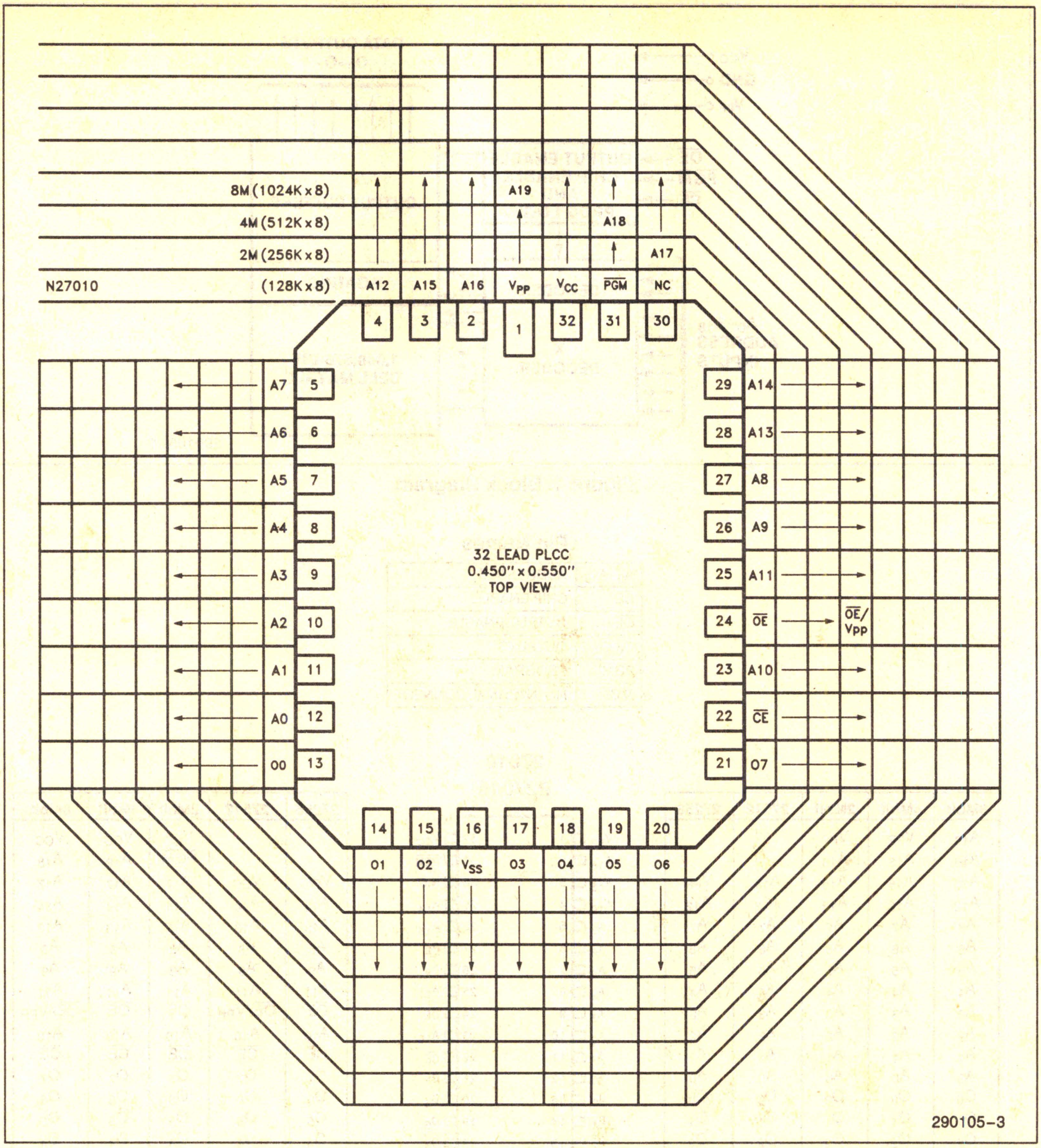

8M (1024K x 8)
4M (512K x 8)
2M (256K x 8)
N27010
(128K x 8)
A19
A18
A17
A12
A15
A16
V_{PP}
V_{CC}
$\overline{PGM}$
NC
4
3
2
1
32
31
30
A7
5
A6
6
A5
7
A4
8
A3
9
A2
10
A1
11
A0
12
O0
13
32 LEAD PLCC
0.450" x 0.550"
TOP VIEW
29
A14
28
A13
27
A8
26
A9
25
A11
24
$\overline{OE}$
$\overline{OE}$/V_{PP}
23
A10
22
$\overline{CE}$
21
O7
14
15
16
17
18
19
20
O1
O2
V_{SS}
O3
O4
O5
O6
290105-3

Figure 3. PLCC (N) Lead Configuration

NOTE:
Intel "Universal Site"—compatible EPROM pin configurations are shown in the blocks adjacent to the 27010 pins.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27010 VERSIONS

Speed Versions	Packaging Options	
	Cerdip	Plastic*
-250/05	Q, T, L	
-250/10	Q, T, L	
-300/05	Q, T, L	
-300/10	Q, T, L	

*Available 2H '86

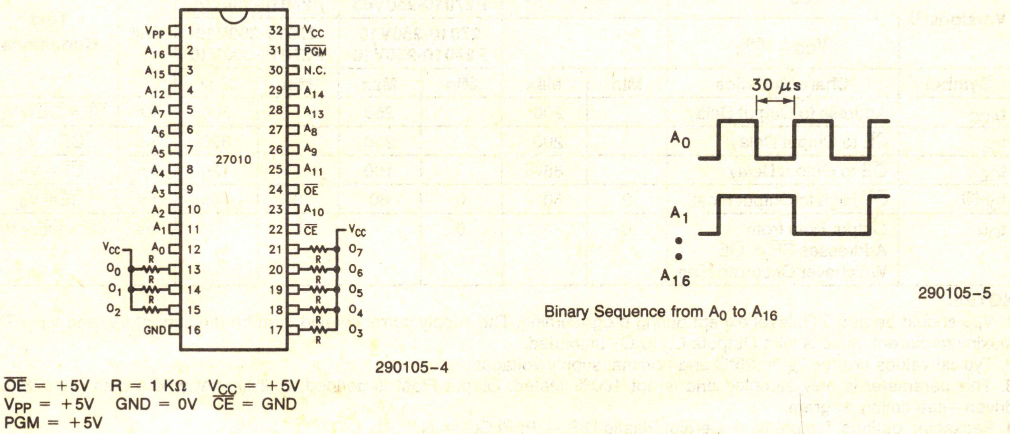
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27010 LD27010		Test Conditions
		Min	Max	
I_{CC_1}(1)	V_{CC} Active Current (mA)		160	$\overline{OE} = \overline{CE} = V_{IL}$, $T_{Ambient} = -40°C$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.


V_PP 1
A16 2
A15 3
A12 4
A7 5
A6 6
A5 7
A4 8
A3 9
A2 10
A1 11
A0 12
O0 13
O1 14
O2 15
GND 16
32 V_CC
31 PGM
30 N.C.
29 A14
28 A13
27 A8
26 A9
25 A11
24 OE
23 A10
22 CE
21 O7
20 O6
19 O5
18 O4
17 O3
27010
V_CC
R
30 µs
A0
A1
A16
Binary Sequence from A0 to A16

290105-4

$\overline{OE}$ = +5V   R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V   GND = 0V $\overline{CE}$ = GND
PGM = +5V

290105-5

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read .... 0°C to +70°C

Temperature Under Bias .... −10°C to +80°C

Storage Temperature .... −65°C to +125°C

All Input or Output Voltages with Respect to Ground .... −0.6V to +6.5V

Voltage on A_9 with Respect to Ground .... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground .... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(2)	Max	Units	
I_{LI}	Input Load Current			1	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{PP1}(1)	V_{PP} Load Current			1	μA	$V_{PP} \leq V_{CC}$
I_{SB}	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
I_{CC1}(1)	V_{CC} Current Active			150	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{PP}(1)	V_{PP} Read Voltage	−0.1		$V_{CC}+1$	V	$V_{CC} = 5.0V \pm 0.25$

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(4)	$V_{CC} \pm 5\%$	27010-200V05		27010-250V05 P27010-250V05		27010-300V05 P27010-300V05		Unit	Test Conditions
	$V_{CC} \pm 10\%$			27010-250V10 P27010-250V10		27010-300V10 P27010-300V10			
Symbol	Characteristics	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		85(5)		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	60	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

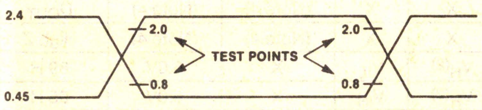
NOTES:

1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. Packaging options: No prefix = Cerdip; Plastic DIP = P; PLCC = N.
5. The 85 ns t_{OE} specification is a temporary relaxation. The final specification will be 75 ns.

CAPACITANCE[2] $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Capacitance	18	25	pF	$V_{PP} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM

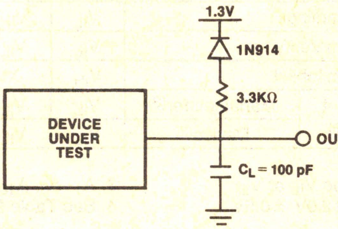


2.4
2.0
TEST POINTS
2.0
0.45
0.8
0.8

290105-6

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



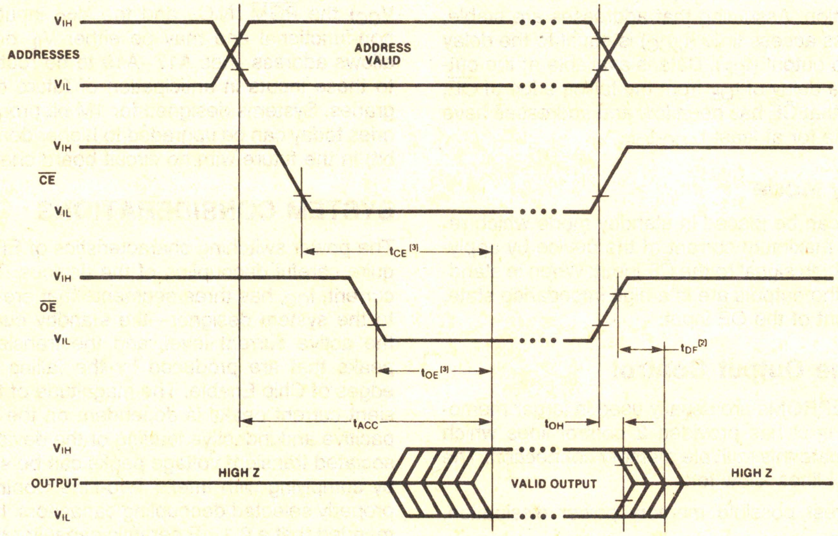
1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
$C_L = 100$ pF

C_L = 100 pF

C_L Includes Jig Capacitance

290105-7

A.C. WAVEFORMS



V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}[3]
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF}[2]
t_{OE}[3]
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z

290105-8

NOTES:

1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27010 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Mode	Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X(1)	X	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IL}	X	5.0V	89 H
	Device(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IH}	X	5.0V	05 H

NOTES:

1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1-A_8, $A_{10}-A_{16} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27010 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Upgrade Path

Future upgrades to 8M-bits are easily accomplished due to the standardized pin configuration of the 27010. When the 27010 is in the Read Mode ($V_{PP} \leq V_{CC}$) the $\overline{PGM}$, N.C., and the V_{PP} inputs become non-functional and may be either V_{IL} or V_{IH}. This allows address lines A17–A19 to be routed directly to these inputs in anticipation of future density upgrades. Systems designed for 1M-bit program memories today can be upgraded to higher densities (8M-bit) in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_{e}$ligent Identifier™ Mode

The int$_{e}$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_{e}$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

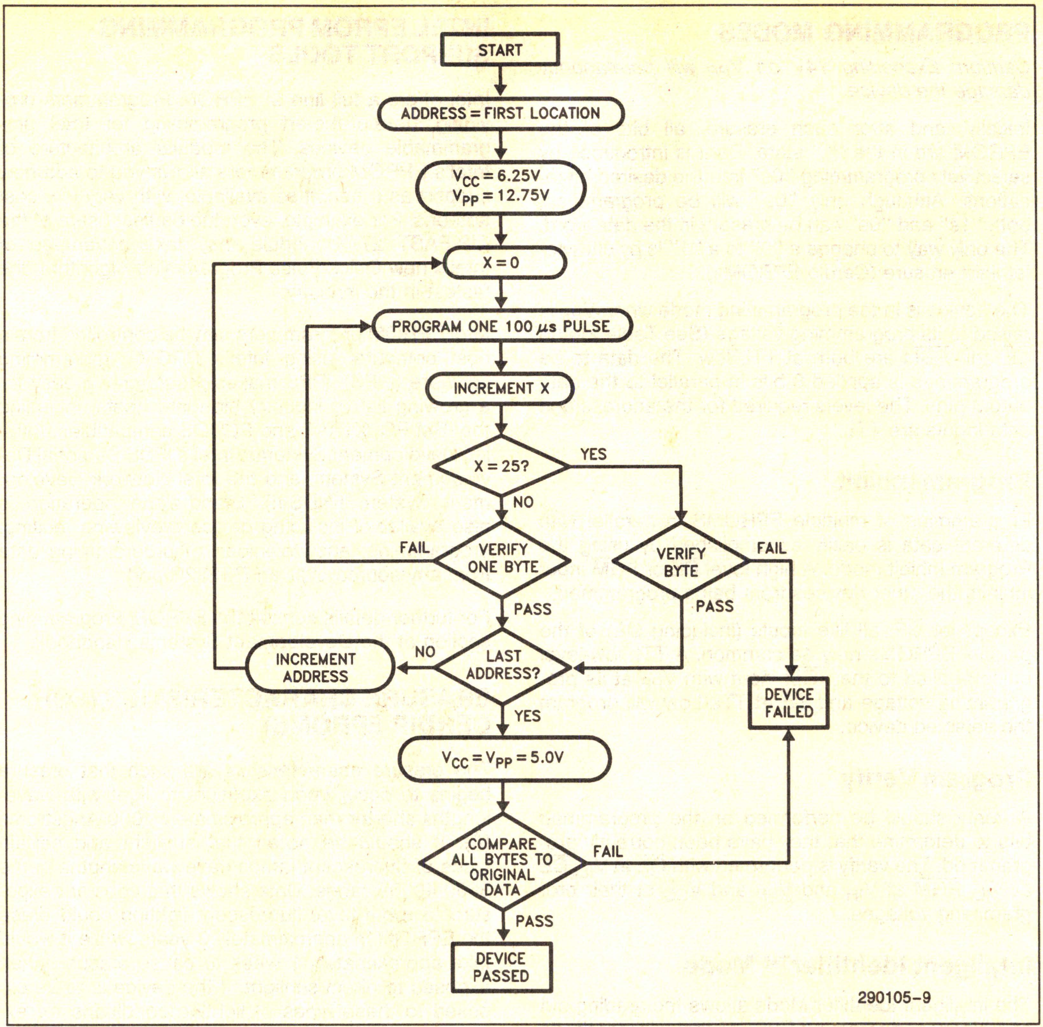

START
ADDRESS = FIRST LOCATION
$V_{CC} = 6.25V$
$V_{PP} = 12.75V$
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
VERIFY BYTE
FAIL
PASS
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
$V_{CC} = V_{PP} = 5.0V$
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
290105–9

Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27010 EPROM can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under 15 seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{CC} = 6.25V$ and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = 5.0V$ ($V_{PP} \leq V_{CC}$).

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program & Verify)		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

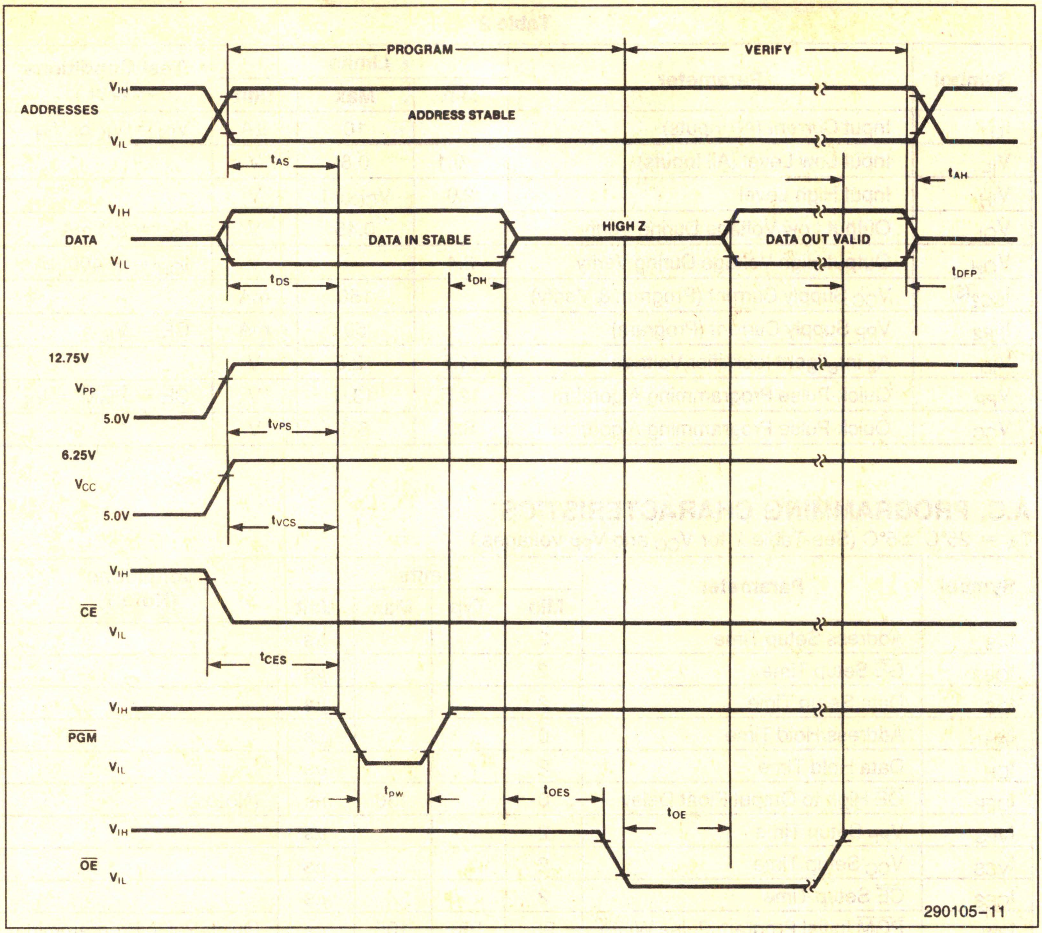
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V$_{IH}$
V$_{IL}$
ADDRESS STABLE
t$_{AS}$
t$_{AH}$
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t$_{DS}$
t$_{DH}$
t$_{DFP}$
12.75V
V$_{PP}$
5.0V
t$_{VPS}$
6.25V
V$_{CC}$
5.0V
t$_{VCS}$
CE
t$_{CES}$
PGM
t$_{PW}$
t$_{OES}$
t$_{OE}$
OE
290105-11

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27010, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27011
PAGE-ADDRESSED 1M (8 x 16K x 8) EPROM

- **Paged Organization**
  - **Reduced Physical Address Requirement**
- **Compatible with 28-Pin JEDEC EPROMs**
  - **Single-Trace Modification for Retrofitting 27128-Based Designs**
- **No-Hardware-Change Upgrades**
  - **Drop-In 27513 Replacement**
  - **Direct Pin Compatibility through 32 M-Bit Density**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **Automatic Page Clear**
  - **Resets to Page 0 on Power-Up**
- **High-Performance HMOS* II-E**
  - **200 ns Access Time**
  - **Low 150 mA Active Power**
- **Standard EPROM Features**
  - **TTL Compatibility**
  - **Two Line Control**
  - **int$_e$ligent Identifier™ for Automated Programming**
- **Smallest Megabit Packages**
  - **28-Pin DIP, Minimal Footprint without Address/Data Multiplexing**
  - **32-Lead PLCC**

(See Packaging Spec., Order #231369)

The Intel 27011 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 8 pages of 16K 8-bit words. Its pin-compatibility with byte-wide JEDEC EPROMs allows retrofitting existing designs to the greater storage capacity afforded by the page-addressed organization. Its 16 K-byte physical address space requirement allows the 27011 to be utilized in address-constrained system designs.

When a 28-pin DIP or 32-lead PLCC (Plastic Leaded Chip Carrier) socket is configured for 2764 or 27128 EPROMs, it is easily retrofitted to the 27011. By adding a WRITE ENABLE signal to pin 27 (DIP) or pin 31 (PLCC) (unused on 2764 and 27128), the 27011 can be used in an existing design. Thus, the 27011 enables product enhancements via additional feature sets and firmware-intensive performance upgrades. For sockets specifically configured for page-addressed EPROM, no hardware changes are required for upgrades through 32 M-bits in density!

The page-addressed organization allows the use of 28-pin DIP packages, the smallest megabit EPROM footprint with applicability to all microprocessors. This provides very efficient circuit board layouts. For even greater board space savings, the 27011 will also be offered(1) in 32-lead PLCC packages, along with the production-oriented OTP (One Time Programmable) Plastic DIP.

The 27011 is part of a three-product megabit EPROM family. The other two members are standard-addressed byte-wide and word-wide versions, the 27010 and 27210, respectively. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 27210 is packaged in a 40-pin DIP with a 64K x 16 organization.

The 27011 has an automatic page clear circuit for ease of use of its paged organization. The page-select latch is automatically cleared to the lowest order page upon system power-up. The 27011 also contains many industry-standard features such as two-line output control for simple interfacing and the int$_e$ligent Identifier™ feature for automated programming. It also can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27011 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986

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Order Number: 290107-002

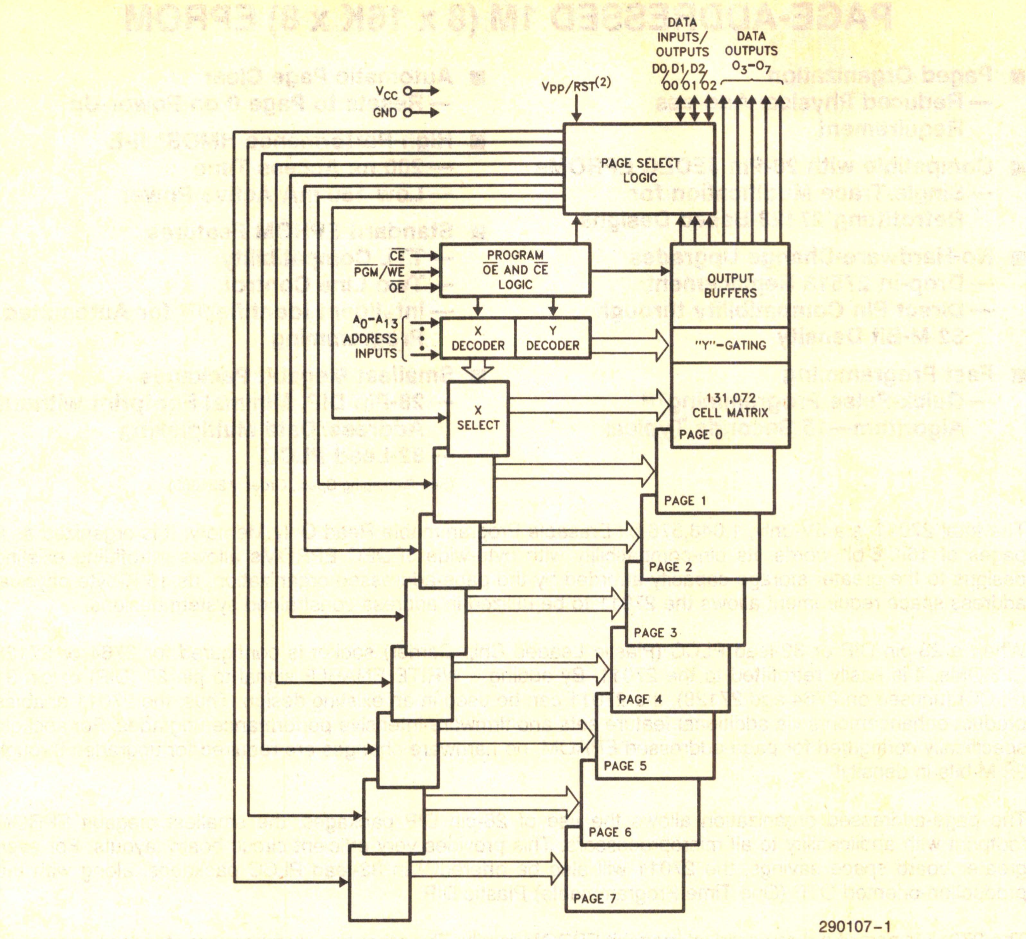
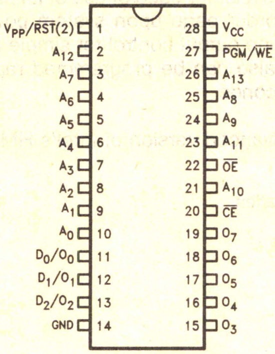

DATA INPUTS/ OUTPUTS
D0 D1 D2
O0 O1 O2
DATA OUTPUTS
O3–O7
VPP/RST(2)
VCC
GND
PAGE SELECT LOGIC
CE
PGM/WE
OE
PROGRAM OE AND CE LOGIC
OUTPUT BUFFERS
A0–A13 ADDRESS INPUTS
X DECODER
Y DECODER
"Y"-GATING
X SELECT
131,072 CELL MATRIX
PAGE 0
PAGE 1
PAGE 2
PAGE 3
PAGE 4
PAGE 5
PAGE 6
PAGE 7
290107-1

Figure 1. Block Diagram

4 M-bit	2 M-bit	27513	27128A
$V_{PP}/\overline{RST}$	$V_{PP}/\overline{RST}$	$\overline{RST}^{(2)}$	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	D_0/O_0	D_0/O_0	O_0
D_1/O_1	D_1/O_1	D_1/O_1	O_1
D_2/O_2	D_2/O_2	O_2	O_2
GND	GND	GND	GND

27011
P27011


$V_{PP}/\overline{RST}^{(2)}$ 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
D_0/O_0 11
D_1/O_1 12
D_2/O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}/\overline{WE}$
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3

27128A	27513	2 M-bit	4 M-bit
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{WE}$	$\overline{PGM}/\overline{WE}$	$\overline{WE}$
A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	D_4/O_4
O_3	O_3	D_3/O_3	D_3/O_3

290107-2

Figure 2. Pin Configuration

Pin Names

A_0–A_{13}	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Page-Select Write Enable
O_2–O_7	Outputs
D_X/O_X	Input/Outputs
$V_{PP}/\overline{\text{RST}}^{(2)}$	V_{PP}/Page 0 RESET
N.C.	No Internal Connection
D.U.	Don't Use

512K TO 8M PAGE-ADDRESSED EPROM FAMILY IN 32-PIN PLCC

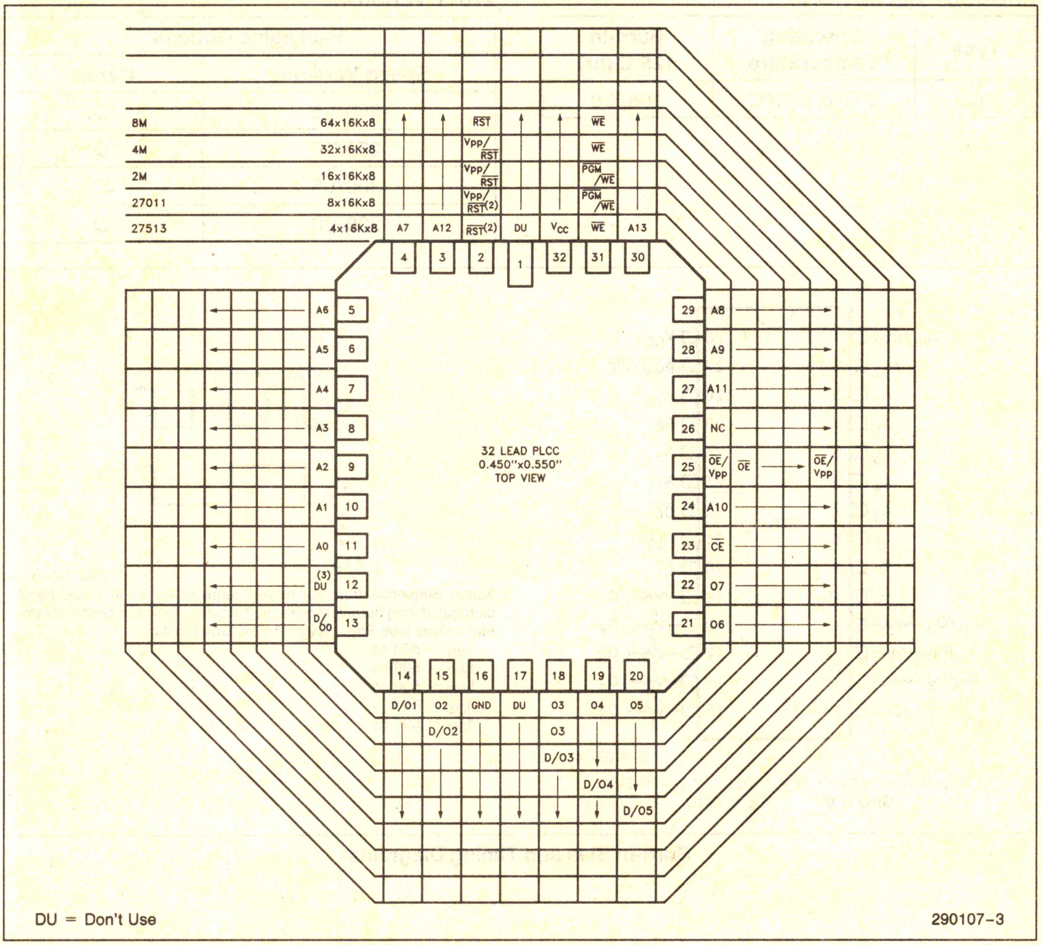

8M
64x16Kx8
4M
32x16Kx8
2M
16x16Kx8
27011
8x16Kx8
27513
4x16Kx8
RST
Vpp/RST
Vpp/RST
Vpp/RST(2)
RST(2)
WE
WE
PGM/WE
PGM/WE
WE
A7
A12
DU
Vcc
A13
4
3
2
1
32
31
30
A6
5
A5
6
A4
7
A3
8
A2
9
A1
10
A0
11
(3) DU
12
D/O0
13
29
A8
28
A9
27
A11
26
NC
25
OE/Vpp
OE
OE/Vpp
24
A10
23
CE
22
O7
21
O6
32 LEAD PLCC
0.450"x0.550"
TOP VIEW
14
15
16
17
18
19
20
D/O1
O2
GND
DU
O3
O4
O5
D/O2
O3
D/O3
D/O4
D/O5
DU = Don't Use
290107-3

Figure 3. PLCC (N) Lead Configuration

NOTES:

1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27011 pins.
2. This pin should be tied to an active low system reset line ($\overline{\text{RST}}$). Now available on the 27513, this feature will be added later (1987) on the 27011 to reset devices to Page 0 when this line is brought to a TTL low (V_{IL}).
3. This pin may be common with A_0 and should not be used for routing other signals.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

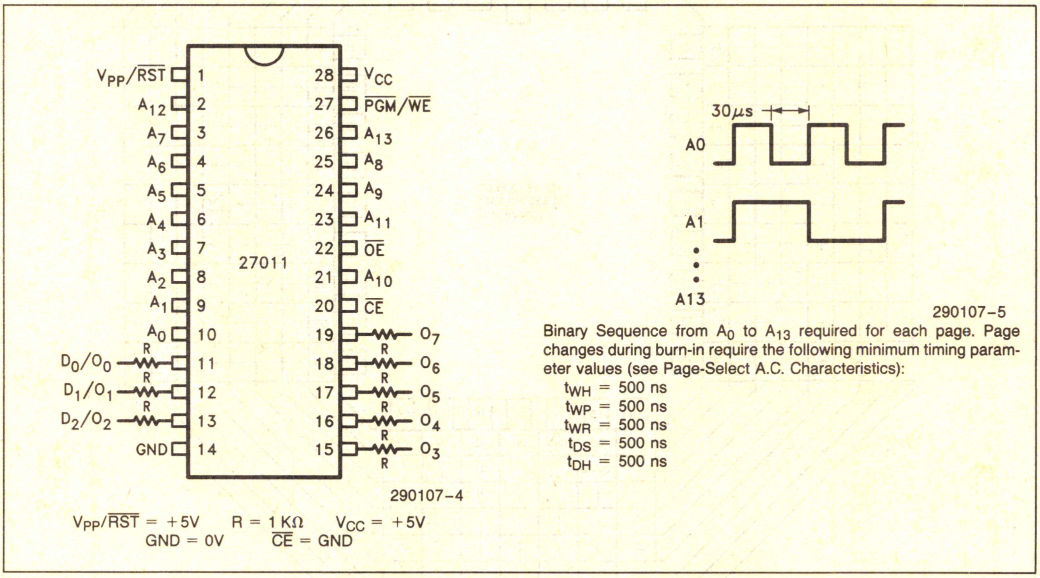
PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8

EXPRESS OPTIONS

27011 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-250/05	Q
-250/10	Q
-300/05	Q
-300/10	Q


$V_{PP}/\overline{RST}$ 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
D_0/O_0 11
D_1/O_1 12
D_2/O_2 13
GND 14
28 V_{CC}
27 $\overline{PGM}/\overline{WE}$
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$
21 A_{10}
20 $\overline{CE}$
19 O_7
18 O_6
17 O_5
16 O_4
15 O_3
R
27011
30µs
A0
A1
A13

290107-4

$V_{PP}/\overline{RST}$ = +5V R = 1 KΩ V_{CC} = +5V
GND = 0V $\overline{CE}$ = GND

290107-5

Binary Sequence from A_0 to A_{13} required for each page. Page changes during burn-in require the following minimum timing parameter values (see Page-Select A.C. Characteristics):

t_{WH} = 500 ns
t_{WP} = 500 ns
t_{WR} = 500 ns
t_{DS} = 500 ns
t_{DH} = 500 ns

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
 Read ....0°C to +70°C

Temperature Under Bias ....−10°C to +80°C

Storage Temperature ....−65°C to +125°C

All Input or Output Voltages with
 Respect to Ground† ....−0.6V to +6.25V

Voltage on A_9 with
 Respect to Ground ....−0.6V to +13.5V

V_{PP} Supply Voltage with Respect to
 Ground During Programming ....−0.6V to +14V

V_{CC} Supply Voltage
 with Respect to Ground ....−0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			1	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
$I_{LRST}^{(1)}$	$V_{PP}/\overline{RST}$ Load Current			500	µA	$V_{PP}/\overline{RST} = 0V$
I_{SB}	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
$I_{CC1}^{(5)}$	V_{CC} Current Active			150	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{CLR}	Page Latch Clear—V_{CC}		3.5	4.0	V	

A.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Versions (5)	V_{CC} ±5%	27011-200V05		27011-250V05 P27011-250V05 N27011-250V05		27011-300V05 P27011-300V05 N27011-300V05		Units
	V_{CC} ±10%			27011-250V10 P27011-250V10 N27011-250V10		27011-300V10 P27011-300V10 N27011-300V10		
Symbol	**Characteristics**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		$85^{(6)}$		100		120	ns
$t_{DF}^{(3)}$	$\overline{OE}$ High to Output Float	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

NOTES:

1. $V_{PP}/\overline{RST}$ load current is worst case at 0V. This pin should be tied to an active low system reset line ($\overline{RST}$). Although not initially included on 27011, a feature will be added later (1987) to reset the device to PAGE 0 when this line is brought to a TTL low (V_{IL}). A minimum voltage level of V_{IH} must be supplied to this pin during normal read operation to ensure future compatibility.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. Packaging options: No prefix = Cerdip; Plastic DIP = P; PLCC = N.
5. The maximum current value is with outputs O_0 to O_7 unloaded.
6. The 85 ns t_{OE} specification is a temporary relaxation. The final specification will be 75 ns.

PAGE-SELECT WRITE OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

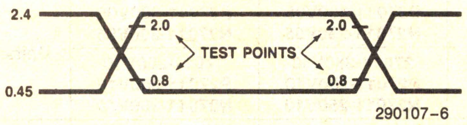
Symbol	Parameter	Limits Min	Limits Max	Units	Test Conditions
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}$ High Delay Time	55		ns	

CAPACITANCE(1) $T_A = +25°C$, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{V_{PP}/\overline{RST}}$	$V_{PP}/\overline{RST}$ Capacitance	18	25	pF	$V_{IN} = 0V$

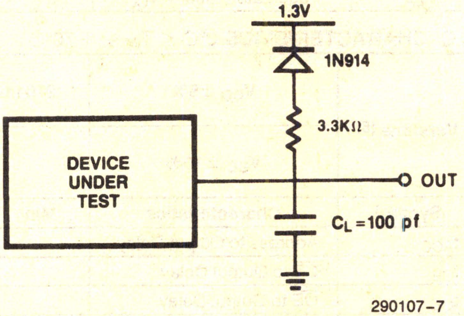
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



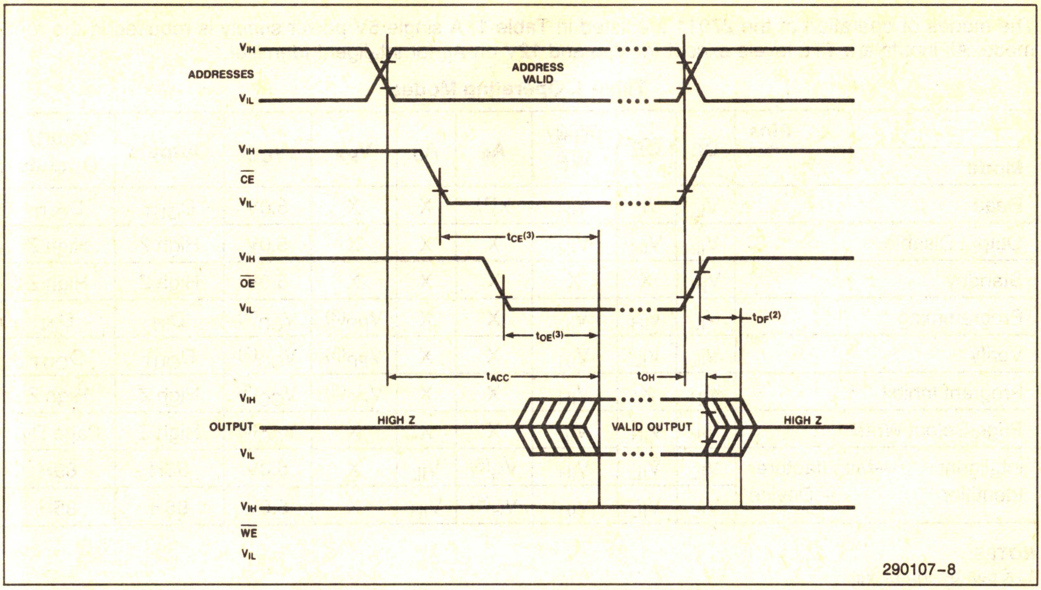
AC Testing inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

A.C. TESTING LOAD CIRCUIT

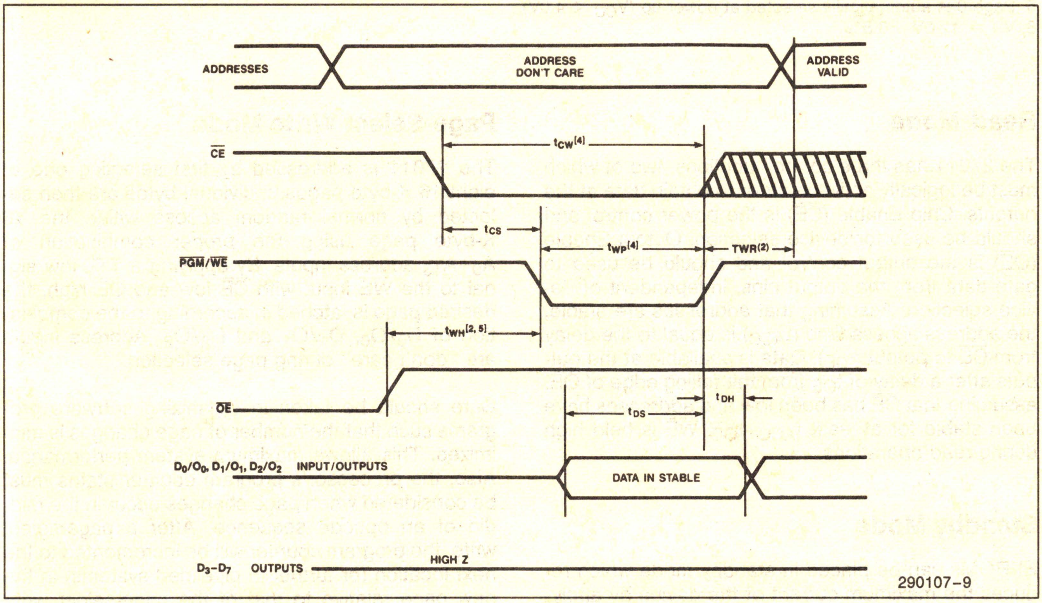


C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION


ADDRESSES
V_IH
V_IL
ADDRESS VALID
CE
OE
tCE(3)
tOE(3)
tDF(2)
tACC
tOH
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
WE
290107-8

A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION


ADDRESSES
ADDRESS DON'T CARE
ADDRESS VALID
CE
tCW(4)
tCS
tWP(4)
TWR(2)
PGM/WE
tWH(2, 5)
OE
tDH
tDS
D0/O0, D1/O1, D2/O2 INPUT/OUTPUTS
DATA IN STABLE
D3–D7 OUTPUTS
HIGH Z
290107-9

NOTES:

1. Typical values are for T_A = +25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27011 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_{e}$ligent Identifier.

Table 1. Operating Modes

Pins Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$/ $\overline{WE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	5.0V	High Z	High Z
Standby	V_{IH}	X	X	X	X	X	5.0V	High Z	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}(3)	V_{CC}(3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{CC}(5)	High Z	Page D_{IN}
int$_{e}$ligent Identifier —Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IL}	X	5.0V	89H	89H
—Device	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IH}	X	5.0V	85H	85H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 3 for V_{CC} and V_{PP}.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. $V_H = 12.0V \pm 0.5\%$.

Read Mode

The 27011 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27011 is addressed by first selecting one of eight 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0, D_1/O_1 and D_2/O_2. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output Page Selection	D_2/O_2	D_1/O_1	D_0/O_0
Select Page 0	V_{IL}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}
Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 7	V_{IH}	V_{IH}	V_{IH}

Automatic Page Latch Clear

The 27011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case −10% V_{CC} supply condition) against spurious page latch clearing.

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27011s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} will permanently damage the 27011.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27011 is in the programming mode when the V_{PP} input is at its programming voltage and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27011s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27011s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27011s may be common. A TTL low-level pulse applied to the $\overline{PGM}/\overline{WE}$ input with V_{PP} at its programming voltage will program the selected 27011.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPs makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

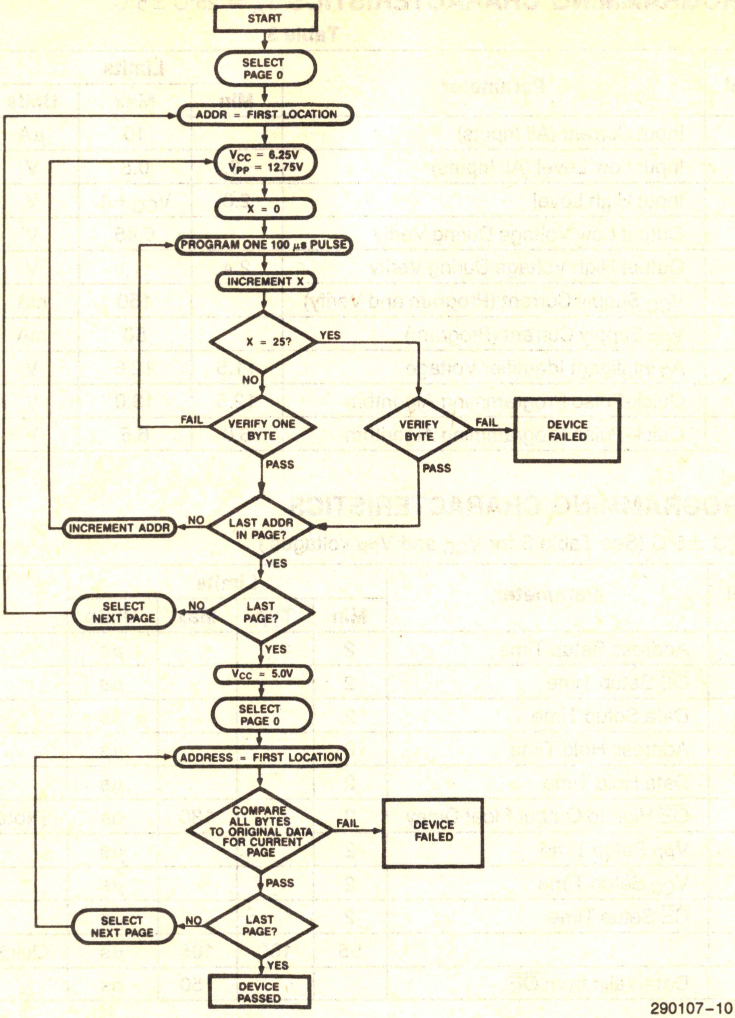

START
SELECT PAGE 0
ADDR = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 μs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY ONE BYTE
FAIL
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
LAST ADDR IN PAGE?
NO
INCREMENT ADDR
YES
LAST PAGE?
NO
SELECT NEXT PAGE
YES
V_{CC} = 5.0V
SELECT PAGE 0
ADDRESS = FIRST LOCATION
COMPARE ALL BYTES TO ORIGINAL DATA FOR CURRENT PAGE
FAIL
DEVICE FAILED
PASS
LAST PAGE?
NO
SELECT NEXT PAGE
YES
DEVICE PASSED
290107–10

Figure 4. 27011 Quick-Pulse Programming™ Flowchart

Quick Pulse Programming™ Algorithm

Intel's 27011 EPROM can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 3

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400\ \mu$A
I_{CC2}(3)	V_{CC} Supply Current (Program and Verify)		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 3 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}		95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

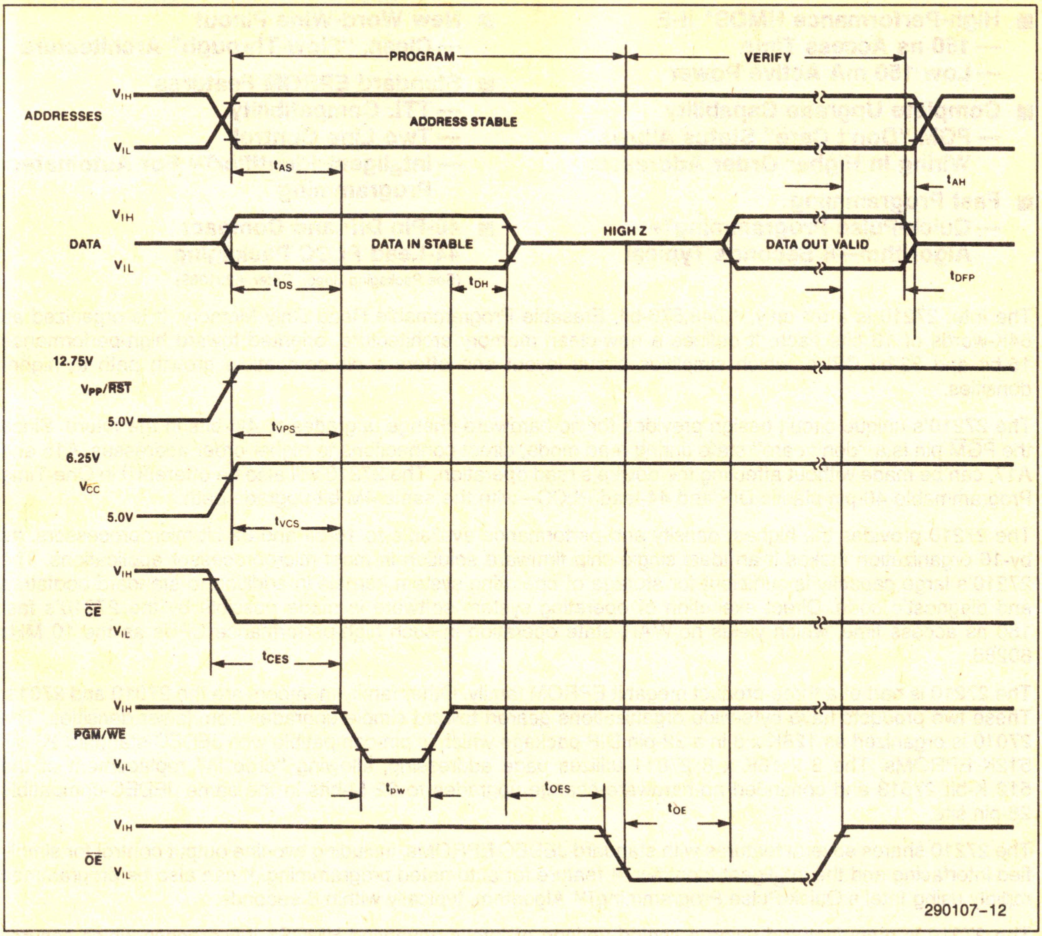
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . . 20 ns
Input Pulse Levels . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_IH
V_IL
ADDRESS STABLE
t_AS
t_AH
DATA
V_IH
V_IL
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DFP
12.75V
V_PP/RST
5.0V
t_VPS
6.25V
V_CC
5.0V
t_VCS
V_IH
CE
V_IL
t_CES
V_IH
PGM/WE
V_IL
t_PW
t_OES
t_OE
V_IH
OE
V_IL

290107-12

NOTES:

1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

PRELIMINARY

27210
1M (64K x 16) WORD-WIDE EPROM

- **High-Performance HMOS* II-E**
  - **150 ns Access Time**
  - **Low 150 mA Active Power**
- **Complete Upgrade Capability**
  - **PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Fast Programming**
  - **Quick-Pulse Programming™ Algorithm—8 Seconds Typical**
- **New Word-Wide Pinout**
  - **Clean, "Flow-Through" Architecture**
- **Standard EPROM Features**
  - **TTL Compatibility**
  - **Two Line Control**
  - **int$_{e}$ligent Identifier™ For Automated Programming**
- **40-Pin DIP and Compact 44-Lead PLCC Packaging**
  (See Packaging Spec., Order #231369)

The Intel 27210 is a 5V only, 1,048,576-bit, Erasable Programmable Read Only Memory. It is organized as 64K-words of 16 bits each. It defines a new-clean memory architecture, oriented toward high-performance 16-bit and 32-bit CPUs, which simplifies circuit layout and offers a pin-compatible growth path to higher densities.

The 27210's unique circuit design provides for no-hardware-change upgrades to 4M-bits in the future. Since the $\overline{\text{PGM}}$ pin is a "don't care" state during read mode, direct connections to higher order addresses, A16 and A17, can be made without affecting the device's read operation. The 27210 will also be offered(1) in One-Time Programmable 40-pin plastic DIP and 44-lead PLCC—with the same 4M-bit upgrade path.

The 27210 provides the highest density and performance available to 16-bit and 32-bit microprocessors. Its by-16 organization makes it an ideal single-chip firmware solution in most microprocessor applications. The 27210's large capacity is sufficient for storage of operating system kernels in addition to standard bootstrap and diagnostic code. Direct execution of operating system software is made possible by the 27210's fast 150 ns access time, which yields no-WAIT-state operation in such high-performance CPUs as the 10 MHz 80286.

The 27210 is part of a three-product megabit EPROM family. Other family members are the 27010 and 27011. These two products have byte-wide organizations geared toward simple upgrades from lower densities. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 8 x 16K x 8 27011 utilizes page addressing, allowing "drop in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site.

The 27210 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_{e}$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 8 seconds.

The 27210 is manufactured using a scaled verison of Intel's advanced HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

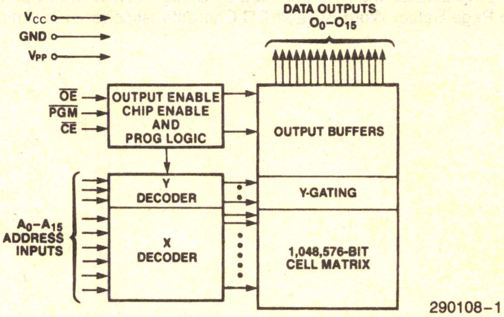


Figure 1. Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

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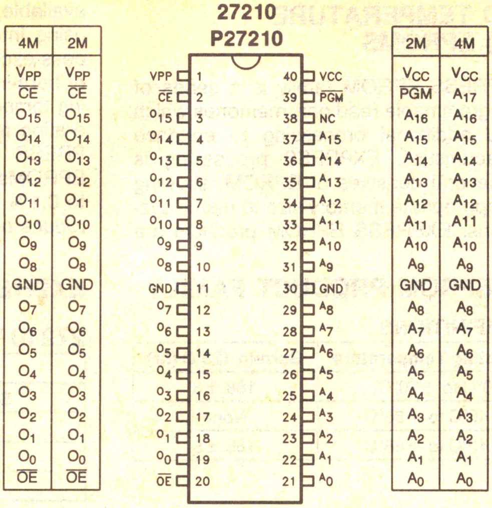
Order Number: 290108-002

Pin Names

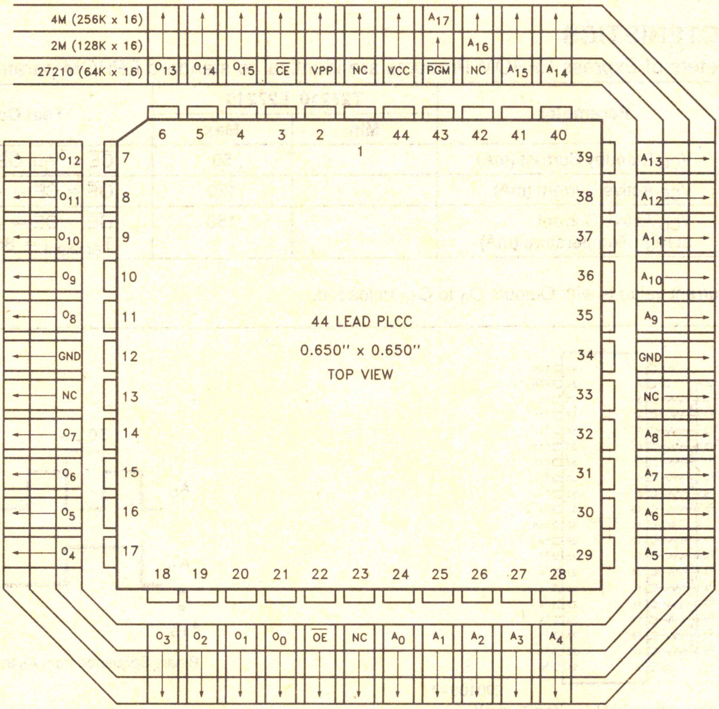
A_0–A_{17}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE


27210
P27210
4M
2M
VPP
CE
O15
O14
O13
O12
O11
O10
O9
O8
GND
O7
O6
O5
O4
O3
O2
O1
O0
OE
VPP 1
CE 2
O15 3
O14 4
O13 5
O12 6
O11 7
O10 8
O9 9
O8 10
GND 11
O7 12
O6 13
O5 14
O4 15
O3 16
O2 17
O1 18
O0 19
OE 20
40 VCC
39 PGM
38 NC
37 A15
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 GND
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
2M
4M
VCC
PGM
A17
A16
A15
A14
A13
A12
A11
A10
A9
GND
A8
A7
A6
A5
A4
A3
A2
A1
A0

290108-2

NOTE: Compatible Higher Density Word Wide EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27210 Pins

Figure 2. Cerdip/Plastic(P) DIP Pin Configurations


4M (256K x 16)
2M (128K x 16)
27210 (64K x 16)
A17
A16
O13
O14
O15
CE
VPP
NC
VCC
PGM
NC
A15
A14
6
5
4
3
2
1
44
43
42
41
40
O12
O11
O10
O9
O8
GND
NC
O7
O6
O5
O4
7
8
9
10
11
12
13
14
15
16
17
44 LEAD PLCC
0.650" x 0.650"
TOP VIEW
39
38
37
36
35
34
33
32
31
30
29
A13
A12
A11
A10
A9
GND
NC
A8
A7
A6
A5
18
19
20
21
22
23
24
25
26
27
28
O3
O2
O1
O0
OE
NC
A0
A1
A2
A3
A4

290108-3

Figure 3. PLCC(N) Lead Configuration

NOTE:

1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27210 pins.

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27210 Versions

Packaging Options	
Speed Versions	Cerdip
-170/05	Q
-200/05	T, L, Q
-250/05	T, L, Q
-170/10	T, L, Q
-200/10	T, L, Q
-250/10	T, L, Q

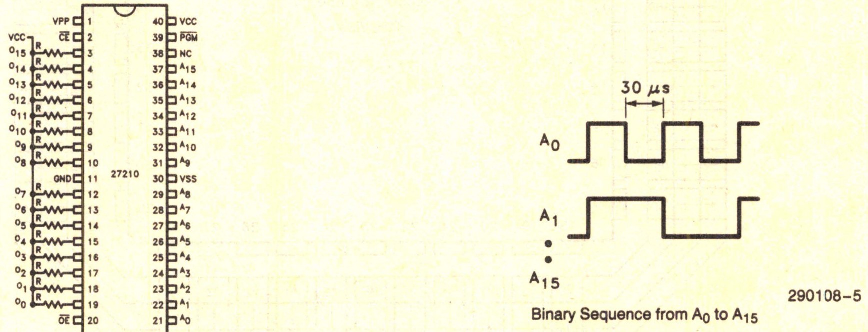
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	T27210, L27210		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		170	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with Outputs O_0 to O_{15} unloaded.



290108-4

$\overline{OE}$ = +5V R = 1 kΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = GND

290108-5

Binary Sequence from A_0 to A_{15}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read .... 0°C to +70°C

Temperature Under Bias .... −10°C to +80°C

Storage Temperature .... −65°C to +125°C

All Input or Output Voltages with Respect to Ground .... −0.6V to +6.25V

Voltage on A_9 with Respect to Ground .... −0.6V to +13.0V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground .... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			1	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			1	μA	$V_{OUT} = 5.5V$
I_{PP1}(2)	V_{PP} Load Current Read			1	μA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			150	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(5)	$V_{CC} \pm 5\%$	27210-150/05		27210-170/05 P27210-170/05 N27210-170/05		27210-200/05 P27210-200/05 N27210-200/05		27210-250/05 P27210-250/05 N27210-250/05		Unit
	$V_{CC} \pm 10\%$			27210-170/10		27210-200/10 P27210-200/10 N27210-200/10		27210-250/10 P27210-250/10 N27210-250/10		
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		65		70		75		100	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	50	0	55	0	60	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns

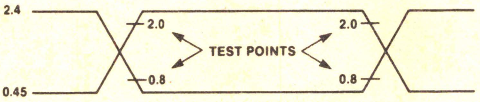
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The maximum current value is with Outputs O_0 to O_{15} unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging options: No prefix = Cerdip; Plastic DIP = P; PLCC = N.
6. Both GND pins should be connected to the ground trace on circuit boards.

CAPACITANCE(2) $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Input Capacitance		25	pF	$V_{PP} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM

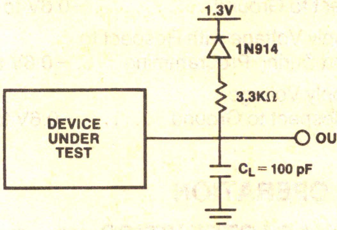


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8

290108-6

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT

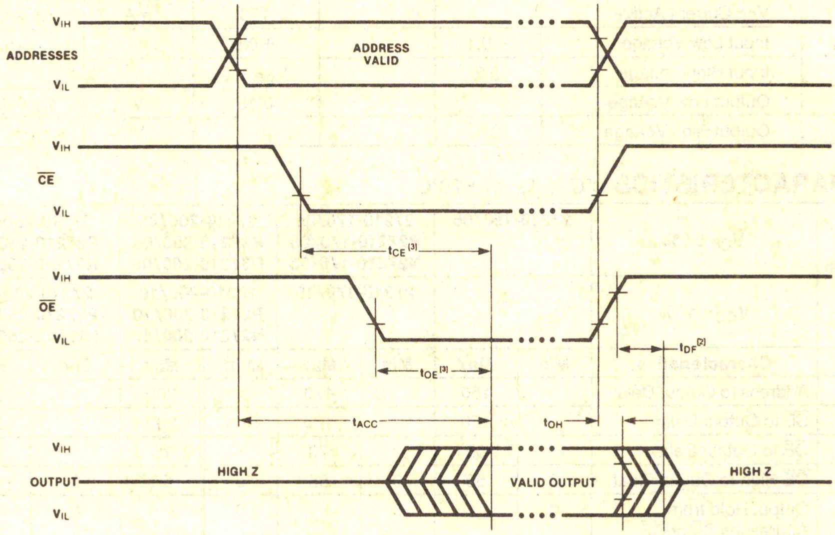


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
C_L = 100 pF

290108-7

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}[3]
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF}[2]
t_{OE}[3]
t_{ACC}
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z

290108-8

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Pins Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X(1)	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IL}	V_{CC}	5.0V	0089 H
	Device(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IH}	V_{CC}	5.0V	00FFH

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. $A_1 - A_8$, $A_{10} - A_{15} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu\text{W/cm}^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 $\mu\text{W/cm}^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

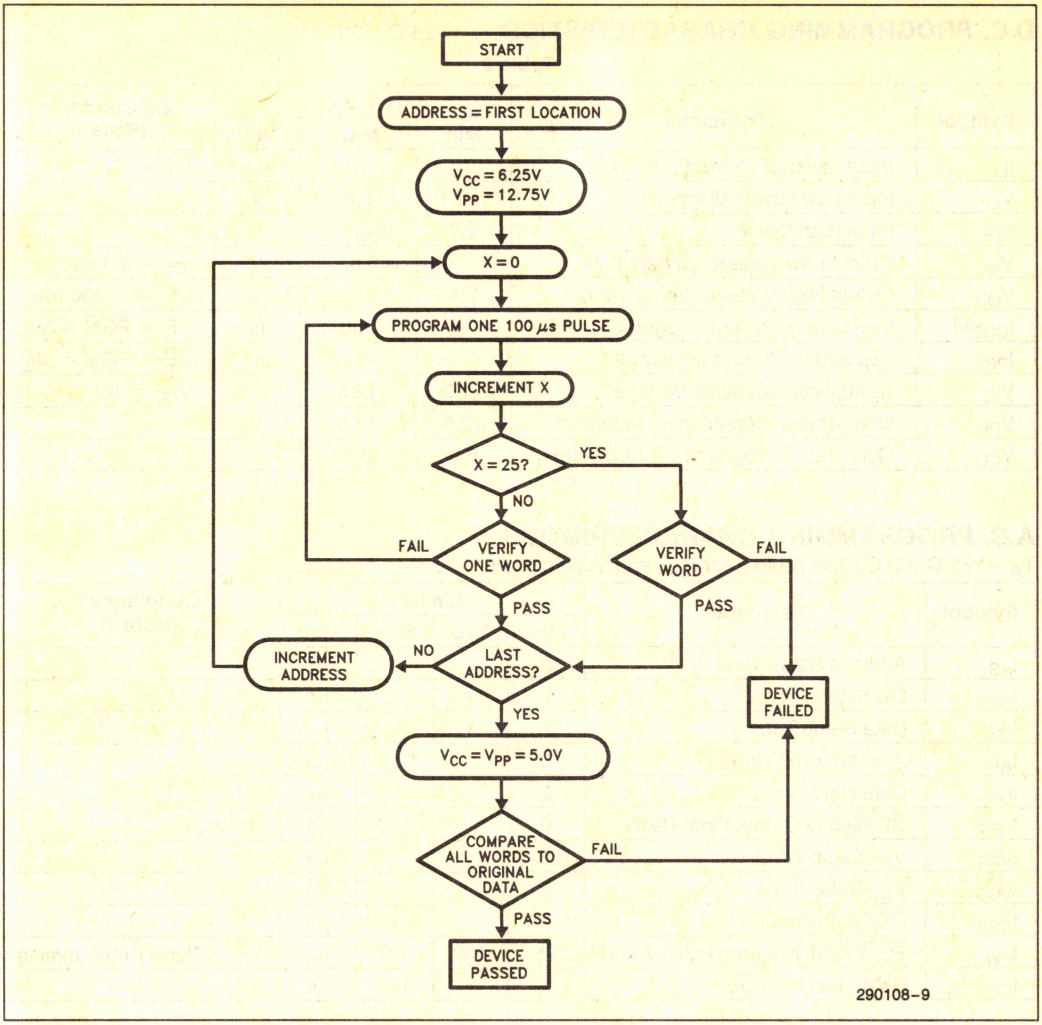

START
ADDRESS = FIRST LOCATION
V_{CC} = 6.25V
V_{PP} = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE WORD
VERIFY WORD
FAIL
PASS
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
V_{CC} = V_{PP} = 5.0V
COMPARE ALL WORDS TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
290108-9

Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27210 EPROMs can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under eight seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a word verification to determine when the addressed word has been successfully programmed. Up to 25 100 µs pulses per word are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and word verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all data words should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Leakage Current (All Inputs)		10	μA	$V_{IN} = 6V$
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program & Verify)		160	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	$V_{CC} = 5V$
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

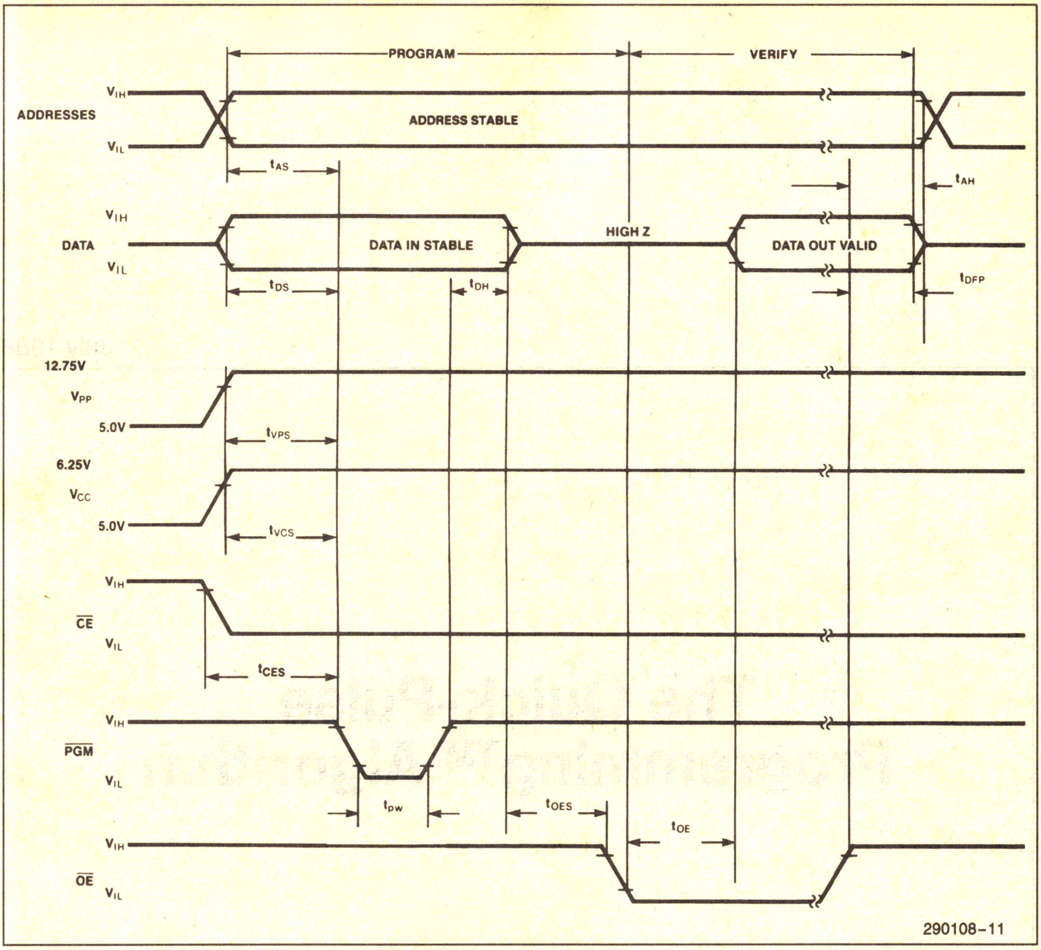
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ...... 20 ns
Input Pulse Levels .... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V and 2.0V
Output Timing Reference Level ...... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_{15} unloaded.

PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_IH
V_IL
ADDRESS STABLE
t_AS
t_AH
DATA
V_IH
V_IL
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DFP
12.75V
V_PP
5.0V
t_VPS
6.25V
V_CC
5.0V
t_VCS
V_IH
CE
V_IL
t_CES
V_IH
PGM
V_IL
t_PW
t_OES
t_OE
V_IH
OE
V_IL

290108-11

NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27210, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

intel®

APPLICATION NOTE

AP-277

July 1986

The Quick-Pulse Programming™ Algorithm

TERRY KENDALL
PROGRAMMABLE MEMORY OPERATION
INTEL CORPORATION

© Intel Corporation, 1986

Order Number: 292013-001

INTRODUCTION

Intel developed the Quick-Pulse Programming™ algorithm to dramatically reduce the programming throughput time in production environments. The algorithm supports plastic and PLCC (Plastic Leaded Chip Carrier) EPROMs because these devices are ideally suited for production applications. By using the Quick-Pulse Programming algorithm, a substantial decrease in programming time can be realized over older programming algorithms. For example, a 256k EPROM can be programmed in under four seconds, a 40 fold time improvement over the int$_{e}$ligent Programming™ algorithm.

BENEFITS FOR THE PRODUCTION ENVIRONMENT

The Quick-Pulse Programming algorithm has been introduced as the primary programming technique for OTP™ (One Time Programmable) EPROMs. OTP Plastic DIP EPROMs are ideal for production because they can be used in auto-insertion and auto-programming machines. Ceramic DIP (CERDIP) versions of newly introduced devices including the 27C256 and Megabit EPROMs (27010, 27011, and 27210) can also use Quick-Pulse Programming. Because of their erasability and reprogrammability, CERDIP EPROMs are used for prototyping and system development. When manufacturing begins, OTP EPROMs can be programmed as needed on the production floor using the Quick-Pulse Programming algorithm. If an error in firmware is discovered or a density increase is required after manufacturing has commenced, the production line need not come to a halt. Changes can be implemented instantly with OTP EPROMs. Scrapping an entire stock of masked ROMs or waiting weeks for revised ROMs is no longer necessary.

For surface-mount and space constrained applications, PLCC EPROMs are ideal. The footprint of a PLCC requires only 1/3 the surface area of a conventional DIP EPROM. PLCCs provide additional usable board space because both sides of the printed circuit board can be used for device surface mounting. To keep pace with automated handling equipment, which is used extensively with PLCCs, production line programming equipment must have fast throughput times. Again, the Quick-Pulse Programming algorithm comes to the rescue. Coupled with auto-handlers, Quick-Pulse Programming equipment can place code in PLCC EPROMs on the production floor.

The primary benefit of plastic EPROMs and the Quick-Pulse Programming algorithm is throughput time (TPT). The Quick-Pulse Programming algorithm provides a significant increase in the number of units that can be programmed in a given time. Below is an example that compares a typical PROM programmer (using the int$_{e}$ligent Programming algorithm) with a state-of-the-art Quick-Pulse Programmer.

Although the int$_{e}$ligent Programmer in the example above is typical of high quality programmers on the market today, it can achieve a TPT of only 3% that of an optimized Quick-Pulse Programmer. To put this in production terms, a supply of EPROMs that previously required a month to program using conventional programming equipment can now be programmed in only half a day using Quick-Pulse Programming equipment.

The Quick-Pulse Programming algorithm is supported by many single socket programmers. Coupled with automatic handlers, these programmers can be used for automated programming. High performance gang programmers that approach theoretical Quick-Pulse Programming times are also available.

		Quick-Pulse Programmer	**Typical int$_{e}$ligent Programmer**
Auto Handler	time/part	0.5 sec/part	0.5 sec/part
Programming	time/part (256k)	4.0 sec/part	158 sec/part
Total	time/part	4.5 sec/part	158.5 sec/part
Total	units/hour	800 U/hour	22 U/hour
Total	units/month	139 kU/month	3.9 kU/month

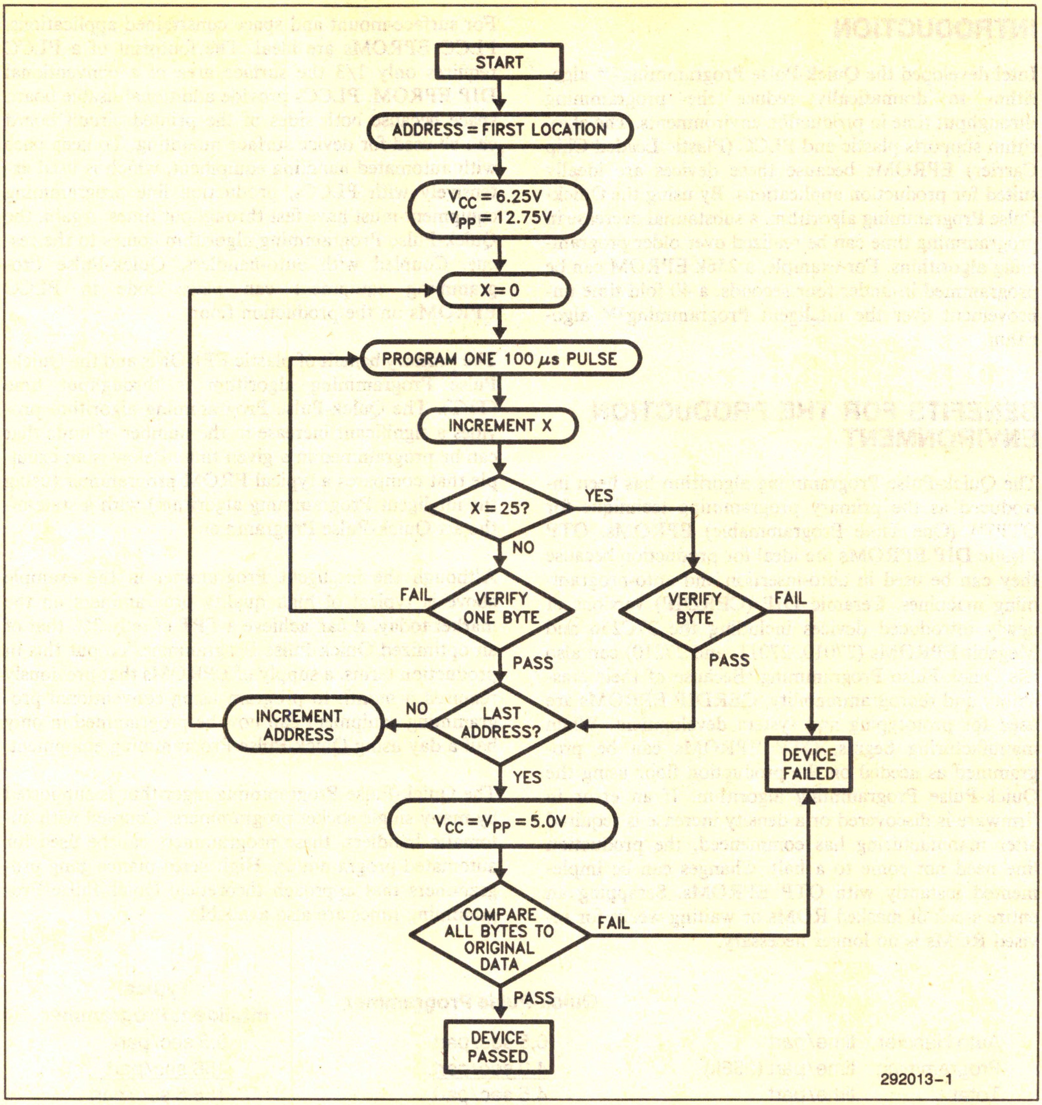

START
ADDRESS = FIRST LOCATION
VCC = 6.25V
VPP = 12.75V
X = 0
PROGRAM ONE 100 µs PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
DEVICE FAILED
VCC = VPP = 5.0V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
PASS
DEVICE PASSED
292013–1

Figure 1. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING CHARACTERISTICS

The Quick-Pulse Programming algorithm uses a higher VPP voltage than the int$_e$ligent Programming algorithm to provide greater programming energy. This leads to faster programming. Overprogramming pulses are eliminated by using a higher reference level to check cell charge margin. At the beginning of the programming sequence, V_{CC} is raised from 5.0V to 6.25V and V_{PP} from 5V to 12.75V. A 100 microsecond programming pulse is applied and immediately followed by a byte verification. Up to twenty-five program/verify cycles are provided per byte before a programming failure is recognized. When all bytes are programmed, V_{CC} and V_{PP} are lowered to their 5.0V read mode voltages. All bytes are then compared with the original data to confirm proper programming. A flowchart of the Quick-Pulse Programming algorithm is shown in Figure 1.

Table 1

EPROM	Theoretical Programming Times		int_eligent Identifier™	
	Quick-Pulse	Inteligent	Company	Device
P2764A	0.875 sec	32.86 sec	88	08
N27C64	0.875 sec	32.86 sec	88	07
N87C64	0.894 sec	32.87 sec	88	37
P27128A/N27128A	1.75 sec	65.71 sec	88	89
P27256	3.50 sec	131.29 sec	88	04
27C256/N27C256	3.50 sec	131.42 sec	89	86
P27512	7.04 sec	262.89 sec	88	0D
P27513	7.04 sec	262.89 sec	88	0F
27010/P27010	14.00 sec	525.69 sec	89	05
27011/P27011/N27011	14.00 sec	525.69 sec	89	85
27210/P27210/N27210	6.99 sec	262.84 sec	0089	00FF

Packaging Options: No prefix = Ceramic DIP, P = Plastic DIP, N = PLCC.

THEORETICAL PROGRAMMING TIMES

The Quick-Pulse Programming algorithm decreasees the program pulse to only 10% that of the int$_e$ligent Programming algorithm and eliminates the overprogram pulse. Idle time inherent in older programming algorithms has been drastically reduced by the shorter program pulse of the Quick-Pulse Programming algorithm. Theoretical programming times are most easily achieved if fast microprocessors and efficient programming code are used.

A comparison of minimum Quick-Pulse Programming and int$_e$ligent Programming times is shown in Table 1. With program-verify and read-verify times added to the programming time, the Quick-Pulse Programming algorithm achieves a 97% decrease in total programming time. Decrease of the program pulse width impacts most on the program/verify cycle time. Decreasing the total pulse time from a minimum of 4 ms (tPW + tOPW for the int$_e$ligent Programming algorithm) to 0.1 ms (Quick-Pulse Programming algorithm) results in dramatic program time reduction.

Data obtained during Quick-Pulse characterization of the 27C256 shows that over 87% of these devices program within 3.38 seconds and 99.7% within 5.8 seconds; the minimum program pulse time required for a 27C256 is 3.28 seconds. Figure 2 is a graph of the percent of 27C256 EPROM cells programmed versus the number of 100 µs pulses required. The Quick-Pulse Programming algorithm takes advantage of the fact that most EPROM cells program during the first 100 µs pulse.

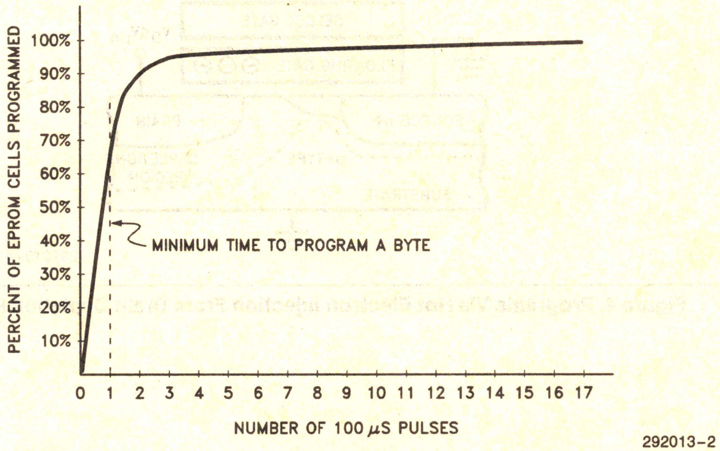


Figure 2. Pulses Required to Program 27C256 EPROM Cells

STORING DATA IN THE EPROM

The EPROM storage cell consists of a single MOS transistor with a floating gate (made of a layer of polysilicon surrounded by oxide layers) placed between the select gate and the substrate's diffusion layer. Figure 3 shows a simplified cross section of an EPROM cell. Data, representing a logic "0", is stored in the cell by placing electrons on the floating gate. The polysilicon-oxide interface creates a 3.1 eV potential barrier that traps these electrons on the floating gate. The absence of electrons on the floating gate represents an unprogrammed state; a logic "1".

Electrons are removed from the floating gate by exposure to ultra-violet (U.V.) light of wavelength 2537Å. Photons contained in the high frequency U.V. light are absorbed by these electrons. This places the electrons in a high energy state which allows them to overcome the 3.1 eV energy barriers of the interpoly oxide and gate oxide. With this energy the electrons are able to reach the Poly-2 layer (select gate) or substrate where they are removed from the cell.

Just as removing electrons (erasing) requires overcoming the energy barriers imposed by the gate oxide, programming requires energy to move electrons in the opposite direction. Placing a high voltage, V_{PP}, on the select gate and on the drain of the transistor allows programming (see figure 4). This potential causes electrons to be accelerated as they move from the source to the drain. Some of these electrons reach a high enough energy state to be drawn onto the floating gate.

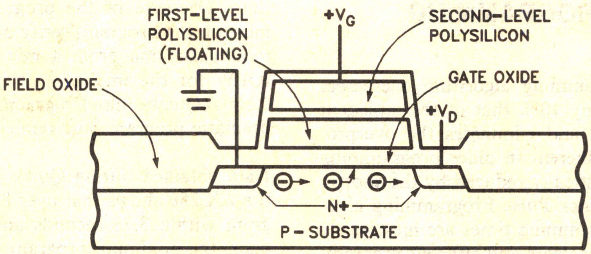

FIRST-LEVEL POLYSILICON (FLOATING)
+V_G
SECOND-LEVEL POLYSILICON
FIELD OXIDE
GATE OXIDE
+V_D
N+
P - SUBSTRATE
292013-3

Figure 3. EPROM Cell

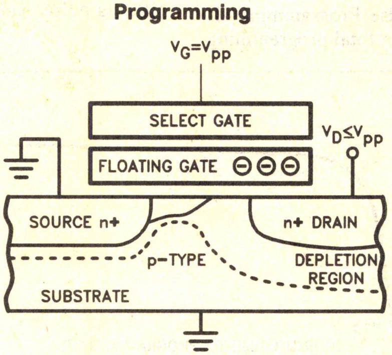

Programming
V_G=V_PP
SELECT GATE
V_D≤V_PP
FLOATING GATE
SOURCE n+
n+ DRAIN
p-TYPE
DEPLETION REGION
SUBSTRATE
292013-4

Figure 4. Programs Via Hot Electron Injection From Drain Depletion Region

More efficient programming of an EPROM cell is achieved by increasing the programming voltage, V_{PP}. As the programming voltage increases, the energy supplied to electrons as they accelerate through the channel increases. This energy allows "hot electrons" to overcome the potential barrier of the gate oxide. Since increasing the V_{PP} voltage makes for more efficient programming, the time required to place charge on the floating gate decreases. The Quick-Pulse Programming algorithm takes advantage of this.

Data stored in an EPROM cell is represented by the threshold voltage required to turn on the MOS transistor. In the Read Mode, information is requested from a cell by placing a voltage approximately equal to V_{CC} on the select gate. If the transistor turns on, a logic "1" is interpreted; if the transistor remains off, a logic "0" is detected. Programming an EPROM cell alters the threshold voltage required to turn on the transistor. The larger the number of electrons on the floating gate, the more effective is the blocking of the positive select gate voltage. Figure 5 shows the I-V relationships of programmed and unprogrammed EPROM cells.

To provide extra margin for V_{CC} fluctuations, EPROMs rated to operate at 5V ±10% must have programming margins that are at least 5.5V. The Quick-Pulse Programming algorithm monitors the cell charge margin by using a closed loop technique that is much more stringent than other algorithms. Applying 6.25V to V_{CC} allows the algorithm to detect marginally programmed cells.

PROGRAMMER DESIGN PRACTICES

Reliable programming of EPROMs requires more than just an efficient algorithm. Good design practices should be followed when designing a PROM programmer to ensure that timing parameters, voltage parameters, and sequencing of control signals are properly implemented.

The power supply that drives the EPROM to its programming levels should be well regulated. Circuit board traces should be short, low-inductance lines that are decoupled at V_{CC} and V_{PP} device inputs with high-frequency capacitors; typically 0.1 μF ceramic capacitors. In addition, a 4.7 μF electrolytic capacitor should be used between V_{CC} and GND for every eight devices. Planes for routing V_{CC} and GND should be used to reduce the effects of current surges and ground loops (see application notes AP-74 and AP-238, available from Intel literature).

Noise is the most common nemesis of programmer design. Voltage swings caused by switching circuitry can cause significant noise on V_{CC}, GND, V_{PP}, address, data, and control inputs. To reduce the effect of current surges caused by these voltage swings, decoupling capacitors and isolation of the programming socket(s) should be employed whenever possible. Overshoot and undershoot should be minimized to keep voltage parameters within the limits specified in the data sheets. A high-bandwidth oscilloscope (at least 150 MHz) should be used to monitor the signals at the programming socket (with EPROM inserted).

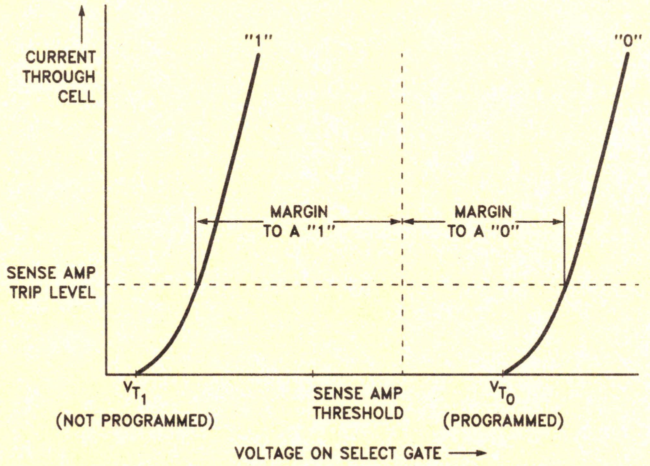


Figure 5. Read Operation

Since V_{PP} is the highest voltage applied to an EPROM, it is closest to the physical limits of the device. A V_{PP} voltage above 14.0V for any length of time will cause permanent damage to the EPROM. Proper decoupling capacitors should be placed at all V_{PP} inputs to help prevent damage caused by transients. Again, a high-bandwidth oscilloscope should be used to look for overshoot when adjusting V_{PP}.

Clean switching of V_{CC} and V_{PP} voltages will help ensure proper programming. Circuits for switching these voltages are easily built. Article reprint AR-294, which can be ordered from Intel's literature department, has example circuits that can be used to cleanly switch V_{CC} and V_{PP} from 5V to their programming voltages. These switching circuits also allow V_{CC} and V_{PP} to be switched off so EPROMs are not hot-socketed when they are inserted and removed.

SUMMARY

Production of electronic equipment requires programmable memory devices that can be used in auto-test and auto-insertion machines. Electronic systems also require program memory that can be changed easily when code crashes or program errors occur. Plastic and PLCC EPROMs provide solutions to both of these needs. They can be used in automated test and manufacturing equipment, and code changes can be implemented immediately. To reduce the programming times of these devices to accommodate production-line speeds, Intel has developed the Quick-Pulse Programming algorithm. Intel's line of plastic EPROMs can now be tested, quickly programmed, and mounted on circuit boards by totally automated production equipment.

APPLICATION NOTE

October 1986

Using Page-Addressed EPROMS

TERRY KENDALL
APPLICATIONS ENGINEERING
PROGRAMMABLE MEMORY OPERATION

© Intel Corporation, 1986

Order Number: 292020-001

INTRODUCTION

For several years, eight-bit systems have been a mainstay of computerized systems. There are some very good reasons for this. The instruction sets of most 8-bit microprocessors and microcontrollers are very rich. Basic operations—move, jump, arithmetic, and logical—are common to all. These CPUs can perform the vast majority of functions available in later generation processors, but at a different performance level. 8-bit machines are entrenched in thousands of applications and are more than adequate for many new ones. So, why are 16-bit processors replacing their smaller cousins in new systems?

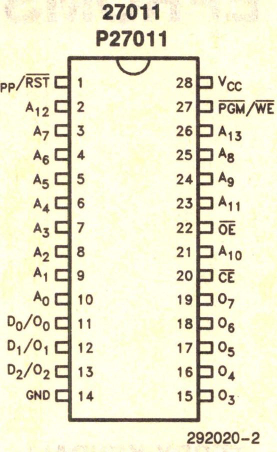
Part of the reason, of course, is the more powerful data manipulation made possible by the wider word width. Many 8-bit systems, however, are redesigned with 16-bit processors simply because extended memory addressing capability is needed. Most existing 8-bit systems function adequately, but 64 kilobytes of memory addressing is too small to accommodate RAM and constantly maturing program memory. The instruction sets of 8-bit processors usually suffice for new applications as well, except for the address constraint. Many 16-bit systems have predefined segments set aside for program memory. Additional program memory can not be expanded without intruding on RAM memory space.

Bank switching is a good way of providing additional program memory to address limited systems. A few logic gates, latches, decoders, ample circuit board space, and a lot of memory chips allow designers to provide virtual program memory capability to any system. This solution, although not ideal, can be implemented in new designs, but what happens when an existing design requires additional program memory? Board real estate is non-existent and a hardware redesign to implement bank switching is a very costly proposition.

An ideal solution to this problem would be one that implements a form of bank switching with no extra hardware, not even additional memory devices. An even better solution would allow for future growth in the system's program memory.

This "no extra hardware" expansion of program memory is now possible with Intel's page-addressed (paged) EPROM family. These devices allow 8-bit, 16-bit, 32-bit, . . . systems utilizing 27128 EPROMs to quadruple or octuple their program memory space with only a plug-in replacement. In addition, the page addressing scheme allows for future density upgrades to 4 Megabytes! within the same 28-pin (32-pin PLCC) footprint. Figure 1 shows the pin configurations for paged EPROMs and their relationship to other 28-pin DIP and 32-pin PLCC EPROMs.

4 M-bit	2 M-bit	27513	27128A
$V_{PP}/\overline{RST}$	$V_{PP}/\overline{RST}$	$\overline{RST}$	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	D_0/O_0	D_0/O_0	O_0
D_1/O_1	D_1/O_1	D_1/O_1	O_1
D_2/O_2	D_2/O_2	O_2	O_2
GND	GND	GND	GND



27128A	27513	2 M-bit	4 M-bit
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{WE}$	$\overline{PGM}/\overline{WE}$	$\overline{WE}$
A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	D_4/O_4
O_3	O_3	D_3/O_3	D_3/O_3

292020-2

Figure 1a. Cerdip(D)/Plastic(P) DIP Pin Configurations

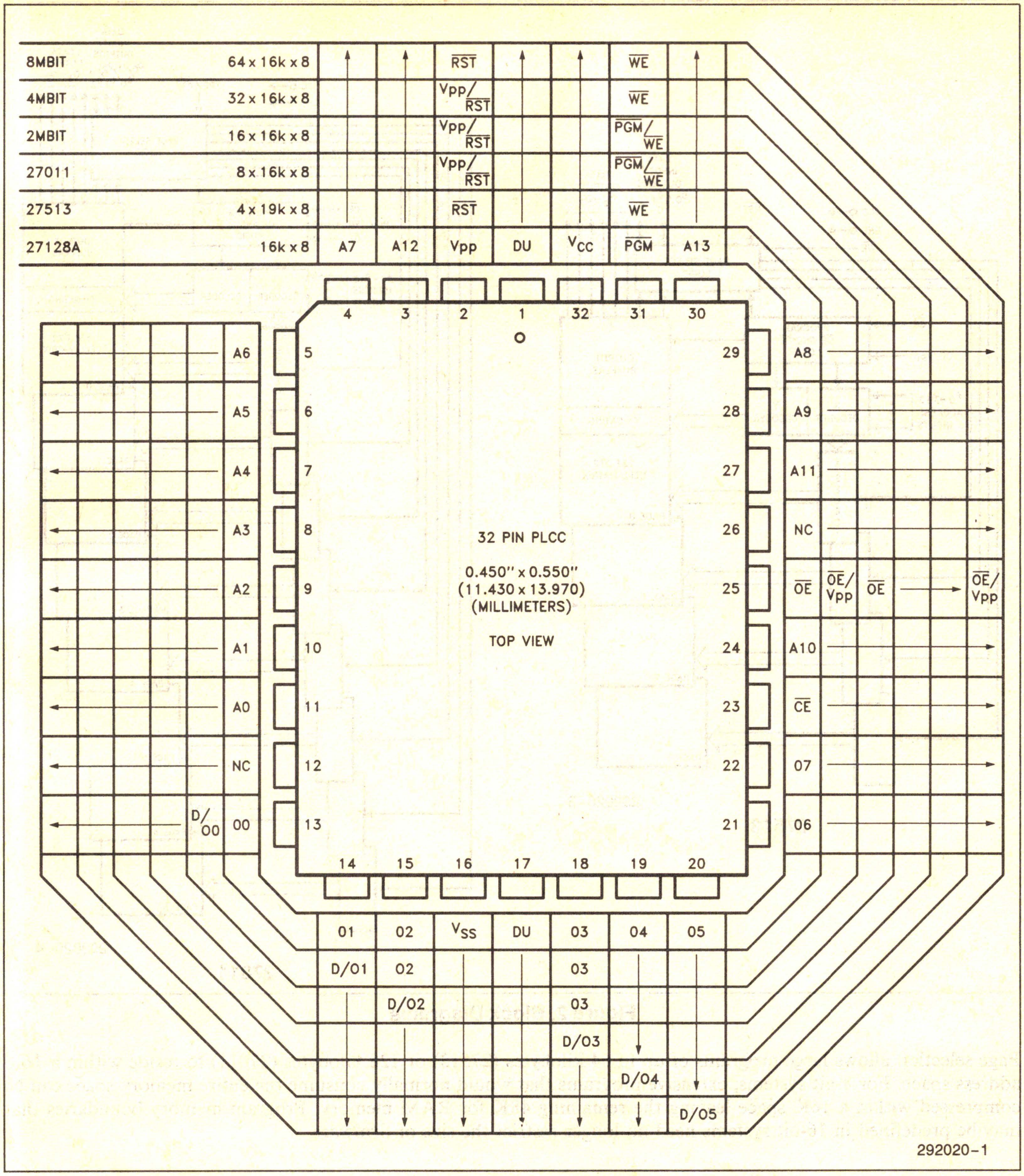
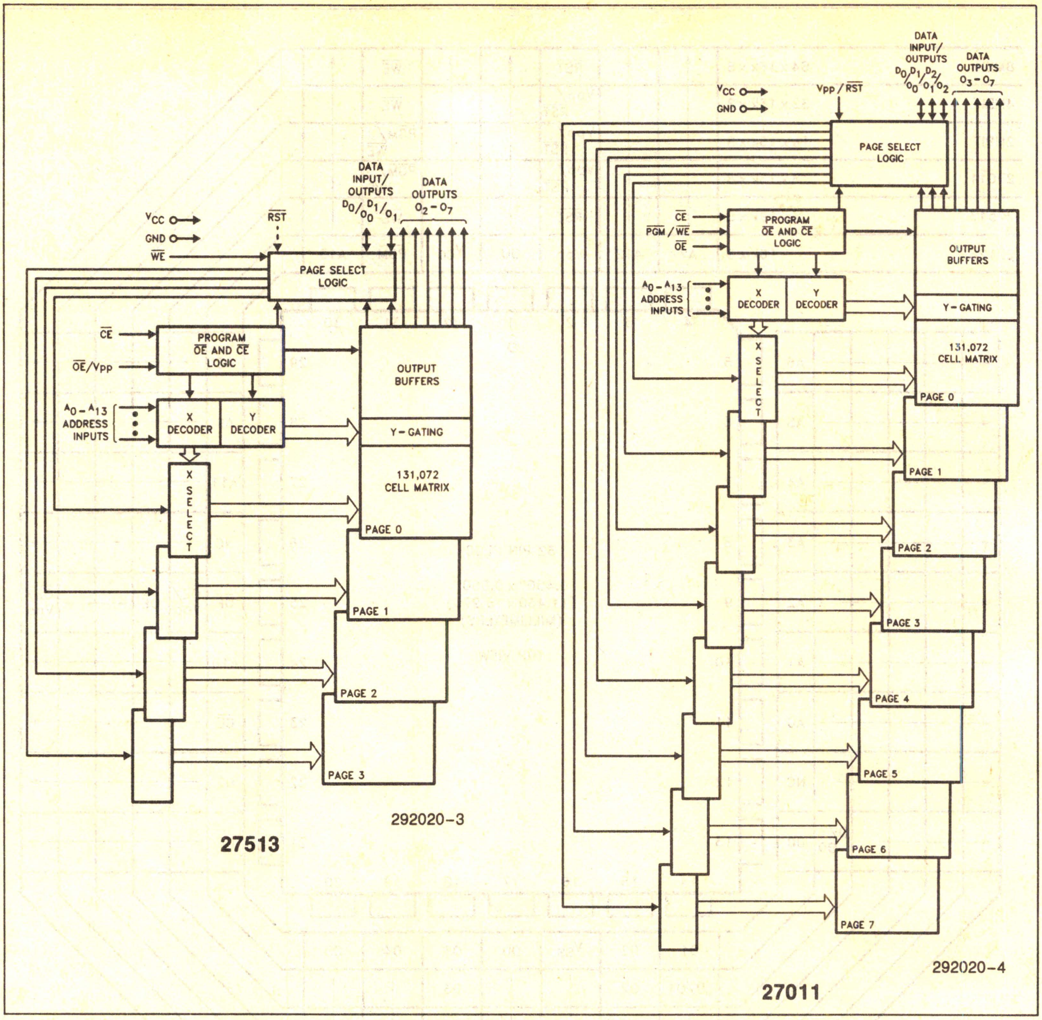

8MBIT
64 x 16k x 8
4MBIT
32 x 16k x 8
2MBIT
16 x 16k x 8
27011
8 x 16k x 8
27513
4 x 19k x 8
27128A
16k x 8
A7
A12
Vpp
DU
VCC
PGM
A13
RST
Vpp/RST
WE
PGM/WE
4
3
2
1
32
31
30
A6
A5
A4
A3
A2
A1
A0
NC
D/00
00
5
6
7
8
9
10
11
12
13
29
28
27
26
25
24
23
22
21
A8
A9
A11
NC
OE
OE/Vpp
A10
CE
07
06
32 PIN PLCC
0.450" x 0.550"
(11.430 x 13.970)
(MILLIMETERS)
TOP VIEW
14
15
16
17
18
19
20
01
02
VSS
DU
03
04
05
D/01
D/02
D/03
D/04
D/05
292020-1

Figure 1b. PLCC(N) Lead Configuration

The 27513 is a 64 kilobyte EPROM organized as four 16 kilobyte pages that fits within a single 16K address space. Address-constrained applications that require more than 64K of program memory can benefit by using Intel's 1 megabit (128K byte) page-addressed EPROM, the 27011. The 27011 provides eight 16K pages within a single 16K memory space and is fully hardware compatible with the 27128 and 27513 EPROMs. Figure 2 shows the block diagram of paged EPROMs. Refer to data sheets for further details.


VCC
GND
WE
RST
DATA INPUT/ OUTPUTS
D0/O0 D1/O1
DATA OUTPUTS
O2 - O7
PAGE SELECT LOGIC
CE
OE/Vpp
PROGRAM OE AND CE LOGIC
A0 - A13 ADDRESS INPUTS
X DECODER
Y DECODER
OUTPUT BUFFERS
Y - GATING
131,072 CELL MATRIX
X SELECT
PAGE 0
PAGE 1
PAGE 2
PAGE 3
292020-3
VCC
GND
Vpp / RST
DATA INPUT/ OUTPUTS
D0/O0 D1/O1 D2/O2
DATA OUTPUTS
O3 - O7
PAGE SELECT LOGIC
CE
PGM / WE
OE
PROGRAM OE AND CE LOGIC
A0 - A13 ADDRESS INPUTS
X DECODER
Y DECODER
OUTPUT BUFFERS
Y - GATING
131,072 CELL MATRIX
X SELECT
PAGE 0
PAGE 1
PAGE 2
PAGE 3
PAGE 4
PAGE 5
PAGE 6
PAGE 7
292020-4

27513

27011

Figure 2. Block Diagrams

Page selection allows large programs of up to 64 kilobytes (27513) or 128 kilobytes (27011) to reside within a 16K address space. For 8-bit systems, extensive programs that would normally consume the entire memory space can be compressed within a 16K space leaving the remaining 48K for RAM memory. Program memory boundaries that may be predefined in 16-bit systems need no longer restrict the size of firmware.

Page segmentation allows discrete applications or overlays to reside within the same program address space. For example, using separate pages, a personal computer can have its operating system, diagnostic routines, high level languages, and specialized software packages reside within the same physical address space. Word processing, spreadsheet, and CAD applications require large amounts of RAM to store data. Using program overlays rather than RAM to hold the driver software keeps RAM memory free for user data. Each application is invoked by issuing a software command, either manually or by pressing a function key on the terminal.

The upgrade path provided by page addressed EPROMs allows for density increases using a method similar to bank switching but without the extra hardware or address space (and associated decoding circuitry). The need for a decoded location in the memory map dedicated to a special bank select latch is eliminated by the on chip latch located within the inherently free writable locations of the EPROM's memory space.

Switching to a new bank, or page in 27513 and 27011 nomenclature, is accomplished by simply selecting the device and writing the page number, via the data lines, to any address within the device's address range. Since the page latch is internal and is within the device's address range, no separate access to an outside location is required to change the bank. An index register can point to a destination within the chip's address range, and, because it points to the chip, can also be used to perform the page change. This will become clear when page turning algorithms are discussed.

DEVICE OPERATION

The 27513 and 27011 have identical read and page-select modes. Since programming is unique for each, refer to operation tables in each device's data sheet for program signal inputs.

Two-Line Control

Since EPROMs are generally used in memory arrays, two-line control provides lower system power consumption and assures that output/data bus contention will not occur. The $\overline{\text{CE}}$ and $\overline{\text{OE}}$ inputs control the device output drivers but do so in different ways. The $\overline{\text{CE}}$ input should be decoded from the address bus and used as the primary device selection control. $\overline{\text{OE}}$ should be a common connection to $\overline{\text{OE}}$ inputs of all system memory devices and the system's control bus $\overline{\text{READ}}$ line. Connecting $\overline{\text{CE}}$ and $\overline{\text{OE}}$ in this manner assures that all de-selected devices are in their low-power standby mode and that the data bus is driven only by outputs of selected devices.

In Page-Select Mode, the $\overline{\text{CE}}$ input is used to determine the memory device to be written to when the $\overline{\text{WE}}$ input is active ($\overline{\text{WE}}$ = VIL). This allows $\overline{\text{WE}}$ inputs of all memory devices to be tied together and controlled by the $\overline{\text{WRITE}}$ line of the system control bus.

Paged EPROMs are easily retrofitted into existing EPROM sockets. One jumper change is all that is required. Pin 27, which is connected to 5V on 27128 EPROMs, is connected to the system $\overline{\text{WRITE}}$ line in paged EPROM applications. All future paged EPROMs and the compacted HMOS II-E version of the 27513 will have a $\overline{\text{RST}}$ input on pin 1 that can be connected to the system's active low $\overline{\text{RESET}}$ line. This will provide automatic page zero reset when the system is reset. See Figure 3 for these connections.

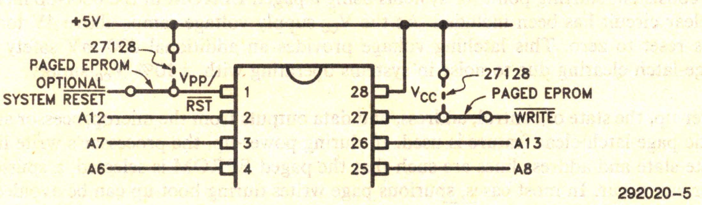

+5V
27128
PAGED EPROM
OPTIONAL SYSTEM $\overline{\text{RESET}}$
V_{PP}/$\overline{\text{RST}}$
A12
A7
A6
1
2
3
4
28
27
26
25
V_{CC}
27128
PAGED EPROM
$\overline{\text{WRITE}}$
A13
A8
292020-5

Figure 3. Single Jumper Change for Paged EPROM in Read and Write Modes

STANDBY and CHIP ENABLE Modes

Standby mode reduces the maximum EPROM current whenever data is not required from the EPROM. Standby mode is entered any time $\overline{\text{CE}}$ is at a TTL-high. All other mode select inputs ($\overline{\text{OE}}$ and $\overline{\text{WE}}$), are don't care, and outputs are in a high impedance state. The active mode ($\overline{\text{CE}}$ = VIL) allows the EPROM to enter the read, page-select, or program modes.

READ Mode

Information is obtained from the EPROM when it is placed in the read mode. This mode is entered when the device is selected ($\overline{\text{CE}}$ = VIL), the page-select (or write) mode is disabled ($\overline{\text{WE}}$ = VIH), and the outputs are enabled ($\overline{\text{OE}}$ = VIL). Outputs of all memory devices in the system can be connected directly to the data bus. Two-line control ensures that bus conflict is avoided by enabling only the outputs of the selected device.

PAGE-SELECT (WRITE) Mode

The page-select (or write) mode is entered by applying a TTL-low signal to the chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs. This mode allows for random access to any page. Individual page selection is accomplished by selecting the chip ($\overline{\text{CE}}$ = VIL) and writing ($\overline{\text{WE}}$ = VIL) the page number, via the data inputs, to the device ($\overline{\text{OE}}$ = VIH). Table 2 shows the data required to perform a page change. When a page change occurs in the middle of a program sequence, the processor's program counter status must be considered. After a page-select write, the program counter will point to the physical location immediately following the write instruction. Since this location is on a new page, it contains code that may not be valid for program continuation. Therefore, proper sequencing of the page change events is necessary. Procedures to accomplish this are described in later sections of this application note.

Table 1. Page Selection Data

Input/Output Page Selection			D_2/O_2	D_1/O_1	D_0/O_0
27011	27513	Select Page 0	V_{IL}	V_{IL}	V_{IL}
		Select Page 1	V_{IL}	V_{IL}	V_{IH}
		Select Page 2	V_{IL}	V_{IH}	V_{IL}
		Select Page 3	V_{IL}	V_{IH}	V_{IH}
		Select Page 4	V_{IH}	V_{IL}	V_{IL}
		Select Page 5	V_{IH}	V_{IL}	V_{IH}
		Select Page 6	V_{IH}	V_{IH}	V_{IL}
		Select Page 7	V_{IH}	V_{IH}	V_{IH}

Automatic Page-Latch Clear

To ensure a consistent starting point for systems using a paged EPROM in the boot-up memory space, an automatic page-latch clear circuit has been included. As the V_{cc} supply voltage ramps above 4V to its operating voltage, the page-latch is reset to zero. This latching voltage provides an additional 500 mV safety margin to guard against spurious page-latch clearing due to noise in systems operating with ± 10% V_{cc} supply.

During power-up, the state of control, address, and data outputs from the microprocessor should be considered when the automatic page-latch clear feature is used. If, during power-up, the processor's write line is in a TTL-low or an indeterminate state and address lines are such that the paged EPROM is selected, a spurious write of an undesired page number can occur. In most cases, spurious page writes during boot-up can be avoided by connecting a pull-up resistor (1K to 10 KΩ) between the $\overline{\text{WE}}$ pin and V_{cc}.

Relative Addressing

At power-up the device is automatically reset to page zero allowing program execution to begin from a known location in the EPROM memory. For example, 8085 systems automatically begin execution at location 0000H on page zero and continue sequential operation until the 16K page boundary is encountered. At that time, a program sequence can change the EPROM to page 1 and reset the program counter to 0000H allowing program execution to continue on the new page. This means that all address locations within the paged EPROM are relative to the base address of the device (in this case location 0000H). Jumps and calls within a page are easily accomplished using relative addressing, as opposed to absolute addressing. This is consistent with modular programming techniques and allows for flexible code structure in the paged format.

DEVICE PROGRAMMING

The programming mode is entered when the V_{PP} input is at its programming voltage. A byte of data is stored when the programming input is pulsed to a TTL-low. Data to be programmed is applied 8 bits in parallel to the data output pins. Levels required for the address and data inputs are TTL. Refer to data sheets for parameters, algorithms, and programming inputs used to program paged EPROMs.

Program Inhibit

Programming of multiple paged EPROMs in parallel with different data is easily accomplished using the program inhibit mode. A TTL-high level on the $\overline{CE}$ input will prevent programming of a device. This allows normal chip enable circuitry to select the particular EPROM to be programmed. Except for $\overline{CE}$, and $\overline{OE}$ in certain gang programming applications, all control inputs and bus lines of parallel EPROMs may be common.

Program Verify

A verify (read) should be performed on the programmed bytes immediately following the program pulse to determine that they have been correctly programmed. Data is read with V_{CC} and V_{PP} at their programming voltages and $\overline{OE}$ and $\overline{CE}$ at VIL. See the data sheets for programming voltages and proper sequencing of device control inputs.

TYPICAL PAGED EPROM/8085 SYSTEM

Hardware

A first approach to understanding the hardware and software considerations for interfacing a paged EPROM to a microsystem can be seen by analyzing the operation of a single paged EPROM in an 8085 8-bit microprocessor system. Paged EPROMs are easily incorporated into 16-bit systems by using techniques similar to those described below for 8-bit systems. Also, see Appendix D for an example that uses paged EPROMs in an 8086 system. Figure 4 shows the configuration of a basic 8-bit system.

System boot-up during power-up initializes the EPROM to page zero. This automatic feature of the page-latch circuit is meant to ensure consistent page selection when power is first applied. Similar to other microprocessors, the 8085 begins program execution at location 0000H after power-on or reset. Bootstrap initialization or vectoring routines should be located at 0000H of page 0.

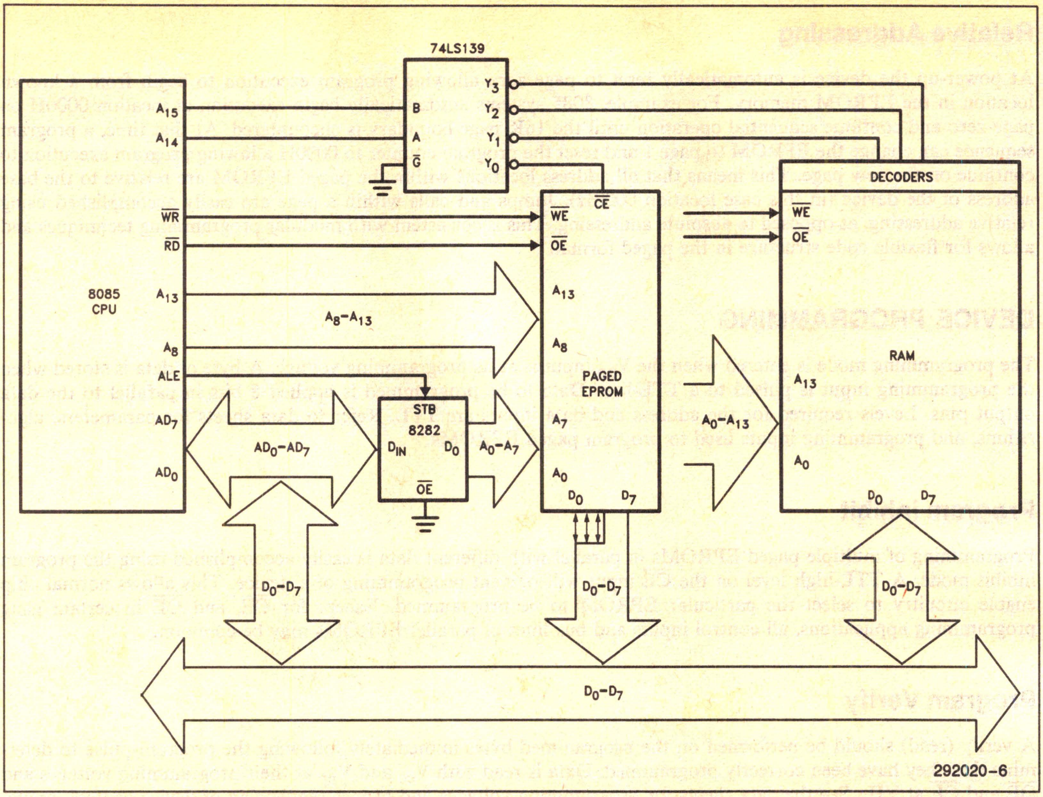

74LS139
Y3
Y2
Y1
Y0
B
A
G
8085 CPU
A15
A14
WR
RD
A13
A8
ALE
AD7
AD0
A8–A13
STB
8282
DIN
D0
OE
AD0–AD7
A0–A7
D0–D7
CE
WE
OE
A13
A8
PAGED EPROM
A7
A0
D0
D7
D0–D7
A0–A13
DECODERS
WE
OE
RAM
A13
A0
D0
D7
D0–D7
D0–D7
292020–6

Figure 4. Basic 8-bit Microsystem

Unlike power-up, a hardware reset or software "RST" command will not automatically select page zero on early 27513 versions. A simple software routine can be placed at location 0000H of other pages to accomplish page 0 selection. A two line (6 byte) sequence to select page 0 is:

```
0000  MVI  H,0000H    ;HL register points to reset location.
0003  JMP  TURNTO_0   ;Jump to routine that changes to page
                      ;0 and begins execution at location
                      ;0000 (HL register).
```

Page selection routines are discussed in the next section.

Software Page Selection

Performing a page change involves proper sequencing of two events: 1) selecting the new page and 2) moving to the appropriate relative location on it. Although this sounds simple, which step should be performed first? After the first step is executed, how is the other performed if information about it resides on the page just left by the program?

The solution is a two-fold approach that 1) places the relative destination in a secure location where it can be retrieved no matter what page or what location is pointed to by the program counter, and 2) continues the program flow on the new page as if no page change had occurred (see Figure 5). Following is a discussion of methods for implementing these steps in a simple 8-bit (8085) microprocessor driven system. Keep in mind that these same techniques can be used when paged EPROMs are incorporated in word-wide systems.

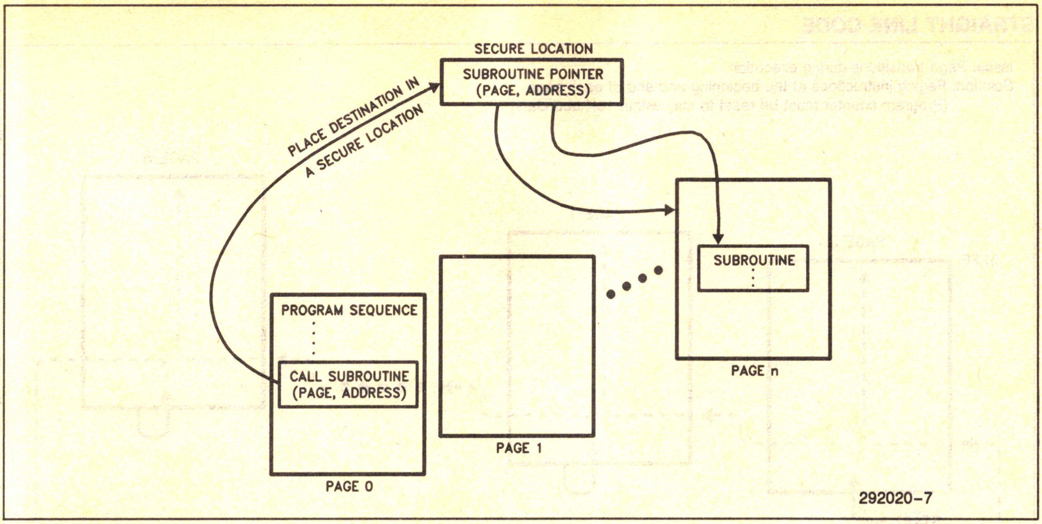

SECURE LOCATION
SUBROUTINE POINTER (PAGE, ADDRESS)
PLACE DESTINATION IN A SECURE LOCATION
PROGRAM SEQUENCE
CALL SUBROUTINE (PAGE, ADDRESS)
PAGE 0
PAGE 1
SUBROUTINE
PAGE n
292020-7

Figure 5. Saving the Destination Pointer

PROGRAMMING TECHNIQUES

Program execution is most commonly performed using one of three techniques: Contiguous coding, discrete application overlays, or modular programming.

Contiguous Coding

The first technique, contiguous coding, is easily accomplished in paged applications by duplicating a simple two-statement software routine at the beginning of each page. This routine writes the number of the next sequential page to the EPROM which changes the page and continues execution at the next relative sequential location on the new page. A one line jump statement at the end of a page boundary re-directs program execution to this page turning routine. For an 8085 system, the page turning routine would be as follows:

```
LOCATION  SOURCE       STATEMENT
0000      CHANGEPG     MVI A,next page number.
0002                   STA Any location within the EPROMs address range.
0005      program continuation
```

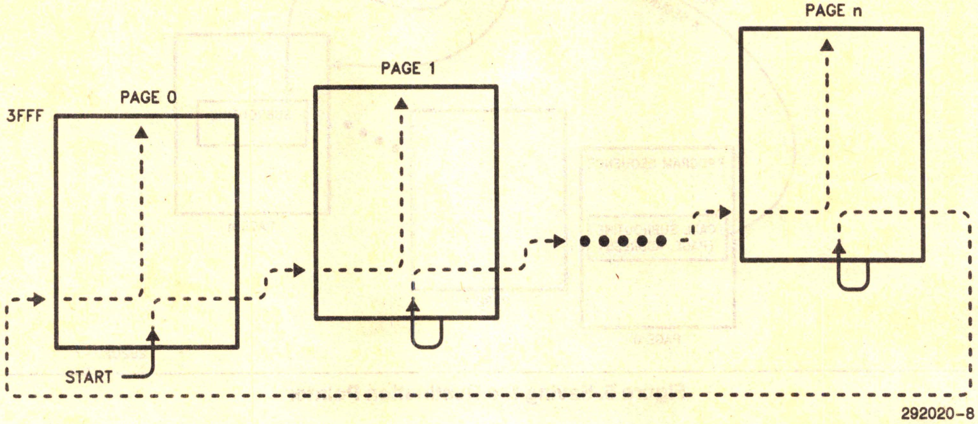
The following statement at the end of the page requests this routine:

```
3FFD      NEXTPG       JMP CHANGEPG
```

Although power-up automatically resets the EPROM to page zero, the page change instructions at the beginning of page zero cause the application software to begin execution at location 0000H on page one. Figure 6 illustrates this technique.

STRAIGHT LINE CODE

Issue: Page transitions during execution.
Solution: Paging instructions at the beginning and end of each page.
(Program counter must be reset to stay within 16K boundary)



Sample instructions for 8085:

			3FFD	C3
Beginning of page 0	JMP	0000	3FFE	00
			3FFF	00
			0000	3E
	MVI	A,01H	0001	01
End of page 0			0002	32
	STA	"PAGED EPROM"	0003 0004	"PAGED EPROM"

—Program Execution Begins at Location 0005

Figure 6. Contiguous Coding

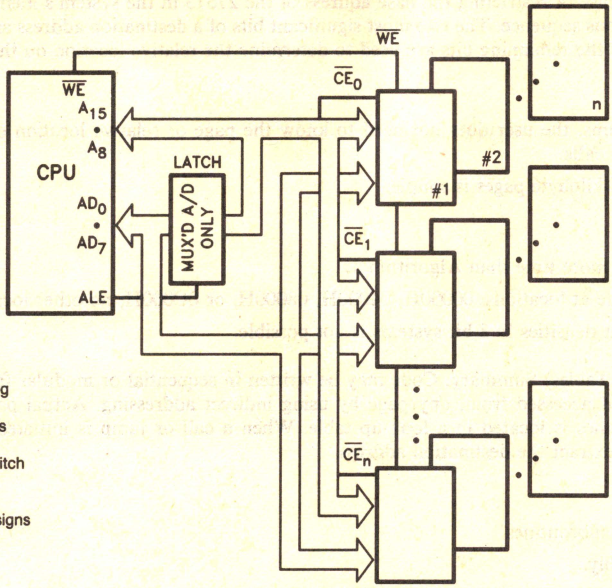
Discrete Applications

The second technique uses the paged EPROM in discrete application overlays. Each page contains all the system information required for individual software applications to stand alone in their control of system operation. A small section at the same location on each page is set aside to handle page-change routines. Another application is requested by a software or function key command that directs the microprocessor to the routine below.

```
APPONE   LXI  H,starting address of page 0 application.
         MVI  M,00H          ;"HL" (M) points to page 0. Next
                             ;instruction continues on page zero.
         PCHL                ;Jump to Application-one.
APPTWO   LXI  H,starting address of page 1 application.
         MVI  M,01H
         PCHL
         etc.
```

A block diagram for discrete system options is shown in Figure 7.

DISCRETE SYSTEM OPTIONS



- No page transitions during execution.
- Paged EPROM treated as consecutive 27128s.
- Hardware or software switch changes pages to new applications software.
- 4X or 8X upgrade for designs currently using 27128s.

292020–9

Figure 7. Paged EPROM's In Discrete Applications

Modular Programming

The third technique, modular programming, is a common and desirable means for implementing application software. This technique requires special considerations for paged EPROMs. Three algorithms for inter-page calls and jumps are discussed in the next section.

SYSTEM IMPLEMENTATION

Three page turning algorithms—Manual Paging, Automatic Paging, and Look-Up Tables—are summarized below in the context of three different hardware configurations—Paged EPROM only, Paged EPROM + Small EPROM, and Paged EPROM + RAM. An 8085 system is used for illustrative purposes, but these implementations can also be used with word-wide systems, except for algorithm 2 (Automatic Paging).

Algorithm 1 (Manual Paging) Summary: This algorithm relies on the ability of the programmer to determine the page and relative location that subroutines inhabit. These two pieces of information must be manually supplied when a subroutine on a different page is called.

Advantage:

- The most direct and most easily understood approach.
- Provides for fast page changes.
- Upgrades easily to megabit page-addressed EPROM applications.

Disadvantage:

- Programmer must know the page and relative location for every call and jump.
- Assembler won't supply this information and has trouble with labels that reference unknown addresses on another page.

Algorithm 2 (Automatic Paging) Summary: Automatic paging is applicable to the 27513 only in 8-bit (16-bit addressing) applications. This method allows the programmer to write code in a more conventional, sequential manner but at the expense of restricting the base address of the 27513 in the system's memory map. Programs are assembled as a contiguous sequence. The two most significant bits of a destination address are used to determine the page (one of four), and the remaining bits are used to determine the relative location on that page.

Advantage:

- While writing programs, the user does not need to know the page or relative location on that page of routines accessed by jumps or calls.
- Segmentation into 16 kilobyte pages is simple.

Disadvantage:

- A page change takes more time than Algorithm 1.
- The 27513 must reside at locations: 00000H, 04000H, 08000H, or 0C000H; no other locations are allowed.
- Upgrading to megabit densities in 8-bit systems is not possible.

Algorithm 3 (Look-up Tables) Summary: Code may be written in sequential or modular form. Global subroutines may be located on, and accessed from, any page by using indirect addressing. Actual page and relative address information of subroutines is located in a look-up table. When a call or jump is initiated, a pointer to the table information is used to extract the destination address.

Advantage:

- Fast access to global subroutines.
- Easy program assembly.
- Easy upgrades to megabit page addressed EPROM applications.

Disadvantage:

- Large look-up tables can occupy significant portions of memory.
- A page change takes a little more time than Algorithm 1.

Algorithm 1: MANUAL PAGING.

This page change algorithm allows for fast jumps and calls to another page. The page of residence for destinations must be determined by the user and supplied with each call and jump instruction. To implement this procedure, one register must be dedicated to the system for current page information and an index register pair must be made available at the time a call, jump, or return to/from a subroutine is made. In the following 8085 example, the "D" register contains the current page number, which is initialized to 00H (page zero) during boot-up, and the "HL" register points to the destination address. This group of routines must be located at the same relative address on every page.

```
SOURCE     STATEMENT
PAGE_0     PUSH       D                 ;Save the current page number.
TURNTO_0   MVI        D,00              ;Change current page identifier.
           MOV        M,D               ;Writing the page number "D" to where
                                        ;"HL" points (EPROM) changes the page.
                      PCHL              ;Change Program Counter to begin at
                                        ;desired location on new page.
PAGE_1     PUSH       D
TURNTO_1   MVI        D,01
           MOV        M,D
           PCHL
           .
           .
           .
PAGE_n     PUSH       D                 ;n=3 for the 27513,n=7 for the 27011.
TURNTO_n   MVI        D,n
```

```
        MOV     M,D
        PCHL
RETURN  POP     D               ;Retrieve old page number.
        POP     H               ;"HL" points to old return address.
        MOV     M,D             ;"HL" points to EPROM; Change the page.
        PCHL                    ;The program counter is loaded with the
                                ;return address.
```

Calling a routine on another page is accomplished by the programming sequence:

```
GETSUB  LXI     H,routine       ;Load "HL" with destination address.
        CALL    PAGE_n          ;Call the subroutine to turn to page
                                ;n=0, 1, 2, ... The CALL instruction
                                ;may be a conditional call since LXI H
                                ;does not affect the flags register.
```

Nested calls to any depth (limited only by the RAM space available to the system stack) are supported with guaranteed returns to the calling routine. One statement at the end of a subroutine will facilitate a return to the calling routine (to its proper page number). The usual return instruction (RET or conditional return) is replaced by

```
        JMP     RETURN          ;A conditional return would use its
                                ;equivalent jump cousin.
```

Jumps to a location on another page do not require that the current page or return address be saved. Only a page change and a jump to the destination are required. This is accomplished by the two program statements:

```
        LXI     H,destin        ;"HL" gets the destination address.
        JMP     TURNTO_n        ;Jump to the standard routine to turn
                                ;the page to n = 0, 1, 2, ... JMP may
                                ;be replaced by a conditional JMP.
```

Figure 8 shows the program flow during page changes.

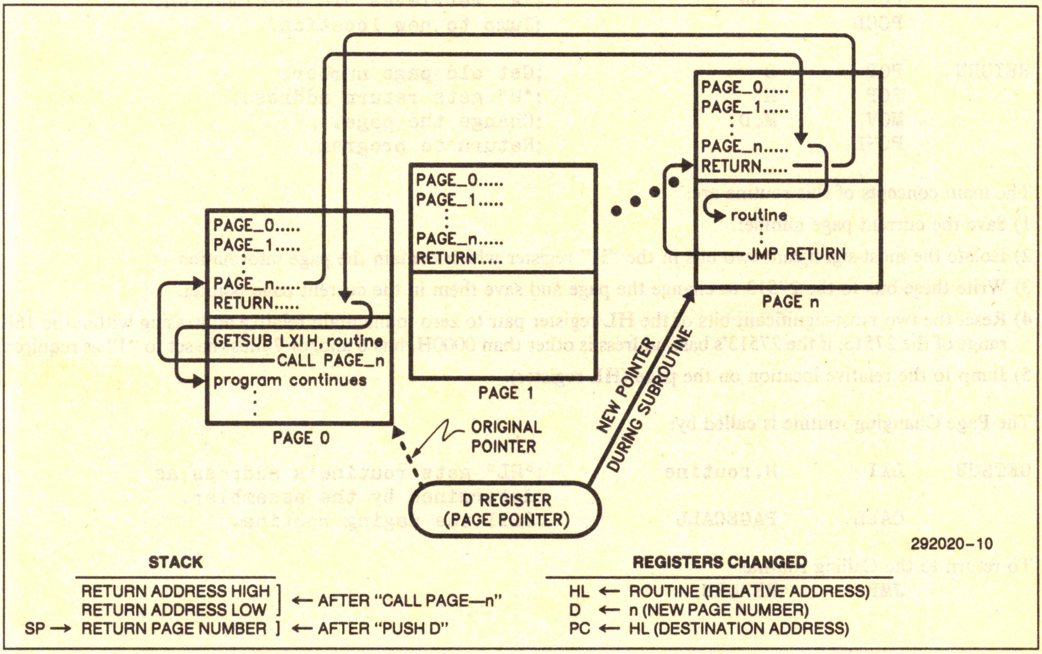

PAGE_0.....
PAGE_1.....
PAGE_n.....
RETURN.....
GETSUB LXI H, routine
CALL PAGE_n
program continues
PAGE 0
PAGE_0.....
PAGE_1.....
PAGE_n.....
RETURN.....
PAGE 1
PAGE_0.....
PAGE_1.....
PAGE_n.....
RETURN.....
routine
JMP RETURN
PAGE n
NEW POINTER DURING SUBROUTINE
ORIGINAL POINTER
D REGISTER (PAGE POINTER)
292020-10
STACK
RETURN ADDRESS HIGH
RETURN ADDRESS LOW
← AFTER "CALL PAGE—n"
SP → RETURN PAGE NUMBER
← AFTER "PUSH D"
REGISTERS CHANGED
HL ← ROUTINE (RELATIVE ADDRESS)
D ← n (NEW PAGE NUMBER)
PC ← HL (DESTINATION ADDRESS)

Figure 8. Changing Pages with Algorithm 1

Assembling the Program

Program assembly is a two-stage process. Program code for each segment (page) is written as a distinct 16K program; this anticipates assembly problems caused by duplicate addressing inherent in the stacked-page format. The first assembly of each page will generate an error for each label reference that does not reside on the assembled page. A master equate table can be formed by merging the equate tables of each page generated during the first round of assembly. This master table is then used to re-assemble all the pages.

Algorithm 2: AUTOMATIC PAGING (27513 only)

The second algorithm allows a programmer to write code in an uninterrupted manner and assemble the finished program as a single block (up to 64K) without having to discern the page on which a subroutine resides. Figure 10 shows the assembled code and its segmentation into separate pages. This is accomplished by using the two most-significant bits of a destination address as determined during normal assembly of the program. The two most-significant bits hold the page number information (one of four pages) and the remaining bits hold the relative location on the page of the desired routine. As described in Algorithm 1, calls and jumps to routines are not made directly. An intermediate step is required to move to another page. The following page change routine resides at identical relative locations on each page.

```
SOURCE    STATEMENT
PAGECALL  PUSH      D               ;Save old page number.
PAGETURN  PUSH      PSW             ;Save anything in "A".
          MOV       A,H             ;"A" gets high address byte.
          RLC       A               ;Rotate "A" to get two
          RLC       A               ;most-significant bits.
          ANI       00000011B       ;Reset bits 2-7.
          MOV       D,A             ;Bits 0 and 1 are the page number.
          MVI       A,00111111B     ;"A" gets mask bits.
          ANA       H               ;Strip off MS bits of "H".
          MOV       H,A             ;New high-address byte back to "H".
          MOV       M,D             ;Change the page of 27513.
          POP       PSW             ;"A" retrieves old information.
          PCHL                      ;Jump to new location.

RETURN    POP       D               ;Get old page number.
          POP       H               ;"H" gets return address.
          MOV       M,D             ;Change the page.
          PCHL                      ;Return to program.
```

The main concepts of this routine are:

1) Save the current page number.

2) Isolate the most-significant two bits in the “H” register which contain the page information.

3) Write these bits to the 27513 to change the page and save them in the current page pointer.

4) Reset the two most-significant bits of the HL register pair to zero to maintain relative addressing within the 16K range of the 27513; if the 27513’s base address is other than 0000H, bits 6 and/or 7 must be set to “1” as required.

5) Jump to the relative location on the page (HL register).

The Page Changing routine is called by:

```
GETSUB    LXI       H,routine       ;"HL" gets routine's address as
                                    ;determined by the assembler.
          CALL      PAGECALL        ;Call the paging routine.
```

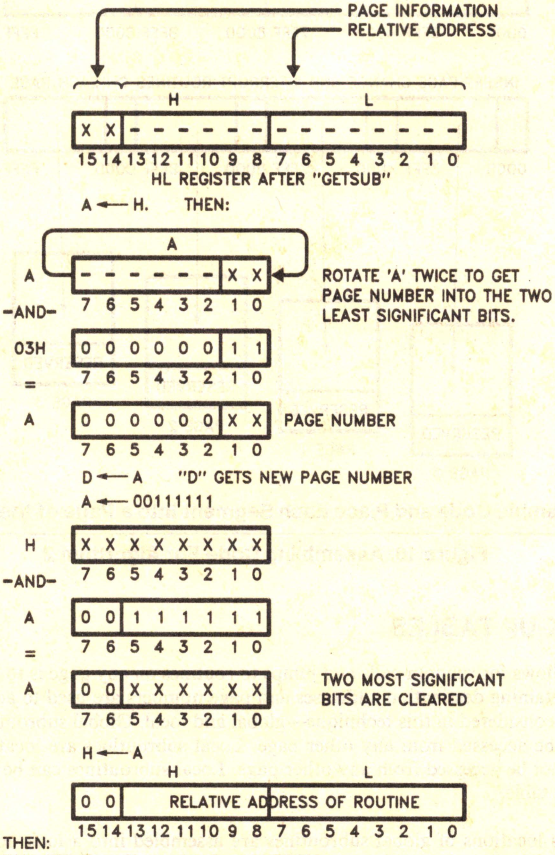
To return to the Calling routine:

```
          JMP       RETURN
```

Jumps to destinations on any page are accomplished by:

```
        LXI         H,destin              ;"HL" gets address of routine as
                                          ;determined by the assembler.
        JMP         PAGETURN
```

Figure 9 shows the "bit stripping" sequence for calling a routine using Algorithm 2.

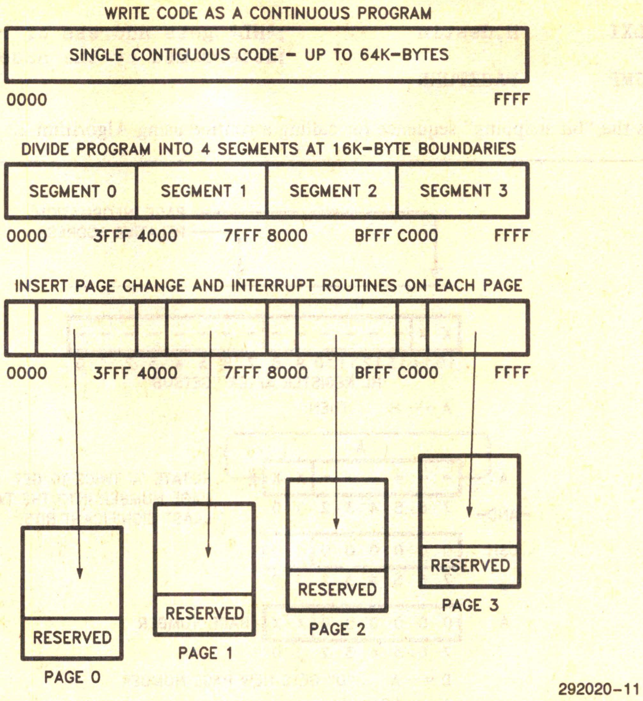

PAGE INFORMATION
RELATIVE ADDRESS
H
L
X X - - - - - - - - - - - - - -
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
HL REGISTER AFTER "GETSUB"
A ← H. THEN:
A
A
- - - - - - X X
7 6 5 4 3 2 1 0
ROTATE 'A' TWICE TO GET PAGE NUMBER INTO THE TWO LEAST SIGNIFICANT BITS.
-AND-
03H
0 0 0 0 0 0 1 1
7 6 5 4 3 2 1 0
=
A
0 0 0 0 0 0 X X
7 6 5 4 3 2 1 0
PAGE NUMBER
D ← A "D" GETS NEW PAGE NUMBER
A ← 00111111
H
X X X X X X X X
7 6 5 4 3 2 1 0
-AND-
A
0 0 1 1 1 1 1 1
7 6 5 4 3 2 1 0
=
A
0 0 X X X X X X
7 6 5 4 3 2 1 0
TWO MOST SIGNIFICANT BITS ARE CLEARED
H ← A
H
L
0 0 RELATIVE ADDRESS OF ROUTINE
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
292020-12

THEN:
Write "D" (Page Number) to Paged EPROM
AND:
JUMP to routine (HL Register)

Figure 9. Changing Pages With Algorithm 2

Assembling the Program

Algorithm 2 allows code to be written using standard programming techniques. 64K of sequential code and subroutines can be written without the need to discern page and relative address information when calls and jumps occur. A section should be reserved at identical locations on each page for reset, interrupt, and page change routines (see Figure 10). Calls and jumps do not address destinations directly. Destinations (derived from subroutine label names as determined by the assembler) are loaded into the "HL" register, and the universal PAGECALL/PAGETURN routine (as described above) is called. The "bit stripping" routine takes care of page selection and relative addressing. RAM locations may be accessed directly. Even though their addresses appear to overlap program memory, no "bit stripping" takes place so RAM actually occupies a unique location.


WRITE CODE AS A CONTINUOUS PROGRAM
SINGLE CONTIGUOUS CODE - UP TO 64K-BYTES
0000
FFFF
DIVIDE PROGRAM INTO 4 SEGMENTS AT 16K-BYTE BOUNDARIES
SEGMENT 0
SEGMENT 1
SEGMENT 2
SEGMENT 3
0000
3FFF
4000
7FFF
8000
BFFF
C000
FFFF
INSERT PAGE CHANGE AND INTERRUPT ROUTINES ON EACH PAGE
0000
3FFF
4000
7FFF
8000
BFFF
C000
FFFF
RESERVED
PAGE 0
RESERVED
PAGE 1
RESERVED
PAGE 2
RESERVED
PAGE 3
292020-11

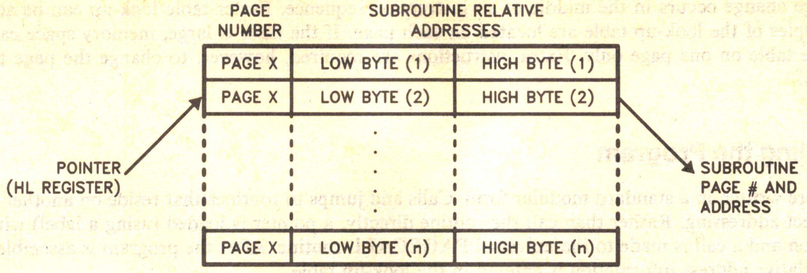
Assemble Code and Place Each Segment Into a Page of the 27513

Figure 10. Assembling Code For Algorithm 2

Algorithm 3: LOOK-UP TABLES

Another technique that allows for random calls and jumps to routines on any page is to use a look-up table. Pointers to locations in a table containing destination addresses and page numbers are used to access subroutines. Two types of subroutines need to be considered in this technique—global and local. Global subroutines are located on any page of the EPROM and can be accessed from any other page. Local subroutines are located on the same page as the calling routines and can not be accessed from any other page. Local subroutines can be called directly and need not be accessed via a look-up table.

Page and relative address locations of global subroutines are assembled into a look-up table. Pointers are used to extract the location information from the table when calling these routines. Figure 11 shows the basic concept of the look-up table approach.



292020-13

Figure 11. Locating a Subroutine From a Look-up Table

When a global subroutine is called, a pointer is loaded with the look-up table location that contains the subroutine's address information. A special global call routine uses this pointer to extract the relative address and page of the desired subroutine. This global call routine, which is located at identical locations on all pages, changes the page and jumps to the destination. When returning from the subroutine, the RETURN routine is used to change to the calling routine's page and relative address. To initiate a call to a global subroutine, a pointer is established that addresses the appropriate look-up table location. An 8085 programming example will illustrate this technique.

```
SOURCE     STATEMENT
GETSUB     LXI        H,Subptr               ;"HL" gets table location of
                                             ;destination information.
           CALL       PAGECALL               ;Enter Global Call routine.
```

The global call routine uses the pointer to extract page and address information from the look-up table.

```
PAGECALL   PUSH       D                      ;Save old page number.
PAGETURN   MOV        D,M                    ;"D" gets destination page from table.
           INX        H                      ;"HL" points to destination's Low
                                             ;address byte in table.
           MOV        E,M                    ;"E" gets destination Low byte.
           INX        H                      ;"HL" points to destination High
                                             ;address byte in table.
           MOV        H,M                    ;"H" gets destination High byte.
           MOV        L,E                    ;"L" gets destination Low byte.
           MOV        M,D                    ;Change page.
           PCHL                              ;Jump to routine.

RETURN     POP        D                      ;Retrieve old page number.
           POP        H                      ;Get return address.
           MOV        M,D                    ;Change page.
           PCHL                              ;Return to program.
```

The RETURN routine is part of the global call routine and provides instructions for return to the calling program. The following statement is used to enter the RETURN routine at the end of a subroutine:

```
           JMP        RETURN
```

The look-up table can also be used when jumps are made to global routines. The following statements will accomplish this.

```
           LXI        H,Jmpptr               ;"HL" gets Table location of
                                             ;destination information.
           JMP        PAGETURN               ;Enter global jump routine.
```

The global call routine must reside at identical locations on each page. This keeps programming flow continuous when a page change occurs in the middle of an instruction sequence. Faster table look-up can be accomplished if identical copies of the look-up table are located on each page. If the table is large, memory space can be saved by locating the table on one page only. Extra instructions are required, however, to change the page to the look-up table's page.

Assembling the Program

Programs are written in a standard modular form. Calls and jumps to routines that reside on another page are done using indirect addressing. Rather than call the routine directly, a pointer is loaded (using a label) with the look-up table location and a call is made to the universal PAGECALL routine. After the program is assembled, destination page and relative address information is entered in the look-up table.

HARDWARE AND ALGORITHMS

The following diagram describes the contexts in which the three algorithms will be discussed. The matrix shows headings for software considerations and system configurations and where they are discussed. Also indicated is the preferred algorithm for a particular hardware/software implementation; the most efficient algorithm for the specific application is listed first if more than one algorithm applies.

		SOFTWARE CONSIDERATION			
SYSTEM CONFIGURATION		**Random Paging**	**Interrupts & Reset**	**Paging @ Page End**	**Discrete Overlays**
PAGED	Heading	A1	A2	A3	A4
EPROM	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
ONLY	Page	17	18	19	19
PAGED +	Heading	B1	B2	B3	B4
SMALL	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
EPROM	Page	19	19	19	20
PAGED	Heading	C1	C2	C3	C4
EPROM	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
+ RAM	Paged	20	20	20	20

System Hardware Configurations

Three configurations will be considered for page addressed implementation using an 8085 system to illustrate each. Word-wide systems use similar techniques (see the appendix for 8086 + Paged EPROM). The algorithms established above will be used to implement page turning for each system. These system configurations are:

A) Paged EPROM Only—located at location 0000H.

B) Paged EPROM + small EPROM—small EPROM placed at location 0000H, paged EPROM at a 16K boundary.

C) Paged EPROM + RAM—EPROM at location 0000H, RAM available anywhere in the memory space.

Within each of these three system configurations, four software considerations will be covered:

1) Paging and continuous program execution.
2) Interrupts and reset.
3) Crossing page boundaries.
4) Discrete programs on each page (preset overlays).

A) Paged EPROM Only

1) Paging and Continuous Programming

The paged EPROM must reside at the beginning of memory (or end of memory for systems that boot up at the top).

Page turning algorithms must reside at the same relative location on each page.

For continuous execution, place these statements at the end of each page:

Algorithm 1

```
                LXI                 H,next page starting location
                JMP                 TURNTO_n           ;n = page number.
```

Algorithms 2 or 3

```
                LXI                 H, next page starting location
                JMP                 PAGETURN
```

2) For interrupt and reset routines:

Page zero can contain the normal reset, boot-up and interrupt routines (or vectors) that would normally be placed at the beginning of memory in a 27128 EPROM. Other pages should contain the following statements.

Algorithm 1

```
0000      RESTART    LXI            H,0000H
0003                 JMP            TURNTO_0
```

Algorithms 2 and 3

```
0000      RESTART    LXI            H,0000H
0003                 JMP            PAGETURN
```

For interrupts (algorithms 2 and 3 shown, algorithm 1 is similar; PAGE_n replaces PAGECALL), the following should reside on each page.

```
0024      TRAP       LXI            H, address of Trap routine
0027                 CALL           PAGECALL

002C      RST5.5     LXI            H,RST5.5 interrupt routine
002F                 CALL           PAGECALL


0034      RST6.5     LXI            H,RST6.5 interrupt routine
0037                 CALL           PAGECALL

003C      RST7.5     LXI            H, RST7.5 interrupt routine
003F                 CALL           PAGECALL
```

Interrupt routines vectored to by an interrupt controller should have space reserved at the same locations on each page in a manner similar to the hardware restart routines shown above.

When returning from an interrupt, the normal return statement (RET or RETI) at the end of an interrupt service routine should be replaced by a jump to the RETURN routine.

```
    Interrupt routine
    :
    :
    :
    INTRTRN  JMP                RETURN
```

The 8085 handles interrupts in a simple manner. An interrupt pushes the contents of the program counter onto the stack as it performs an automatic CALL to the interrupt routine. Therefore, returning from an interrupt is exactly the same as returning from a called routine ("Interrupt Enable", IE, may have to be reestablished).

Some processors push not only the program counter but also certain status registers and the accumulator onto the stack (some push all index registers, accumulator, and status registers) when an interrupt occurs. When using these processors, returns from interrupts must use a procedure appropriate to their implementation.

3) Page Boundaries

Care must be taken when page boundaries are encountered. As program execution continues to the next page, restart and interrupt vectoring routines that reside at the beginning of each page should be jumped over. When a program is assembled, a two line procedure should be placed at the end of the page to allow programming to continue to the next page.

```
ENDPAGE   LXI              H,next page starting address.
          JMP              PAGETURN
```

4) Discrete Applications

When discrete application software is to reside on each page, a kernel routine must also be placed at the beginning of each page. This kernel takes care of reset, interrupts, I/O routines, and general boot-up instructions pertinent to the application program it supports. A routine should be placed on each page to handle softkey switching between discrete applications. Page switching algorithm 1 is most appropriate for softkey generated page switching.

B) Paged EPROM + Small EPROM

1) Paging and Continuous Programming

This is an efficient configuration for using a paged EPROM in a system since reset routines, interrupt vectoring routines, bootstrap codes, and page switching routine(s) can all reside in the small EPROM. These routines can be called from any page of the paged EPROM. The small EPROM can act as the kernel (main driver) of the system and the paged EPROM contains the application program (holding either a continuous block of program or discrete applications; one on each page).

Since the base address of the paged EPROM is offset from location 0000H by some distance, Algorithm 2 (for the 27513 only) can be used only if the paged EPROM is placed on a 16K byte boundary. If the 27513 is located at 04000H, for example, boot-up code must set the 27513 to page 1. Page 2 becomes the second page, page 3 the third page, and page 0 the fourth page. Straight-line coding can then be used to program the 27513 if programming begins at location 04000H. If the assembler can not handle five digit program counter locations, program segments that exceed 0FFFFH must be ORGed at 0000H. When assembly is complete, code is placed into the 27513 by initializing it to page 1 and transferring assembled code as follows:

Assembled Addresses	Page	To 27513 Relative Address
04000-07FFF	1	0000-3FFF
08000-0BFFF	2	4000-7FFF
0C000-0FFFF	3	8000-BFFF
00000-03FFF	0	C000-FFFF

Since information contained in the two most significant bits is the important factor for Algorithm 2, the 27513 can be placed at any 16 kilobyte boundary using programming and assembly methods similar to that shown above. During program execution, proper displacement of the 27513 in the address space can be accomplished by setting either or both of the two high order bits of the "HL" register.

For all algorithms, calls and jumps are performed just as they were in the Paged EPROM Only method. The only difference is that the page turning routine resides in the small EPROM rather than on each page of the paged EPROM.

2) Resets and Interrupts

Resets and interrupts require the same considerations as a system using standard memory. Interrupt vectoring routines lie in the small EPROM. If the service routines addressed by these vectors reside within the paged EPROM, code within the small EPROM must take care of changing the paged EPROM to the proper page.

3) Page Boundaries

Crossing page boundaries in a continuous programming mode is accomplished by a two instruction routine:

```
          LXI              H,Starting address on next page
          JMP              PAGETURN
```

Since redundant code need not be placed on each page, programming and assembly is less of a burden on the programmer.

4) Discrete Applications

Discrete applications on each page can be selected by allowing the small EPROM to act as the operating system. Code within the small EPROM decides which page is to be selected by monitoring softkeys or responding to software directives.

C) Paged EPROM + RAM

1) Paging and Continuous Programming

Since almost all systems contain some amount of RAM, a portion of this RAM can be set aside to hold routines that would otherwise require duplication on every page. Since the paged EPROM is the only ROM in this implementation, boot-up code must be located on page zero (as it was for the Paged EPROM Only configuration). Interrupt and reset vectoring routines, which are fixed locations in most processor schemes, would have to reside as they did in a Paged EPROM Only system. The main variant for this Paged EPROM + RAM system is that the page switching routine(s) can reside in a small amount of RAM rather than on every page of the EPROM.

The boot-up code on page zero must transfer the page switching routine to RAM where it can be accessed from any routine, anywhere in memory; even from any page of the EPROM. Some advantage in EPROM space (due to the elimination of redundant coding) and programming ease is gained.

2) Interrupt and Reset

There is no advantage over the Paged EPROM Only configuration as far as reset and hard-wired interrupt routines are concerned. However, an advantage is realized in systems that use interrupt controllers to provide vector addresses. Interrupt service routines can be placed into RAM by (and from) the boot-up code or downloaded from disk. The interrupt controller can point to RAM code for service routines when an interrupt is encountered.

Service routines may be too lengthy to be duplicated from page zero to RAM. In this case, code pointed to by an interrupt controller can contain information that directs program execution to the proper page and the relative location on that page.

3) Crossing Page Boundaries

Page boundaries are crossed in this Paged EPROM + RAM system just as they were in the Paged EPROM Only configuration; i.e. by using the ENDPAGE routine. As noted in the Paged EPROM Only system, reset and interrupt routines residing at the beginning of each page must be jumped over as a page boundary is crossed.

4) Discrete Programs

When discrete applications reside on each page, provisions must be made to allow reset and interrupt routines to occupy their normal positions on each page. To eliminate redundant coding, routines on page zero, such as keyboard service routines, interrupt service routines common to the applications software on all pages, and I/O routines, can be written to RAM space by the boot-up code on page zero. This code can reside on page zero before being transferred to RAM, or it can be loaded into RAM from a system disk.

MULTIPLE PAGED EPROMs

Multiple Paged EPROMs can be used in any system. For example, if two of these devices are used in adjacent memory mapped locations, continuous program execution between them is performed exactly as it would between two 27128 EPROMs. When page changes occur, both EPROMs should have their page numbers updated. This is most likely to occur when discrete applications are contained on each page. For large discrete applications, a simple page change performed on all paged EPROMs will replace one application with an entirely new one.

SUMMARY

Address-constrained systems can now realize a dramatic increase in program memory through the use of paged EPROMs. Code overflow can be accommodated in existing systems by a simple plug-in replacement of a higher density EPROM. For new applications, program memory constraints need never be the cause of system obsolescence. Programs can occupy 64 kilobytes today and be upgraded to as much as 4 megabytes in the future using a single 28-pin site (32-pin PLCC site). Discrete applications can occupy the same address space without having to add decoders, latches, or logic circuitry for bank selection. The on-chip page latch located within the free writable address locations of the EPROM saves board and address space. Paged EPROMs provide the highest integration, smallest footprint solution for applications requiring programmable nonvolatile memory.

APPENDIX A
PAGED EPROM + 8031

The 8031 microcontroller provides two 64K memory blocks; one for program memory and one for data storage. Microcontrollers are generally used in program intensive environments which require large amounts of nonvolatile memory. Systems requiring up to 64K of memory can use EPROMs with linear addressing schemes, such as the 27512. For systems that require more than the 64K linear address space, the paged EPROM can add a new dimension to the 8031's program memory. Up to four of these devices can be used to provide 256 kilobytes (27513) or 512 kilobytes (27011) of executable memory without intruding on the data memory's space.

The 8031's hardware and instruction set facilitate easy read access of the program memory area but do not provide a simple means for writing to that area in order to change pages. The $\overline{\text{WR}}$ output from port 3 of the 8031 could be routed directly to the $\overline{\text{WE}}$ input of a paged EPROM to allow page changes whenever a write instruction addresses a location within a paged EPROM's memory partition. However, if four of these devices are used, filling all of the program memory space, the entire data area will be overlayed by the program memory area for all write instructions. Advantage can be taken of the output ports provided by the 8031 by designating a single bit of port 1, for example, to serve as a selector to allow the $\overline{\text{WR}}$ output of the 8031 to be directed to either data memory or program memory. Figure A1 shows how the inclusion of simple logic gates can provide up to 512K of program memory and a full array of data memory.

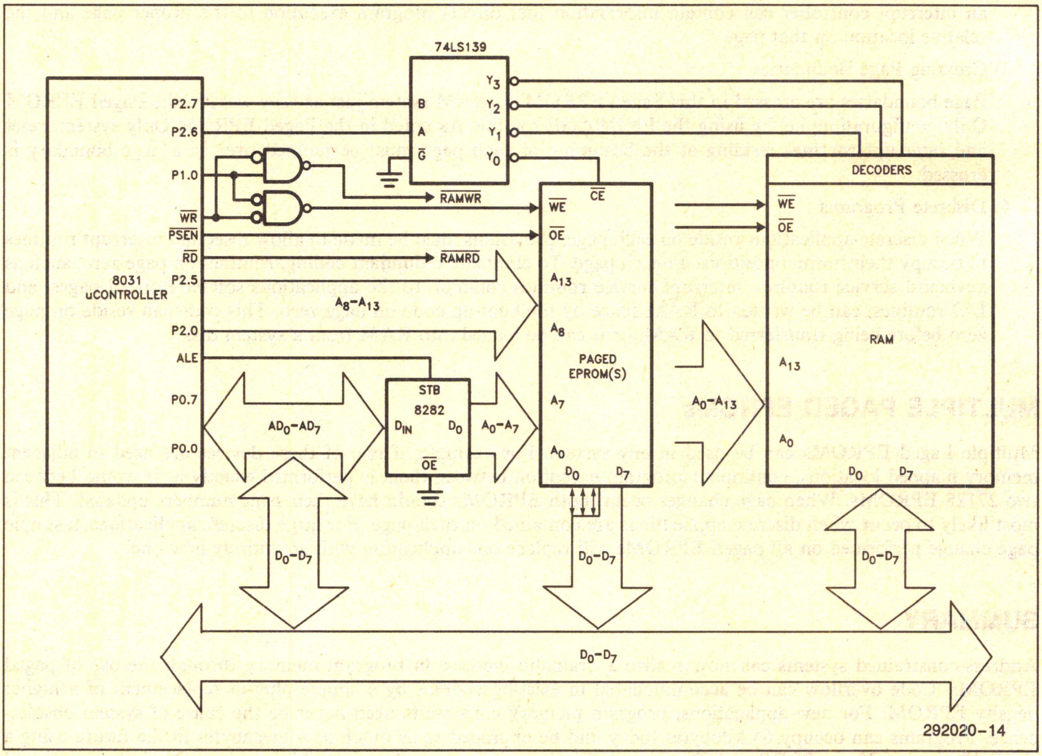

74LS139
Y3
Y2
Y1
Y0
B
A
$\overline{G}$
P2.7
P2.6
P1.0
$\overline{WR}$
$\overline{PSEN}$
$\overline{RD}$
8031
uCONTROLLER
P2.5
P2.0
ALE
P0.7
P0.0
$\overline{RAMWR}$
$\overline{RAMRD}$
$\overline{WE}$
$\overline{OE}$
$\overline{CE}$
A_{13}
A_8
A_7
A_0
PAGED
EPROM(S)
D_0
D_7
A_8–A_{13}
STB
8282
D_{IN}
D_O
$\overline{OE}$
AD_0–AD_7
A_0–A_7
A_0–A_{13}
DECODERS
$\overline{WE}$
$\overline{OE}$
RAM
A_{13}
A_0
D_0
D_7
D_0–D_7
D_0–D_7
D_0–D_7
D_0–D_7
292020–14

Figure A1. 8031 System Configuration

Changing The Pages

Calling or jumping to a subroutine on another page is accomplished by:

```
SOURCE    STATEMENT
GETSUB    MOV         DPTR,#destination ;"DPTR" gets destination address.
          LCALL       Page_n            ;Call the subroutine to turn
                                        ;to page n = 0, 1, 2, ...
```

Following are routines that actually accomplish the page change. "PAGE_n" routines (where n = the page number) are located at identical relative addresses on each page of the EPROM.

```
PAGE_n    PUSH        Present_page      ;Save present page number.
TURNTO_n  MOV         A,#New_page_number;"A" gets destination page number.
          MOV         Present_page,A    ;Update present page.
          MOV         P1.0,0            ;Direct write operations to
                                        ;program memory locations.
          MOV         @DPTR,A           ;Select new page.
          MOV         P1.0,1            ;Direct write operations to
          CLR         A                 ;data memory locations.
          JMP         @A+DPTR           ;Jump to destination.
RETURN    POP         A                 ;Retrieve return page number.
          MOV         Present_page, A   ;Update present page pointer.
          MOV         P1.0,0            ;Direct write operations to
                                        ;program memory locations.
          MOV         @DPTR,A           ;Select page.
          MOV         P1.0,1            ;Direct write operations to
          RET                           ;data memory locations
```

NOTE:
If the accumulator or DPTR registers contain valuable information, provisions should be made to save and retrieve their contents when entering and exiting the "PAGE_n" or "TURNTO_n" routines.

APPENDIX B
PAGED EPROM + Z80

Z80 microprocessor systems easily accommodate the paged EPROM. Address and data bus connections are straight forward, and software page changing routines are very similar to those used by the 8085. Figure B1 shows the hardware block diagram for a Z80/Paged EPROM system. Although the $\overline{\text{MREQ}}$ output of the Z80 need not be used in conjunction with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals, maximum system flexibility is achieved by using $\overline{\text{MREQ}}$ and $\overline{\text{IORQ}}$ to select between Program/Data memory and I/O locations.

Z80 instructions at identical locations on each page call routines on other pages.

Algorithm 1: Manual Paging

```
SOURCE    STATEMENT
PAGE_n    PUSH     DE               ;Save old page (n = page number).
TURNTO_n  LD       D,#Newpage       ;"D" gets new page number.
          LD       (HL),D           ;Change the page.
          JP       (HL)             ;Go to destination.
RETURN    POP      DE               ;Retrieve old page.
          POP      HL               ;Get return address.
          LD       (HL),D           ;Change the page.
          JP       (HL)             ;Return to calling routine.
```

Calling a routine on another page and returning afterward are accomplished by:

```
GETSUB    LD       HL,#destination
          CALL     PAGE_n
```

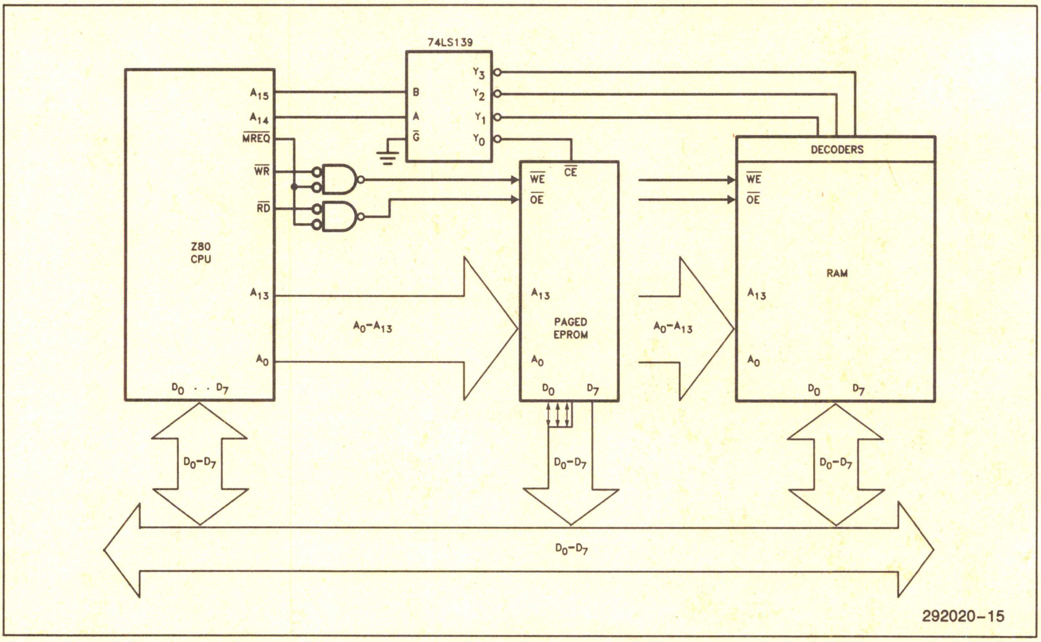

74LS139
B
A
G
Y3
Y2
Y1
Y0
A15
A14
MREQ
WR
RD
Z80 CPU
A13
A0
D0 . . D7
A0–A13
WE
OE
CE
PAGED EPROM
A13
A0
D0
D7
DECODERS
WE
OE
RAM
A0–A13
D0–D7
D0–D7
D0–D7
D0–D7
292020–15

Figure B1. Z80 System Configuration

```
          JP        RETURN
```

The following two statements allow jumps to destinations on other pages.

```
          LD        HL,#destination
          JP        TURNTO_n
```

Algorithm 2: Automatic Paging. Contiguous-code programs can use automatic paging in 27513/Z80 systems. Routines at identical locations on each page access routines on other pages.

```
PAGECALL  PUSH      DE                   ;Save old page # (D register).
PAGETURN  LD        D,H                  ;"D" gets high address byte.
          RLC       D                    ;Rotate to get page # from
          RLC       D                    ;two most significant bits.
          RES       6,H                  ;Clear bits 6 and 7 of the
          RES       7,H                  ;"H" register for relative address.
          LD        (HL),D               ;Change the page.
          JP        (HL)                 ;Jump to new location.
RETURN    POP       DE                   ;Retrieve old page number.
          POP       HL                   ;Get return address.
          LD        (HL),D               ;Change to old page.
          JP        (HL)                 ;Return to program.
```

The page changing routine is called and a return is accomplished by:

```
GETSUB    LD        HL,#destination
          CALL      PAGECALL

          JP        RETURN
```

Jumps to destinations are accomplished by:

```
          LD        HL,#destination
          JP        PAGETURN
```

Algorithm 3: Look-up Table. This approach is easily implemented in Z80 code. To call a subroutine on another page, a pointer to the look-up table is loaded into the "IX" register. A PAGECALL routine at identical locations on each page extracts the subroutine location from the table.

```
PAGECALL  PUSH      DE                   ;Save old page number.
PAGETURN  LD        D,(IX+0)             ;"D" gets new page number from table.
          LD        L,(IX+1)             ;"L" gets destination low byte.
          LD        H,(IX+2)             ;"H" gets destination high byte.
          LD        (IX+0),D             ;Write "D" to change the page.
          JP        (HL)                 ;Jump to subroutine.
RETURN    POP       DE                   ;Retrieve old page number.
          LD        (IX+0),D             ;Write "D" to change page.
          RET                            ;Return to program.
```

The look-up table routine is called, and a return is accomplished, by:

```
GETSUB    LD        IX,#Subptr           ;"IX" gets pointer to table.
          CALL      PAGECALL

          JP        RETURN
```

Jumps to subroutines on another page are accomplished by:

```
          LD        IX,#Subptr
          JP        PAGETURN
```

APPENDIX C
PAGED EPROM + 6800/6809

The 6800 series of microprocessors differs from Intel's and Zilog's in the way it boots up at power on. The 6800/6809 looks to the end of its address space for a restart vector. At power-up, the program counter is loaded with the two-byte address contained at physical addresses 0FFFEH and 0FFFFH. If the paged EPROM is to be the only ROM in the system, as shown in Figure C1, its base address should be memory mapped at system address 0C000H. This allows the 6800/6809 to find its boot-up vector at the top two bytes of page zero (system addresses 0FFFEH and 0FFFFH; device addresses 3FFEH and 3FFFH). To allow for system RESET, the top two bytes of all other pages should also contain vectors that direct program execution to a routine that changes the EPROM to page zero and begins program execution at the boot-up routine.

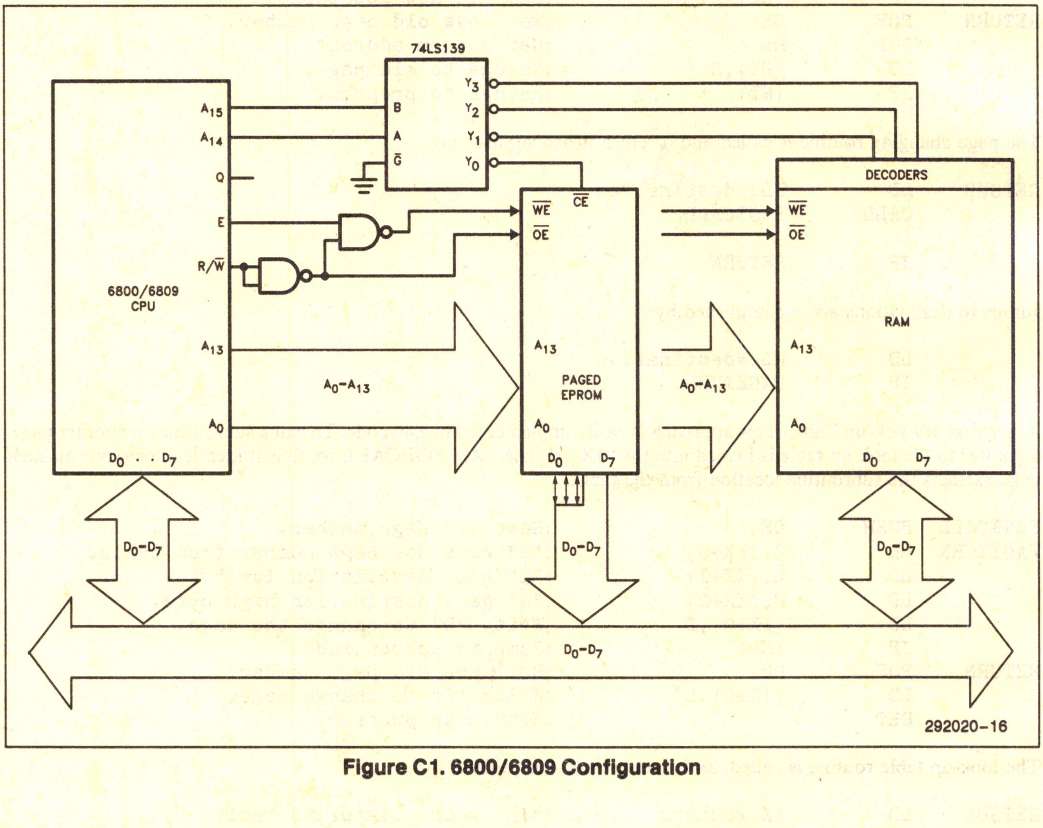

74LS139
B
A
$\overline{G}$
Y_3
Y_2
Y_1
Y_0
A_{15}
A_{14}
Q
E
$R/\overline{W}$
6800/6809
CPU
A_{13}
A_0
D_0 . . D_7
A_0–A_{13}
$\overline{WE}$
$\overline{OE}$
$\overline{CE}$
A_{13}
PAGED
EPROM
A_0
D_0
D_7
A_0–A_{13}
DECODERS
$\overline{WE}$
$\overline{OE}$
RAM
A_{13}
A_0
D_0
D_7
D_0–D_7
D_0–D_7
D_0–D_7
D_0–D_7
292020–16

Figure C1. 6800/6809 Configuration

The 6800/6809 also uses addresses 0FFF0H–0FFFDH to hold vectors that direct program execution to service routines when hardware or software interrupts occur. These addresses must be reserved at the top memory locations for all pages. Locations pointed to by these vectors must either contain service routines or direct the microprocessor to routines on appropriate pages.

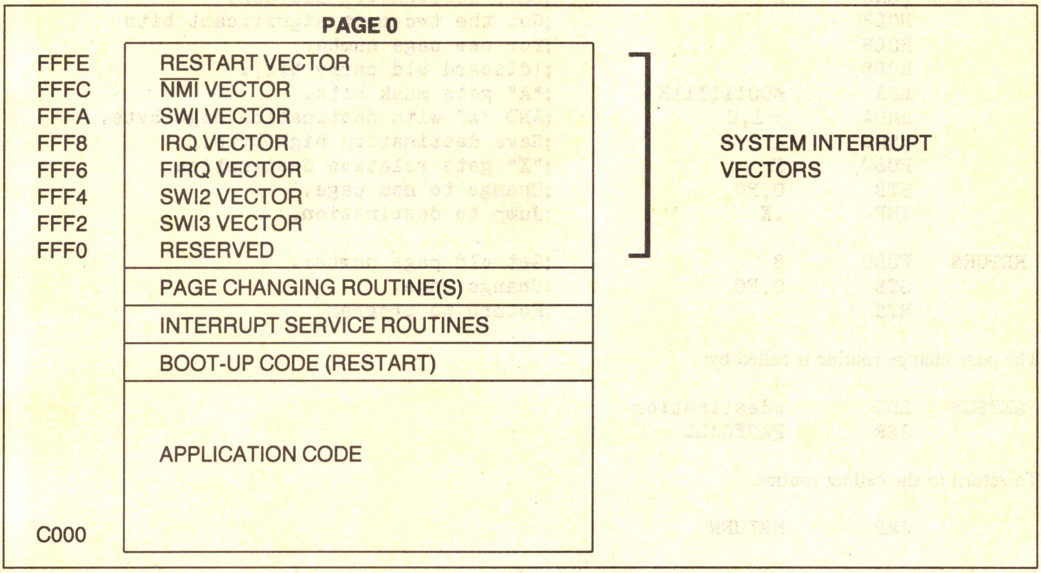

PAGE 0
FFFE
FFFC
FFFA
FFF8
FFF6
FFF4
FFF2
FFF0
C000
RESTART VECTOR
NMI VECTOR
SWI VECTOR
IRQ VECTOR
FIRQ VECTOR
SWI2 VECTOR
SWI3 VECTOR
RESERVED
PAGE CHANGING ROUTINE(S)
INTERRUPT SERVICE ROUTINES
BOOT-UP CODE (RESTART)
APPLICATION CODE
SYSTEM INTERRUPT VECTORS

Figure C2. Page Zero Coding For 6800/6809

Page zero can be coded as shown in Figure C2. Page changing algorithms for the 6800/6809, shown below, are similar to those described in the text for the 8085. The "B" register contains the page number and the "X" register is used as the destination pointer.

Algorithm 1: Manual Paging

```
PAGE_n    PSHU     B          ;Save old page (n = page number).
TURNTO_n  LDB      #n         ;"B" gets new page.
          STB      ,X         ;Change page.
          JMP      ,X         ;Jump to destination.

RETURN    PULU     B          ;Retrieve old page number.
          STB      0,PC       ;Change the page.
          RTS                 ;Return to calling routine.
```

The PAGE_n routine is called by:

```
GETSUB    LDX      #destination
          JSR      PAGE_n
```

To return to the calling routine:

```
          JMP      RETURN
```

Jumps to destinations are accomplished by:

```
          LDX      #destination
          JMP      TURNTO_n
```

Algorithm 2: Automatic Paging (27513 Only). To determine the page and relative address, the following routine can be used in 27513 applications to strip off the two most significant bits.

```
PAGECALL PSHU     B             ;Save old page number.
PAGETURN PSHU     X             ;Save destination address.
         ROLB                   ;Get the two most significant bits
         ROLB                   ;for new page number
         ROLB                   ;(discard old carry bit).
         LDA      #00111111B    ;"A" gets mask bits.
         ANDA     -1,U          ;AND "A" with destination high byte.
         PSHU     A             ;Save destination high byte.
         PULU     X             ;"X" gets relative destination.
         STB      0,PC          ;Change to new page.
         JMP      ,X            ;Jump to destination.

RETURN   PULU     B             ;Get old page number.
         STB      0,PC          ;Change page.
         RTS                    ;Return to program.
```

The page change routine is called by:

```
GETSUB   LDX      #destination
         JSR      PAGECALL
```

To return to the calling routine:

```
         JMP      RETURN
```

Jumps to destinations on another page are accomplished by:

```
         LDX      #destination
         JMP      PAGETURN
```

Algorithm 3: Look-up Table. The indirect indexing capability of the 6809 is particularly useful in the look-up table approach. If identical copies of the table are located on each page, the following routine can be used.

```
PAGECALL PSHU     B             ;Save old page number.
PAGETURN LDB      ,X+           ;"B" gets new page, increment pointer.
         STB      0,PC          ;Change page.
         JSR      [,X]          ;Call routine pointed to by "X".

RETURN   PULU     B             ;"B" gets old page number.
         STB      0,PC          ;Change page.
         RTS                    ;Return to program.
```

The PAGECALL routine is called by:

```
GETSUB   LDX      #destination
         JSR      PAGECALL
```

Return to the calling routine is simply:

```
         RTS
```

A Jump to a destination is accomplished by:

```
         LDX      #destination
         JMP      PAGETURN
```

APPENDIX D
PAGED EPROM + 8086: A 16-BIT APPLICATION

Sixteen-bit systems can also have limitations placed on the size of program memory space. Discrete firmware based applications such as word processing, data base management, and spreadsheet programs don't need to occupy unique locations in the linear address space. Each of these applications can be placed on a separate page of the paged EPROM(s). A simple software or function key command can switch a new application into the "shared" program memory space. Figure D1 is a block diagram of an 8086 + paged EPROM system.

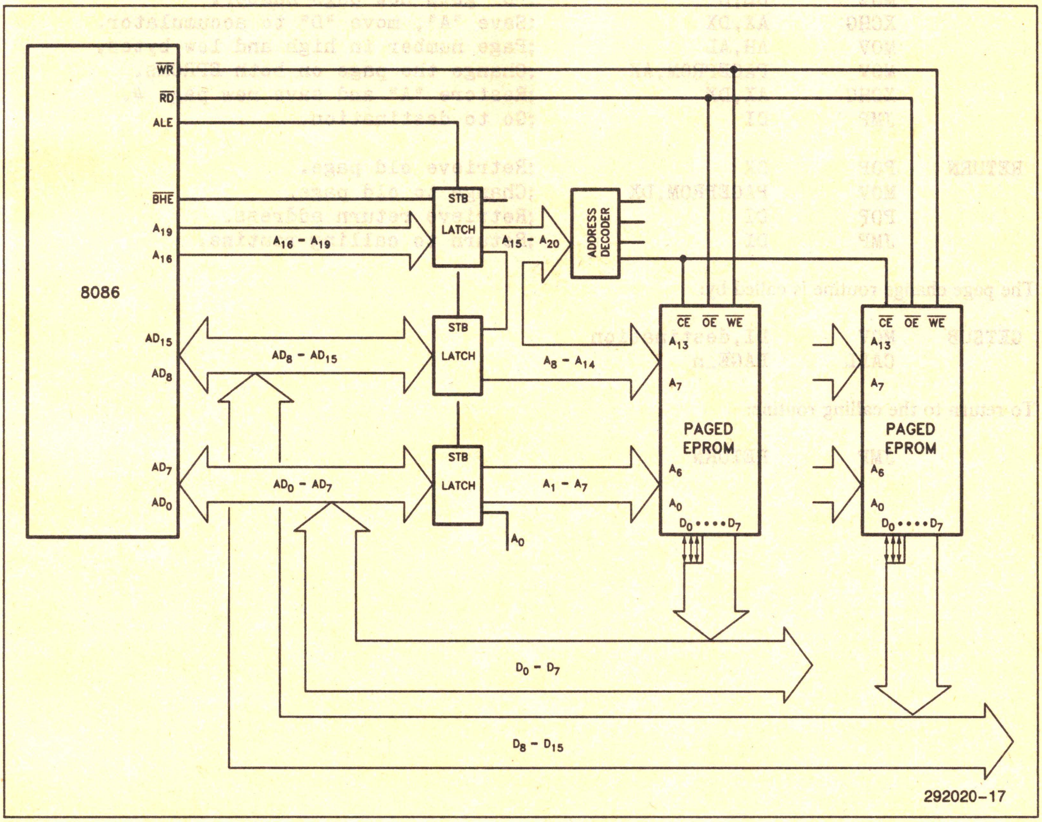

$\overline{WR}$
$\overline{RD}$
ALE
$\overline{BHE}$
A_{19}
A_{16}
8086
AD_{15}
AD_8
AD_7
AD_0
A_{16} - A_{19}
STB
LATCH
A_{15} - A_{20}
ADDRESS DECODER
AD_8 - AD_{15}
STB
LATCH
A_8 - A_{14}
AD_0 - AD_7
STB
LATCH
A_1 - A_7
A_0
$\overline{CE}$ $\overline{OE}$ $\overline{WE}$
A_{13}
A_7
PAGED EPROM
A_6
A_0
D_0 •••• D_7
$\overline{CE}$ $\overline{OE}$ $\overline{WE}$
A_{13}
A_7
PAGED EPROM
A_6
A_0
D_0 •••• D_7
D_0 - D_7
D_8 - D_{15}
292020-17

Figure D1. 8086 Configuration

The word-wide (16-bit) data bus requires two paged EPROMs: one for lower data (D0–D7) and one for upper data (D8–D15). During a program memory fetch, the 8086 reads an entire word at a time. Only one byte of each instruction fetch is used, and the other byte is discarded. For this reason it is possible to omit the A0 and $\overline{BHE}$ (low-byte and high-byte) decode signals. Both EPROMs are enabled and their data is read by the microprocessor.

During page changes, a single write instruction to an even address within the EPROMs address range will change the page simultaneously on both paged EPROMs. To do this, a word-write instruction is performed with the upper and lower bytes of the word containing identical page numbers. A programming segment using algorithm 1 will illustrate how a page change is accomplished.

In the following, the "D" register holds the present page number, and "DI" is the destination address.

```
SOURCE    STATEMENT
PAGE_n    PUSH      DX              ;Save old page (n=page number).
          MOV       DL,n            ;"D" gets new page number.
          XCHG      AX,DX           ;Save "A", move "D" to accumulator.
          MOV       AH,AL           ;Page number in high and low bytes.
          MOV       PAGEPROM,AX     ;Change the page on both EPROMs.
          XCHG      AX,DX           ;Restore "A" and save new page #.
          JMP       DI              ;Go to destination.

RETURN    POP       DX              ;Retrieve old page.
          MOV       PAGEPROM,DX     ;Change to old page.
          POP       DI              ;Retrieve return address.
          JMP       DI              ;Return to calling routine.
```

The page change routine is called by:

```
GETSUB    MOV       DI,destination
          CALL      PAGE_n
```

To return to the calling routine:

```
          JMP       RETURN
```

ENGINEERING REPORT

ER-15

April 1985

The 512K EPROM Family
27512: 512K (64K x 8) EPROM
27513: Page Addressed 512K (4 x 16K x 8) EPROM
The A Stepping

© Intel Corporation, 1985

Order Number: 290009-001

INTRODUCTION

The 512k EPROM family from Intel consists of the 27512, the standard-addressed version with a 64K × 8 organization, and the 27513, a page-addressed version organized as four 16K × 8 pages. Intel's HMOS*II-E process technology, proven on the 64K through 256K densities, is employed on the 512K EPROMs. The 512K EPROMs have a die size of 185 x 317 mils.

GENERAL DESCRIPTION

Both the 27512 and 27513 are compatible with the industry-standard 28-lead EPROM pinout. The 27512 is the logical density upgrade from the 27256 with pin 1 (V_{PP} on the 27256) freed up for the highest order address, A15, via multiplexing the V_{PP} programming supply with $\overline{OE}$, pin 22.

The 27513 was designed to provide the highest level of memory integration for systems with address range constraints. Popular 8-bit microprocessors and 8- and 16-bit microcontrollers have only 16 address lines. One standard 27512 would consume their entire 64 K-byte address range, leaving no room for other types of memory. The 27513 overcomes these limitations by providing on-chip latches for the two highest order address bits. The former A14 pin (pin 27) becomes a $\overline{WE}$, which when brought low latches the information appearing on the D1 and D0 data lines into internal A14 and A15 registers. Externally, only A0 through A13 are required to address random locations within the selected 16 K-byte page, reducing the physical addressing requirement to 16K (see the 27513 data sheet for a more detailed operational description). The result is that the 27513 is pin for pin compatible in read mode with 128K EPROMs like the 27128A. The $\overline{WE}$ control line, required to change 27513 pages, is on the same pin used for $\overline{WE}$ on byte-wide RAMs. Utilizing the Intel Universal Site concept for byte-wide memories allows simple jumpering of the $\overline{WE}$ function into pin 27 for an easy upgrade to the 27513 from a 128K EPROM. Figure 1 shows the 27513 pinout along with those of the entire Intel EPROM family. Note the compatibility between the 27512 and the 27256 and between the 27513 and the 27128A.

The 27512 and 27513 share the same basic die, benefitting mutually from shared processing. Consequently, they are physically and electrically identical with the exception that the two-bit address latch circuitry is only activated in the process of manufacturing the 27513. The significant differences are in programming and testing where the 27513 is addressed and checked out with page-select operations at the 16 K-byte page boundaries. Figures 2 and 3 illustrate circuit layout relationships (the chip plan) and address decoding scheme (bit map), respectively, for both 512K's.

SIMILARITIES WITH OTHER HMOS II-E EPROMs

The 512K EPROMs share several design features with the other members of the HMOS II-E family. Common features include input buffer circuitry, sense amplifier design, and a reference column sensing scheme (refer to ER-11, "HMOS II-E: The Next Generation EPROM Technology"). The internal programming circuitry is also similar with the exception of additional 512K logic required to multiplex the programming supply voltage, V_{PP}, with $\overline{OE}$ (pin 22).

REDUNDANCY

The 512K EPROM family employs redundant memory array elements for yield enhancement, using an approach similar to that which was first introduced on the 27128. The 27128 proved the viability of the use of unerasable EPROM (UPROM) cells as the programmable elements for redundancy implementation. UPROM cells are normal EPROM cells which have a metal covering and polysilicon layout such that the resulting structure is inpenetrable to UV light. Not only do UPROM cells have excellent programming yields for maximum success rates in repairing defective arrays, they also exhibit the same high reliability as the EPROM array cells.

The 512K EPROMs have both spare rows and columns (4 redundant rows and 16 redundant columns) available for repair. This scheme is also incorporated into the 27256 C-stepping. While Intel's first redundant EPROM, the 27128, had only spare rows, the addition of redundant columns was later shown to produce a higher repairable yield than earlier statistical models predicted. The experience acquired in manufacturing the 27128 enables a 512K EPROM testing approach which optimizes yields through proper identification of defect type and appropriate repair algorithm. This experience also enables identification of defects which are not "hard", repairable problems. 512K EPROM arrays containing these other defect types which may later spread further into the array, such as those that are contamination-related, are rejected and not repaired.

---

*HMOS is a patented process of Intel Corporation.

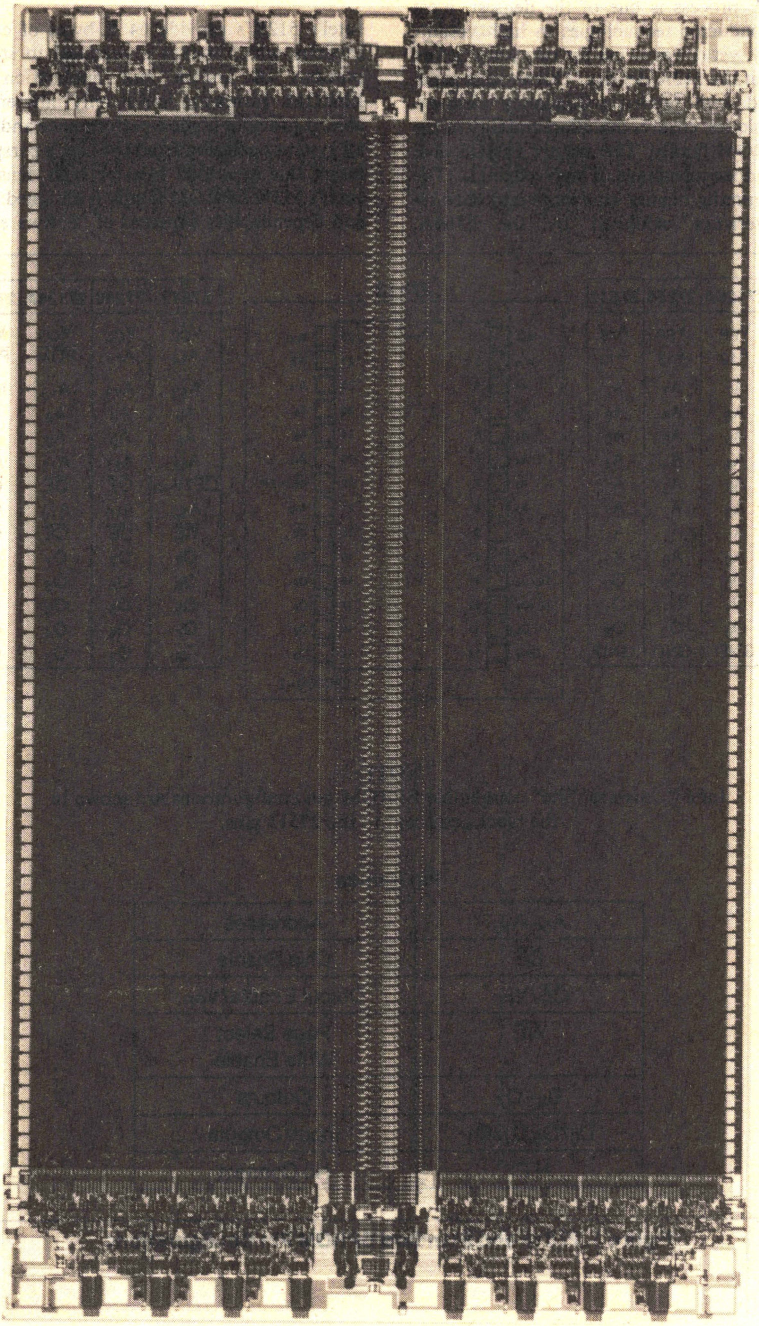


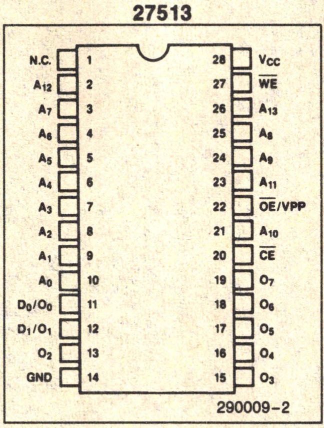
Photo 1. 27512/27513 Die Photograph

SUMMARY

The HMOS II-E process is one of the densest, most advanced semiconductor technologies in high volume production today, yet it was in use for two years before being employed at the 512K density. This process experience, combined with proven redundancy yield-enhancement techniques, ensures manufacturability of the Intel 512K EPROM family. The mature HMOS II-E process has the added advantage of high reliability. The excellent programming quality and long-term data retention characteristics exhibited by the 2764A, 27128A, and 27256 are also found in the 27512 and 27513 since the EPROM array cells are identical.

Intel's 512K's provide 64 K-bytes of code storage, a capacity which makes it practical to store significant portions of system and application software in EPROM. Firmware is not only inherently more reliable, it provides highest performance and simplest overall system operation from the user's perspective. Facilitating this expanded role for high density EPROMs, Intel's 512K EPROM family is designed for availability and dependability expected of "Software Carriers".

2732A	2764A	27128A	27256	27512
	V_{PP}	V_{PP}	V_{PP}	A_{15}
	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



27512	27256	27128A	2764A	2732A
V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$	
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page Select Write Enable
O_2–O_7	Outputs
$D_0/O_0, D_1/O_1$	Input/Outputs
N.C.	No Connect

Figure 1. 27513 and Standard EPROM Pin Configurations

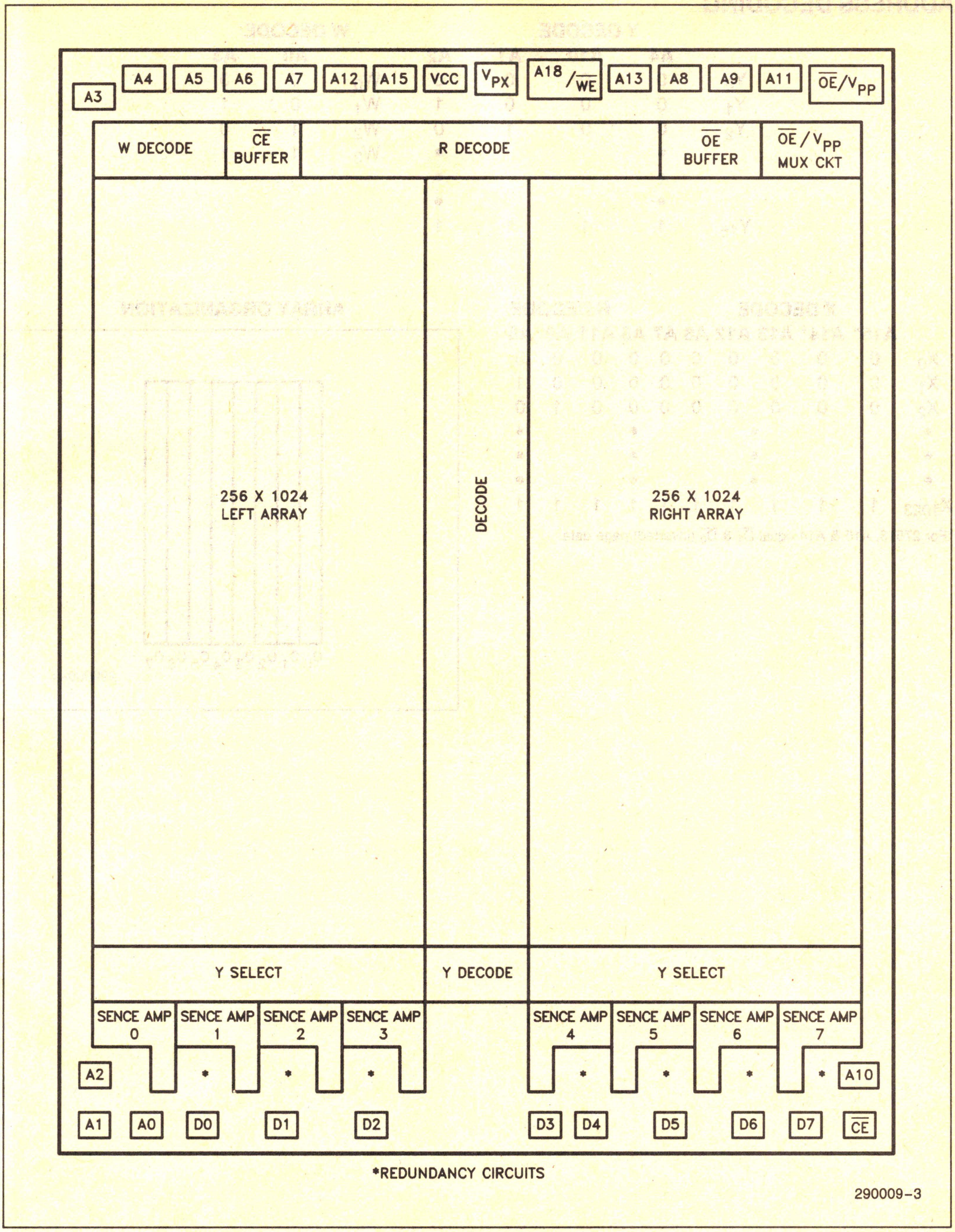

A3
A4
A5
A6
A7
A12
A15
VCC
V_{PX}
A18/$\overline{WE}$
A13
A8
A9
A11
$\overline{OE}/V_{PP}$
W DECODE
$\overline{CE}$ BUFFER
R DECODE
$\overline{OE}$ BUFFER
$\overline{OE}/V_{PP}$ MUX CKT
256 X 1024 LEFT ARRAY
DECODE
256 X 1024 RIGHT ARRAY
Y SELECT
Y DECODE
Y SELECT
SENCE AMP 0
SENCE AMP 1
SENCE AMP 2
SENCE AMP 3
SENCE AMP 4
SENCE AMP 5
SENCE AMP 6
SENCE AMP 7
A2
A10
A1
A0
D0
D1
D2
D3
D4
D5
D6
D7
$\overline{CE}$
*REDUNDANCY CIRCUITS
290009-3

Figure 2. 27512/27513 Chip Plan

ADDRESS DECODING

Y DECODE

	A4	A10	A1	A2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
	•			•
	•			•
	•			•
Y_{15}	1	1	1	1

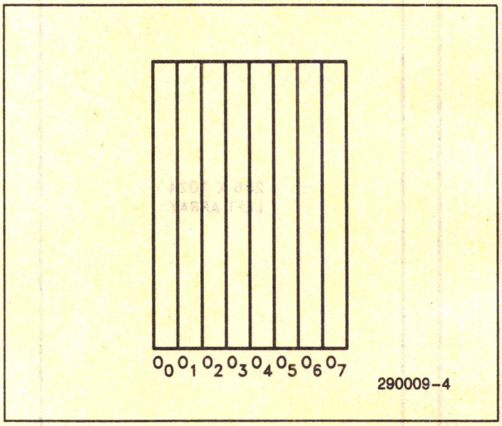
W DECODE

	A0	A3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

	X DECODE							R DECODE		
	A15*	A14*	A13	A12	A8	A7	A6	A11	A9	A5
X_0	0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	0	1	0
•				•			•			•
•				•			•			•
•				•			•			•
X_{1023}	1	1	1	1	1	1	1	1	1	1

*For 27513, A15 & A14 equal $\overline{D_1}$ & $\overline{D_0}$ (inverted) page data

ARRAY ORGANIZATION



BIT MAP

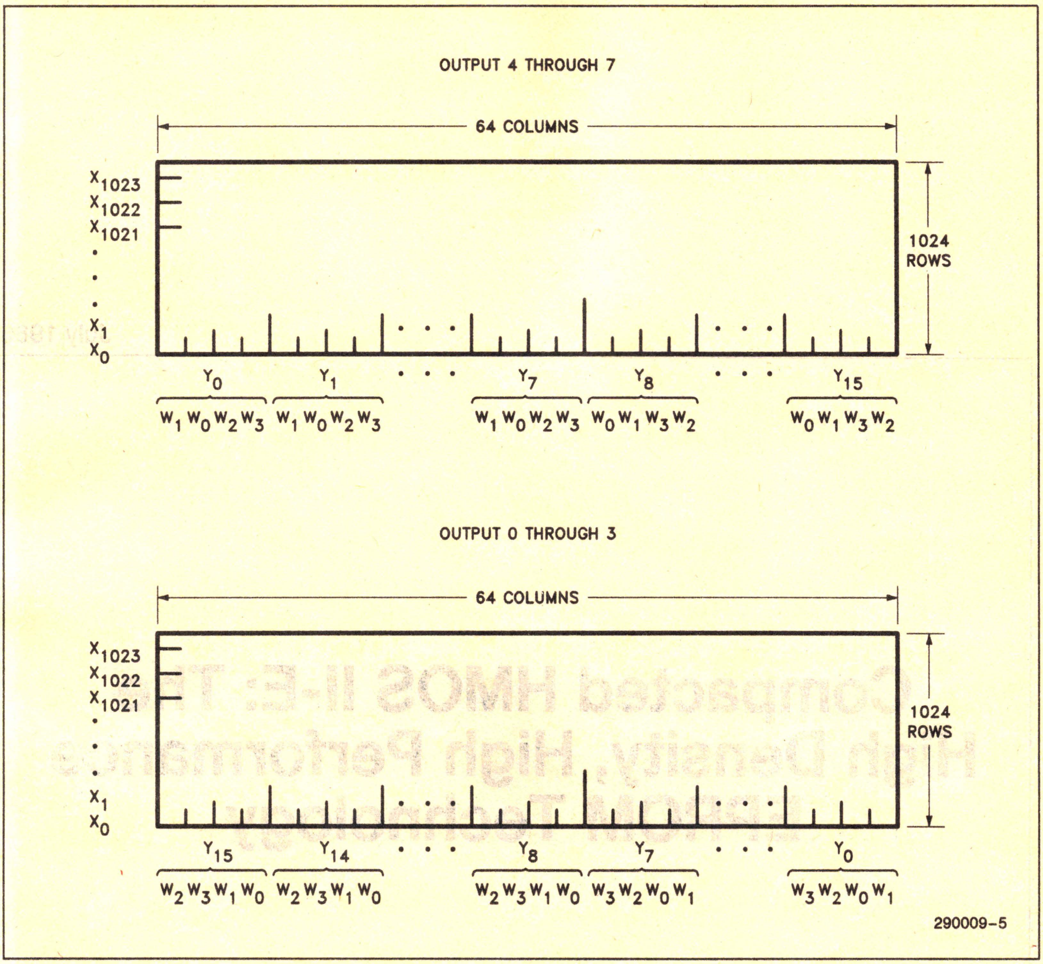

OUTPUT 4 THROUGH 7
64 COLUMNS
1024 ROWS
X1023
X1022
X1021
X1
X0
Y0
Y1
Y7
Y8
Y15
W1 W0 W2 W3
W1 W0 W2 W3
W1 W0 W2 W3
W0 W1 W3 W2
W0 W1 W3 W2
OUTPUT 0 THROUGH 3
64 COLUMNS
1024 ROWS
X1023
X1022
X1021
X1
X0
Y15
Y14
Y8
Y7
Y0
W2 W3 W1 W0
W2 W3 W1 W0
W2 W3 W1 W0
W3 W2 W0 W1
W3 W2 W0 W1
290009-5

Figure 3. 27512/27513 Bit Map

intel®

ENGINEERING
REPORT

ER-16

July 1986

Compacted HMOS II-E: The High Density, High Performance EPROM Technology

© Intel Corporation, 1986

Order Number: 294000-001

INTRODUCTION

This report describes the process, design, and specification changes in the Compacted HMOS* II-E EPROMs. Intel has developed this process to improve the performance and manufacturability of high density EPROMs as part of its continuing commitment to offer the most advanced EPROMs, manufactured to high quality and reliability standards.

Compacted HMOS II-E is a 15% linear shrink of the existing HMOS II-E process. It incorporates Tungsten-Silicide to lower wordline resistance, enhancing device performance. The products which will be based on this new process are: The Megabit Family, 27010, 27011, and the 27210, two new 512K EPROMs, and the 27128B.

New process features of Compacted HMOS II-E include: a.) reduced cell area, b.) addition of Tungsten-Silicide wordlines, c.) reduction of minimum geometry design rules from 1.5μ to 1.2μ. The major benefits that these improvements bring are:

- Immediate availability, and a rapid transition to cost-effectiveness at the megabit density.
- 128K and 512K densities benefit from substantial performance improvements.

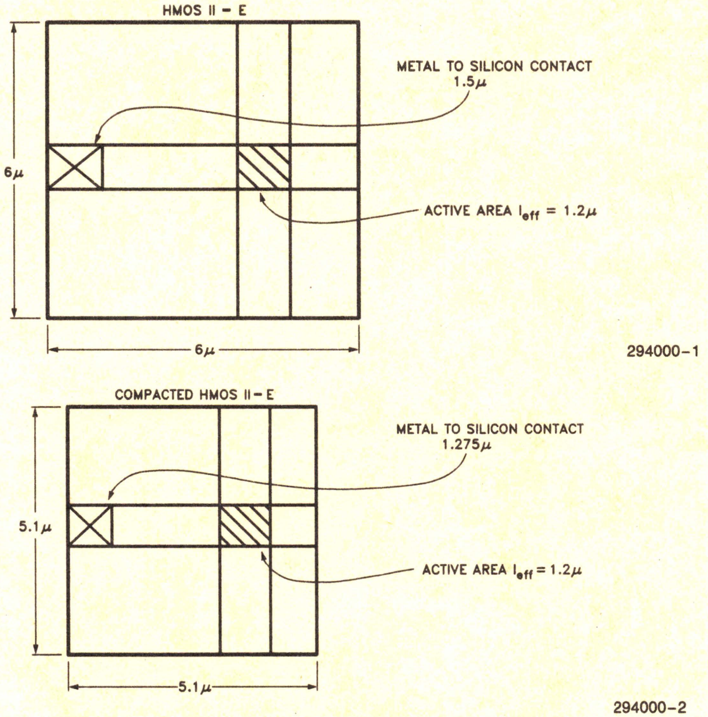
COMPARISON WITH HMOS II-E

Process parameters that are the same as HMOS II-E include: all HMOS II-E EPROM transistor parameters; channel length, depth, and profile, oxide thicknesses, and EPROM programming voltage. The advantages that result from this are:

The same excellent reliability as HMOS II-E.

The same programming algorithms and equipment can be used on Compacted HMOS II-E that were used on HMOS II-E.

Guaranteed availability due to the cumulative learning experience gained on HMOS II-E when applied to Compacted HMOS II-E.


HMOS II - E
METAL TO SILICON CONTACT 1.5μ
ACTIVE AREA l_{eff} = 1.2μ
6μ
6μ
294000-1
COMPACTED HMOS II - E
METAL TO SILICON CONTACT 1.275μ
ACTIVE AREA l_{eff} = 1.2μ
5.1μ
5.1μ
294000-2

EPROM Cell Size Comparision (Drawn to Scale)

---

* HMOS is a patented process of Intel Corporation.

COMPACTION

The compaction of the HMOS II-E process involves a 15% linear shrink of all existing HMOS II-E design features. This is made possible through improvements in photo-resist processing and refinements in wafer stepper lithography techniques. The compaction of the design does not effect the active area of the EPROM transistor, only the spacing between transistors.

TUNGSTEN SILICIDE

Manufacturing Considerations

After the second gate poly-silicon deposition is performed, a layer of Tungsten-Silicide is deposited. This results in reduced wordline resistance optimizing the access time of the device. Tungsten-Silicide is deposited using a CVD (Chemical Vapor Deposition) technique which is an extremely well controlled process. This results in film integrity and excellent step coverage. The characteristics of Tungsten-Silicide film are similar to the poly-silicon film creating a reliable, low-resistance wordline. In fact, the same manufacturing equipment which has yielded over 100 million HMOS II-E devices is employed for this new compacted HMOS II-E process module.

RELIABILITY

Since the HMOS II-E transistor has remained unchanged, the reliability failure rate (FIT's) for devices produced on Compacted HMOS II-E are essentially the same as with HMOS II-E.

Qualification results for Compacted HMOS II-E will be published in the regular updates of the Intel reliability data summary (RR-35).

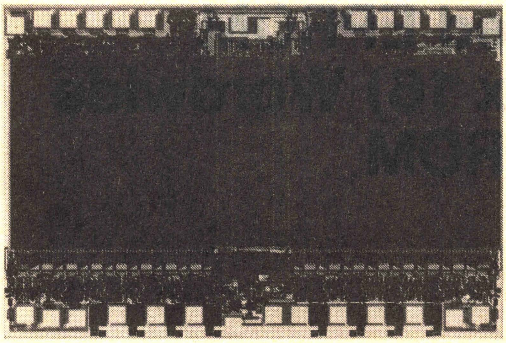
DIE SIZE COMPARISON

27128
205 MIL-SQ

294000-3

HMOS E

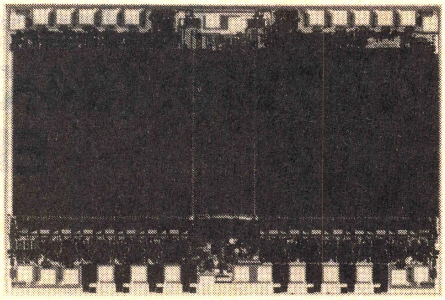
27128A
141 MIL-SQ



294000-4

HMOS IIE

27128B
121 MIL-SQ



294000-5

Compacted HMOS IIE

October 1986

The One-Megabit EPROM Family
27010: (128K x 8) Bytewide EPROM
27011: (8 x 16K x 8) Page-Addressed EPROM
27210: (64K x 16) Wordwide EPROM

© Intel Corporation, 1986

Order Number: 294001-001

INTRODUCTION

The One-Megabit EPROM Family from Intel consists of three products.

1) The 27010 is a standard-addressed version with a 128K x 8 organization. It is housed in a 32 pin DIP package and is upward and downward compatible with other byte-wide EPROM densities. Its die size is 274 x 283 mils.

2) The 27011 is a page-addressed version and is organized as eight 16K x 8 pages. It is fully compatible with the 27513 and is housed in a 28 pin DIP package. Its die size is 274 x 283 mils.

3) The 27210 is a standard-addressed version with a 64K x 16 organization. It is housed in a 40 pin DIP package and is Intel's first word-wide EPROM. Its die size is 282 x 312.

A compacted version of Intel's HMOS II-E process technology, proven on the 64K through 512K densities, is employed on the One-Megabit EPROMs.

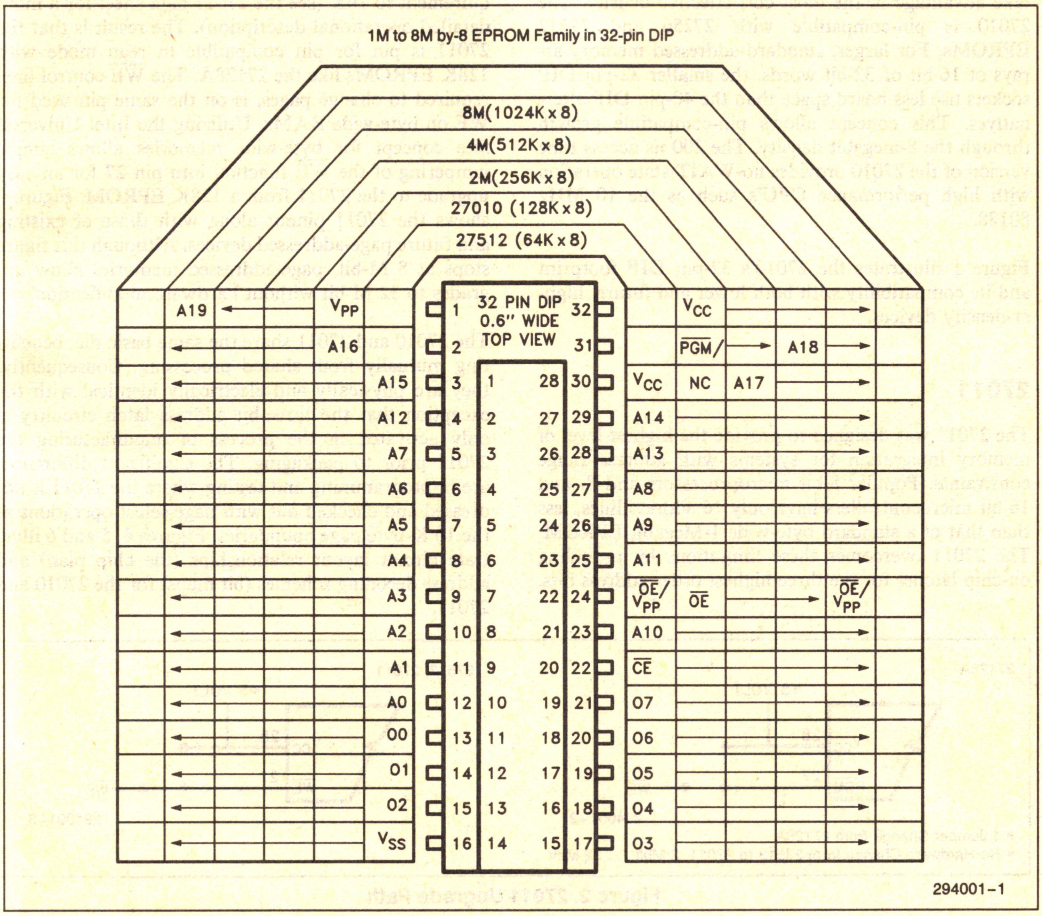

1M to 8M by-8 EPROM Family in 32-pin DIP
8M(1024K x 8)
4M(512K x 8)
2M(256K x 8)
27010 (128K x 8)
27512 (64K x 8)
32 PIN DIP
0.6" WIDE
TOP VIEW
A19
VPP
A16
A15
A12
A7
A6
A5
A4
A3
A2
A1
A0
O0
O1
O2
VSS
VCC
PGM/
A18
NC
A17
A14
A13
A8
A9
A11
OE/VPP
OE
OE/VPP
A10
CE
O7
O6
O5
O4
O3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
294001-1

Figure 1. 27010 Pinout

GENERAL DESCRIPTIONS

27010

The standard-addressed 27010 takes the same step from the 28-pin family as the first 28-pin configuration (the 2764) took from the standard 24-pin site in 1980. It is a logical extension of the mainstream EPROM market today. Its upward and backward compatibility with other densities gives customers the flexibility to accommodate code overruns or to upgrade their systems to take advantage of the most cost-effective density. The 27010 is pin-compatible with 27256 and 27512 EPROMs. For larger, standard-addressed memory arrays of 16-bit or 32-bit words, the smaller 32-pin DIP sockets use less board space than the 40-pin DIP alternatives. This concept allows pin-compatible growth through the 8-megabit density. The 200 ns access time version of the 27010 provides no-WAIT-state operation with high performance CPU's such as the 10 MHz 80188.

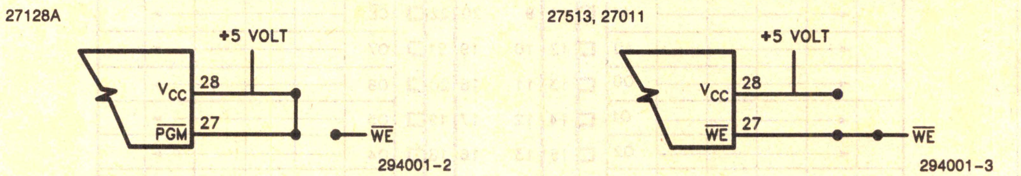
Figure 1 illustrates the 27010's 32-pin DIP footprint and its compatibility with both lower and future, higher-density devices.

27011

The 27011 was designed to provide the highest level of memory integration for systems with address range constraints. Popular 8-bit microprocessors and 8- and 16-bit microcontrollers have only 16 address lines, less than that of a standard byte-wide 1-Megabit EPROM. The 27011 overcomes these limitations by providing on-chip latches for the three highest order address bits. The 27011 is an extension of the page-addressing concept introduced at the 512K density with the 27513. It is the only no-hardware-change upgrade path of all memory architectures; the 27011 drops directly into a 27513 socket with only minor software modifications.

Pin 27 provides a page-write enable ($\overline{\text{WE}}$), which when brought low latches the information appearing on the D2, D1, and D0 data lines into internal A16, A15, and A14 registers. Externally, only A0 through A13 are required to address random locations within the selected 16 K-byte page, reducing the physical addressing requirement to 16K (see the 27011 data sheet for a more detailed operational description). The result is that the 27011 is pin for pin compatible in read mode with 128K EPROMs like the 27128A. The $\overline{\text{WE}}$ control line, required to change pages, is on the same pin used for $\overline{\text{WE}}$ on byte-wide RAMs. Utilizing the Intel Universal Site concept for byte-wide memories allows simple jumpering of the $\overline{\text{WE}}$ function into pin 27 for an easy upgrade to the 27011 from a 128K EPROM. Figure 3 shows the 27011 pinout along with those of existing and future page-addressed devices. Although this figure stops at 8 M-bit, page-addressed memories allow upgrades to 32 M-bit without hardware modification!

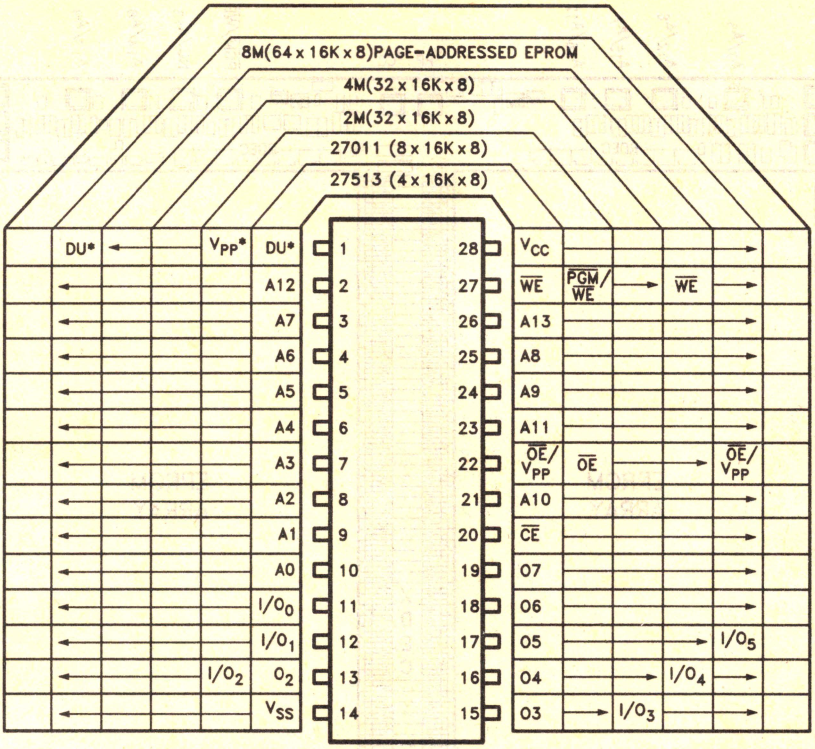
The 27010 and 27011 share the same basic die, benefitting mutually from shared processing. Consequently, they are physically and electrically identical with the exception that the three-bit address latch circuitry is only activated in the process of manufacturing the 27011 prior to packaging. The significant differences are in programming and testing where the 27011 is addressed and checked out with page-select operations at the 16 K-byte page boundaries. Figures 4, 5 and 6 illustrate circuit layout relationships (the chip plan) and address decoding schemes (bit maps) for the 27010 and 27011.



- 1 Jumper Change from 27128A
- No Hardware Change from 27513 to 27011, 2 Mbit . . . 32 Mbit

Figure 2. 27011 Upgrade Path

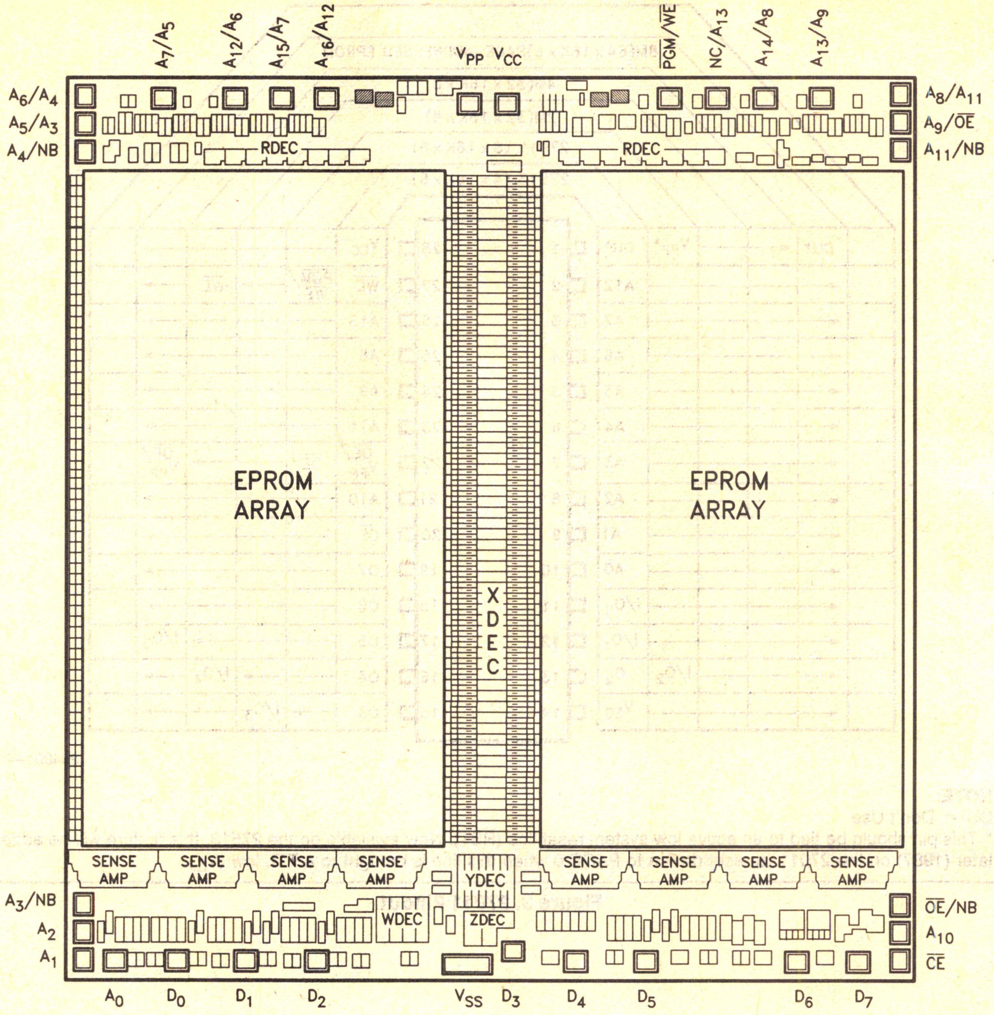
512K to 8M Page-Addressed EPROM Family in 28-pin DIP


8M(64 x 16K x 8)PAGE-ADDRESSED EPROM
4M(32 x 16K x 8)
2M(32 x 16K x 8)
27011 (8 x 16K x 8)
27513 (4 x 16K x 8)
DU*
VPP*
DU*
A12
A7
A6
A5
A4
A3
A2
A1
A0
I/O0
I/O1
I/O2
O2
VSS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
VCC
WE
PGM/WE
WE
A13
A8
A9
A11
OE/VPP
OE
OE/VPP
A10
CE
O7
O6
O5
I/O5
O4
I/O4
O3
I/O3

294001-4

NOTE:
DU = Don't Use
* This pin should be tied to an active low system reset line ($\overline{RST}$). Now available on the 27513, this feature will be added later (1987) on the 27011 to reset device to PAGE 0 when this line is brought to a TTL low (V_{IL}).

Figure 3. 27011 Pinout


A7/A5
A12/A6
A15/A7
A16/A12
VPP
VCC
PGM/WE
NC/A13
A14/A8
A13/A9
A6/A4
A5/A3
A4/NB
A8/A11
A9/OE
A11/NB
RDEC
RDEC
EPROM ARRAY
EPROM ARRAY
XDEC
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
YDEC
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
A3/NB
A2
A1
WDEC
ZDEC
OE/NB
A10
CE
A0
D0
D1
D2
VSS
D3
D4
D5
D6
D7

294001-6

NOTE:
Pin functions are labeled 27010/27011, respectively, when used differently. NB on 27011 are "not bonded" pins.

Figure 4. 27010/27011 Chip Plan

27010 Row Decoding

Row	A_3	A_4	A_{12}	A_{15}	A_{16}	A_{14}	A_{11}	A_{13}	A_9	A_8
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

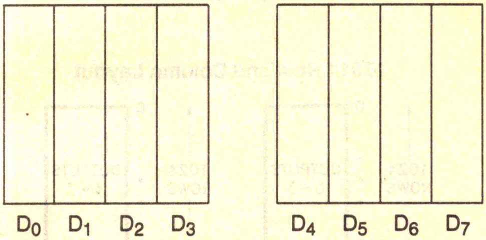
X Decode: A_{16}, A_{15}, A_{14}, A_{12}, A_{11}, A_4 and A_3
R Decode: A_{13}, A_9 and A_8

27010 Column Decoding

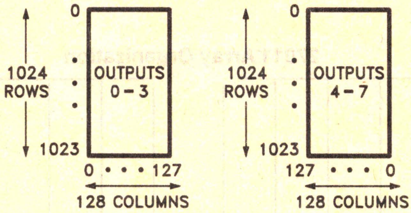
Column	A_2	A_1	A_7	A_6	A_5	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_7, A_6 and A_5
Z Decode: A_{10}

27010 Array Organization


D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7

27010 Row & Column Layout


0
1024 ROWS
1023
OUTPUTS 0 – 3
0 • • • 127
128 COLUMNS
0
1024 ROWS
1023
OUTPUTS 4 – 7
127 • • • 0
128 COLUMNS

294001-7

Figure 5. 27010 Bit Map

27011 Row Decoding

Row	$\overline{D_0}$	$\overline{D_1}$	A_6	A_7	A_{12}	A_8	$\overline{D_2}$	A_9	A_{13}	A_{11}
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

X Decode: D_2, D_1, D_0, A_{12}, A_8, A_7 and A_6
R Decode: A_{13}, A_{11} and A_9

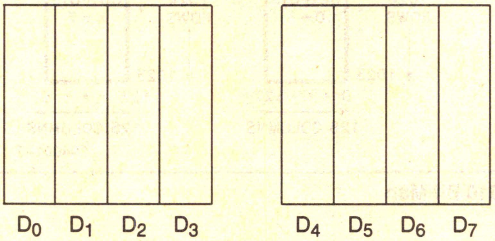
NOTE:
$\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ are complemented page-select write input data.
e.g., $\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ = 000 corresponds to page data 07H.

27011 Column Decoding

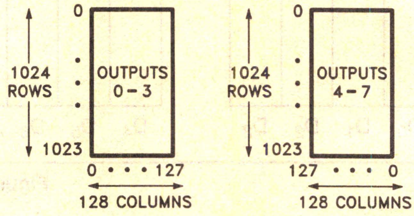
Column	A_2	A_1	A_5	A_4	A_3	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_5, A_4 and A_3
Z Decode: A_{10}

27011 Array Organization


D0
D1
D2
D3
D4
D5
D6
D7

27011 Row and Column Layout


0
1024 ROWS
OUTPUTS 0 – 3
1023
0 • • • 127
128 COLUMNS
0
1024 ROWS
OUTPUTS 4 – 7
1023
127 • • • 0
128 COLUMNS

294001-8

Figure 6. 27011 Bit Map

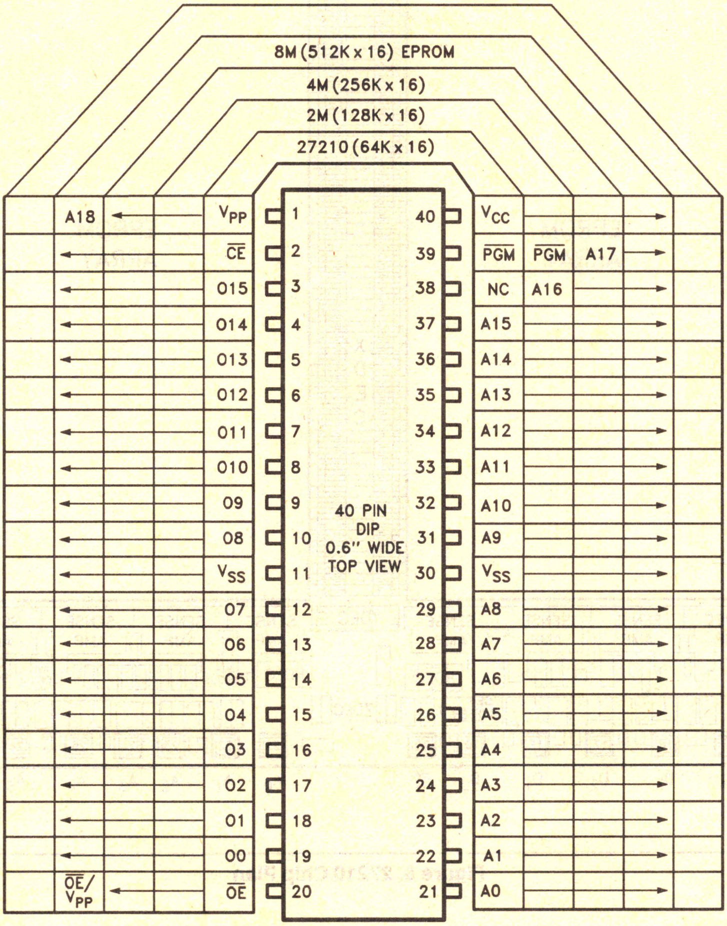
27210

The 27210 is Intel's first word-wide EPROM offering. Intel has broken with the past to offer a simplified pinout, shown in Figure 7, which is well-suited for both 16-bit and 32-bit microprocessor-based systems. All addresses are on one side of the device and data on the other, making this architecture a simple solution that meets the needs of today's advanced microprocessors. This approach preserves performance while simplifying board layout design.

The 27210 also is the fastest 1-Megabit EPROM with speeds up to 150 ns available. This enables no-WAIT-state operation in such high performance CPU's as the 10 MHz 80286.

Figures 8 and 9 illustrate the circuit layout relationships (the chip plan) and the address decoding scheme (the bit map), respectively for the 27210.

1M to 8M by-16 EPROM Family in 40-Pin DIP


8M (512K x 16) EPROM
4M (256K x 16)
2M (128K x 16)
27210 (64K x 16)
A18
V_{PP} 1
$\overline{CE}$ 2
O15 3
O14 4
O13 5
O12 6
O11 7
O10 8
O9 9
O8 10
V_{SS} 11
O7 12
O6 13
O5 14
O4 15
O3 16
O2 17
O1 18
O0 19
$\overline{OE}$ 20
$\overline{OE}$/V_{PP}
40 V_{CC}
39 $\overline{PGM}$ $\overline{PGM}$ A17
38 NC A16
37 A15
36 A14
35 A13
34 A12
33 A11
32 A10
31 A9
30 V_{SS}
29 A8
28 A7
27 A6
26 A5
25 A4
24 A3
23 A2
22 A1
21 A0
40 PIN DIP 0.6" WIDE TOP VIEW

294001-5

VPP on EPROM = VCC in READ Mode

Figure 7. 27210 Pinout

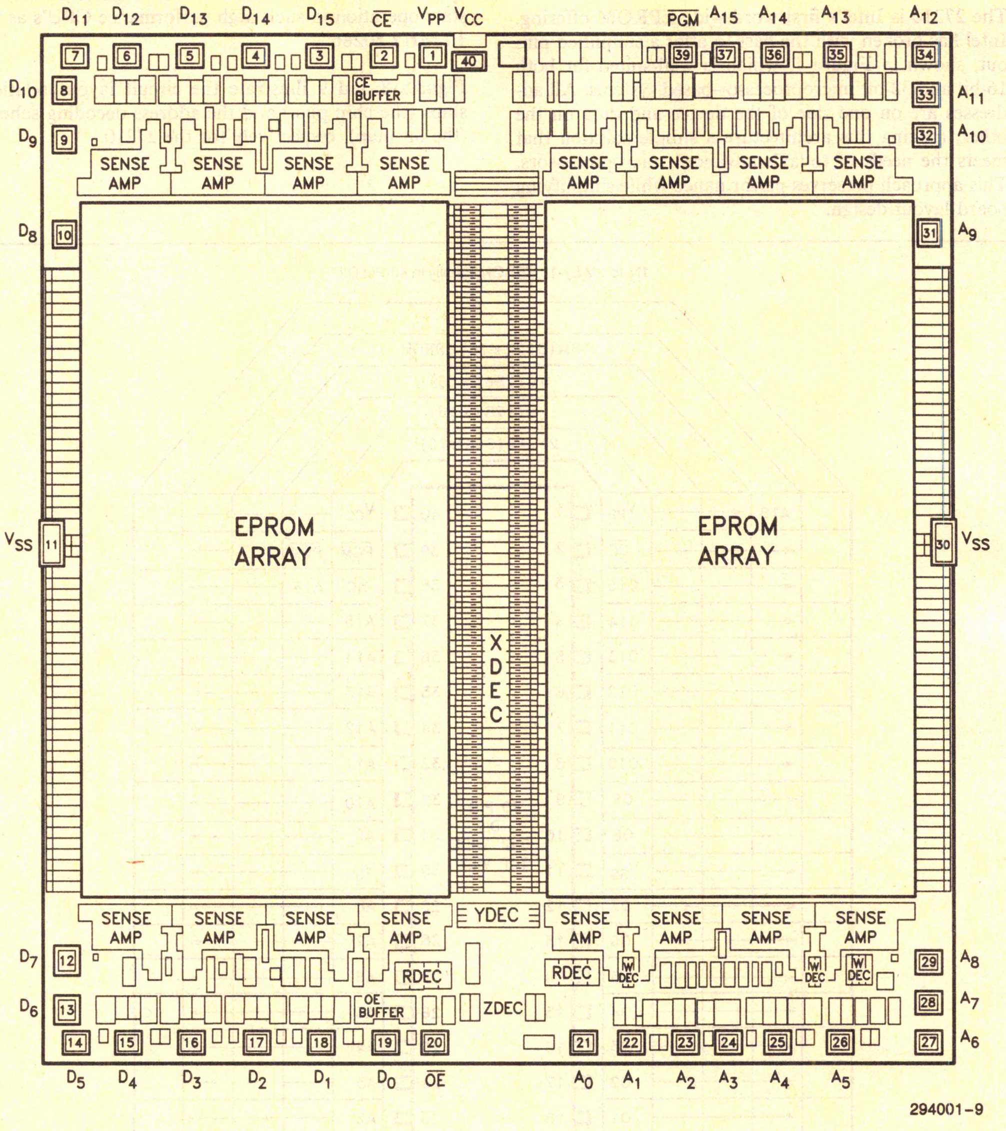

D11
D12
D13
D14
D15
CE
VPP
VCC
PGM
A15
A14
A13
A12
7
6
5
4
3
2
1
40
39
37
36
35
34
CE BUFFER
D10
8
33
A11
D9
9
32
A10
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
D8
10
31
A9
VSS
11
EPROM ARRAY
X DEC
EPROM ARRAY
30
VSS
YDEC
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
SENSE AMP
D7
12
RDEC
RDEC
W DEC
W DEC
W DEC
29
A8
D6
13
OE BUFFER
ZDEC
28
A7
14
15
16
17
18
19
20
21
22
23
24
25
26
27
A6
D5
D4
D3
D2
D1
D0
OE
A0
A1
A2
A3
A4
A5
294001-9

Figure 8. 27210 Chip Plan

27210 Row Decoding

Row	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_{15}	A_{14}	A_{13}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0
•					•				
•					•				
•					•				
511	1	1	1	1	1	1	1	1	1

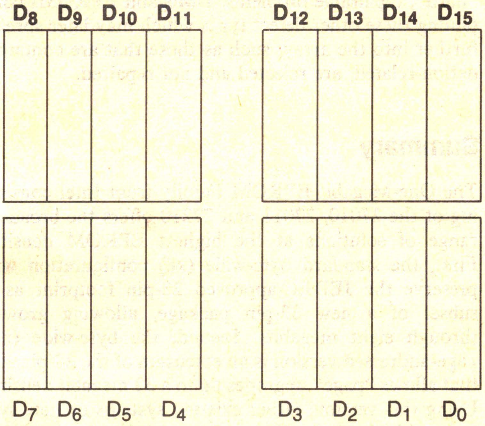
R Decode: A_{15}, A_{14} and A_{13}
X Decode: A_{12}, A_{11}, A_{10}, A_9, A_8 and A_7

27210 Column Decoding

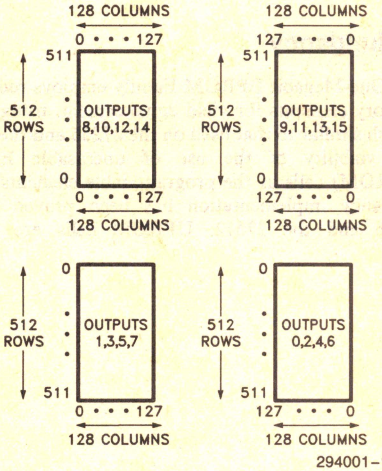
Y Decode	A_3	A_2	A_1	A_0	W Decode	A_6	A_5	A_4
Y_0	0	0	0	0	W_0	0	0	0
Y_1	0	0	0	1	W_1	0	0	1
Y_2	0	0	1	0	W_2	0	1	0
•		•			•		•	
•		•			•		•	
•		•			•		•	
Y_{15}	1	1	1	1	W_7	1	1	1

Column	W	Y	Column	W	Y
0	W_0	> Y_{15}	64	W_4	> Y_{15}
1	W_1		65	W_5	
2	W_1	> Y_{14}	66	W_5	> Y_{14}
3	W_0		67	W_4	
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
30	W_1	> Y_0	94	W_5	> Y_0
31	W_0		95	W_4	
32	W_2	> Y_0	96	W_6	> Y_0
33	W_3		97	W_7	
34	W_3	> Y_1	98	W_7	> Y_1
35	W_2		99	W_6	
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
62	W_3	> Y_{15}	126	W_7	> Y_{15}
63	W_2		127	W_6	

27210 Array Organization


D_8 D_9 D_{10} D_{11}
D_{12} D_{13} D_{14} D_{15}
D_7 D_6 D_5 D_4
D_3 D_2 D_1 D_0

27210 Row & Column Layout


128 COLUMNS
0 • • • 127
511
512 ROWS
OUTPUTS 8,10,12,14
0
0 • • • 127
128 COLUMNS
128 COLUMNS
127 • • • 0
511
512 ROWS
OUTPUTS 9,11,13,15
0
127 • • • 0
128 COLUMNS
0
512 ROWS
OUTPUTS 1,3,5,7
511
0 • • • 127
128 COLUMNS
0
512 ROWS
OUTPUTS 0,2,4,6
511
127 • • • 0
128 COLUMNS

294001-10

Figure 9. 27210 Bit Map

Similarities with Other Intel EPROMs

The One-Megabit Family of EPROMs share several design features with other members of the HMOS II-E family of EPROMs like the 27256 and the 27512. Common features include input buffer circuitry, sense amplifier design and a reference column sensing scheme.

The Compacted HMOS II-E process has reduced the cell dimensions of the 1-Megabit EPROMs to 26 square microns from the 36 square microns used on HMOS II-E. The active region of the EPROM cell for compacted HMOS II-E is the same as for HMOS II-E. However, the inactive cell area has been reduced, resulting in the final cell dimension of 26 square microns. Compacted HMOS II-E also uses advanced photolithography to reduce minimum feature sizes from 1.5 microns to 1.2 microns. The use of existing equipment assures that the manufacturability and reliability of the proven HMOS II-E process will extend to 1-Megabit EPROMs.

New Design Features

Both the 27010 and 27210 have a new feature which allows pre-wiring of higher-order addresses. V_{PP} and $\overline{PGM}$ pins are inactive, that is, in a "don't care" state, as long as V_{PP} is kept at or below the V_{CC} supply voltage. This allows direct wiring of A_{17}/A_{18} and A_{18}/A_{19} (for 27210 and 27010, respectively) to accommodate subsequent 4 M-bit and 8 M-bit devices, eliminating the need for board jumper wires. A_{16}/A_{17} addresses can obviously be routed into the N.C. pins for the 2 M-bit upgrade.

Page-addressed memories, like the 27011, have identical pinouts for upgrades all the way to 32 M-bits without hardware changes.

Redundancy

The One-Megabit EPROM Family employs redundant memory elements for yield enhancement, using an approach similar to that used on the 27256 and the 27512. The viability of the use of unerasable EPROM (UPROM) cells as the programmable elements for redundancy implementation has been proven on the 27256 and the 27512. UPROM cells are normal EPROM cells which have a metal covering and polysilicon layout such that the resulting structure is impenetrable by U.V. light. Not only do UPROM cells have excellent programming yields for maximum success rates in repairing defective arrays, they also exhibit the same high reliability as the EPROM array cells.

The 27010 and 27011 both have 4 redundant rows and 4 redundant columns per output. The 27210 has 4 redundant rows each for the upper and lower bytes and 2 redundant columns per output. The experience acquired in manufacturing the 27256 and the 27512 enables a 1-Megabit EPROM testing approach which optimizes yields through proper identification of defect type and appropriate repair algorithm. This experience also enables identification of defects which are not "hard", repairable problems. 1-Megabit EPROMs containing these other defect types which may later spread further into the array, such as those that are contamination-related, are rejected and not repaired.

Summary

The One-Megabit EPROM Family from Intel consisting of the 27010, 27011 and 27210 offers the broadest range of solutions at the highest EPROM density. First, the standard byte-wide (x8) configuration will preserve the JEDEC-approved 28-pin footprint as a subset of a new 32-pin package, allowing growth through eight megabits. Second, the byte-wide (x8) page-addressed version is an extension of the 28-pin site that allows "page" upgrades up to a 32 megabit density. Using this version, either existing systems or new systems with physical address constraints can be upgraded without hardware changes. Finally, the word-wide (x16) architecture, in a 40-pin package, provides an ideal solution for systems based on today's 16-bit and 32-bit microprocessors.

A compacted version of Intel's HMOS II-E process technology, proven on the 64K through 512K densities, is employed on the 1-Megabit EPROMs. By decreasing the EPROM cell size, manufacturable 1-Megabit EPROMs are feasible and cost-effective. The technological and manufacturing experience we've gained with our HMOS II-E technology on earlier EPROM densities is being applied directly to our One-Megabit Family today.

RELIABILITY REPORT

RR-35D

November 1986

EPROM RELIABILITY DATA SUMMARY

© Intel Corporation, 1986

Order Number: 210473-003

THE IMPORTANCE OF RELIABILITY

Reliability of the non-volatile memories in your end product is critical to your total system reliability. The use of Intel EPROMs can make a difference. Reliability is not just tested, but designed into each component Intel manufactures.

QUALITY ≠ RELIABILITY

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product. While Intel is a quality leader, we also adhere to stringent reliability standards which we have established for ourselves.

Consider Quality vs. Reliability

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end use of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

MONITOR PROGRAM

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is a proven tool that Intel has used for seven years and is now available to its customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. But it's much more than burn-in and device testing. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program. It is the most comprehensive reliability program anywhere.

The paramount objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts—and the performance—that they ordered by specifying Intel. Reliability qualification assures that all new production meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained, day in, day out, over the duration of a device's life. This reliability improves the lifetime reputation of your product, reducing the required number of field service calls.

EPROM RELIABILITY DATA SUMMARY

Intel routinely publishes this "EPROM Reliability Data Summary", a continuing update of reliability information covering Intel's entire EPROM product line. This document includes a discussion on EPROM reliability testing methodology and the most current failure rate calculations, failure analyses and lifetest results.

Intel's commitment to the reliability of our products is clearly reflected in the information we make available to customers. We believe that supplying detailed reliability information to our customers is part of the total solution Intel offers, and is an important part of Intel's leadership in microelectronics technology.

EPROM RELIABILITY TESTING

Intel EPROMs undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and/or during ongoing monitor checks. Where testing differs for plastic packaged production EPROMs, it is so noted.

Intel continually reviews its testing procedures and makes improvements to its methodology whenever overall reliability can be enhanced. Our goal is to be the industry leader in delivering reliable parts and no compromises are accepted.

Information on Intel's reliability testing procedures follows.

High Temperature Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test the memory is sequentially addressed and the outputs are exercised, but not monitored or loaded. A checkerboard data pattern is used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with the failure analysis. In order to best determine long-term failure rate, all devices used for lifetesting are subjected to standard INTEL screening. The 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation. (See Figure 1 for typical burn-in bias and timing diagrams.)

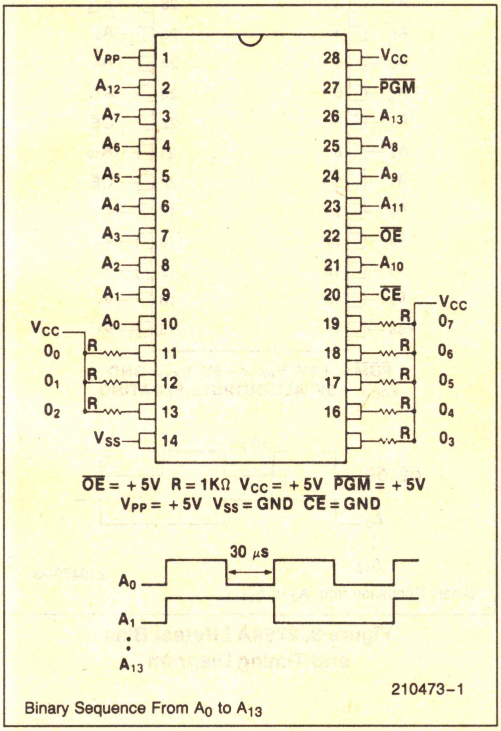

VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
VSS 14
28 VCC
27 PGM
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
O3
VCC
R
OE = +5V R = 1KΩ VCC = +5V PGM = +5V
VPP = +5V VSS = GND CE = GND
30 μs
A0
A1
A13
210473-1
Binary Sequence From A0 to A13

Figure 1. 2764A Burn-In Bias and Timing Diagrams

Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy(1,2,3,4) and the Arrhenius Plot as shown in Figure 2*. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. The failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution to arrive at a confidence level associated failure rate. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Devices submitted to other stresses received a 168 hour lifetest prior to stressing.

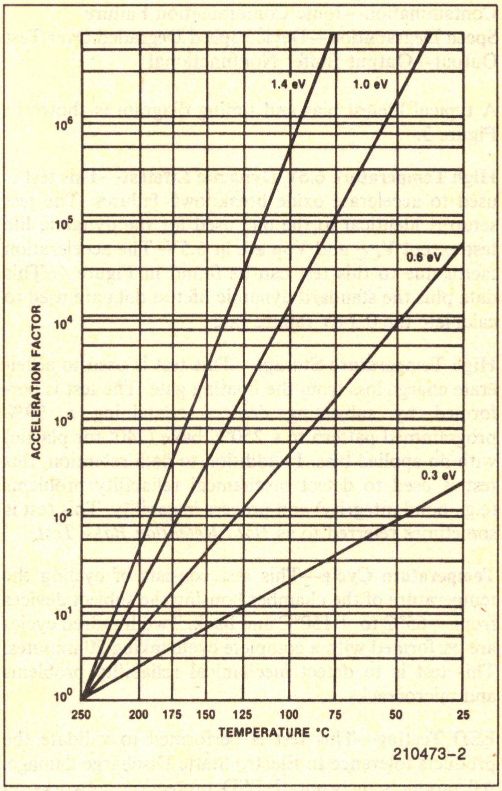


Figure 2. Arrhenius Plot

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Each
Decode/Oxide/Basic Function	0.3
SBCL/SBCG/MBCL/MBCG	0.6
Contamination	1.0
Speed Degradation	0.3–1.0
Output	1.0
Intrinsic Charge Loss	1.4

*The activation energies for various failure mechanisms are listed in Table 1.

Failure Definitions

Decode/Oxide/Basic Function—An Oxide Failure Related Fault
SBCL—Single Bit Charge Loss
SBCG—Single Bit Charge Gain
MBCL—Multiple Bit Charge Loss
MBCG—Multiple Bit Charge Gain
Contamination—Ionic Contamination Failure
Speed Degradation—Device Speed Degraded Over Test
Output—Output Buffer Nonfunctional

A typical lifetest bias and timing diagram is shown in Figure 3.

High Temperature 6.5V Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic life test except V_{CC} and V_{PP} are at 6.5V. The acceleration factor due to this test can be found in Figure 4. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 99% programmed pattern to a 250°C bake (140° for plastic) with no applied bias. In addition to data retention, this test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability. This test is sometimes referred to as *Data Retention Bake Test.*

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. Two hundred cycles are performed with a complete cycle taking 20 minutes. This test is to detect mechanical reliability problems and microcracks.

ESD Testing—This test is performed to validate the products tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks on appropriate pins.

Two types of tests are performed. First, all devices are tested using Mil STD 883 test criteria. In addition, a charged device test is performed to further validate protection occurring during mechanical handling.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is a distinct part of a product qual. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products.

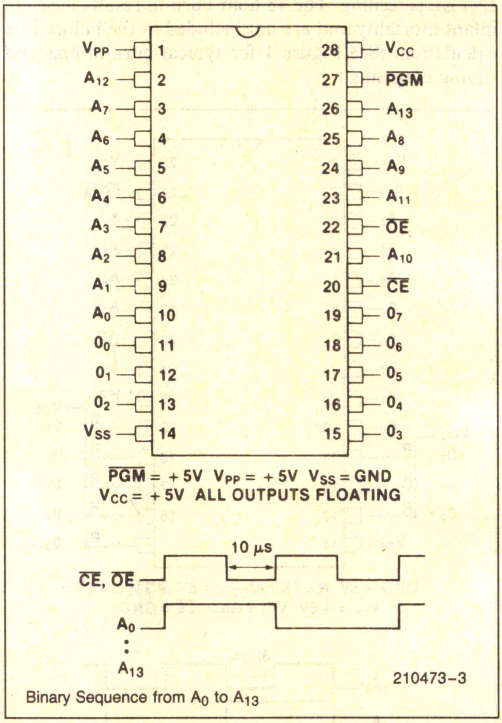


Figure 3. 2764A Lifetest Bias and Timing Diagram

Type	Supply Voltage (Volts)	Oxide Thickness (A)	Operating Stress (MV/CM)	Acceleration Factor at___% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5 x 10^7
HMOS* E	5	700	0.714	3.2	10	320	99,500
HMOS* II E	5	325	1.25	7.5	55	23,700	5.6 x 10^8
CHMOS* II E	5	325	1.25	7.5	55	23,700	5.6 x 10^8

ASSUMES:
1. No Bias Generators
2. Depletion Loads

Figure 4. Time-dependent Oxide Failure Accelerations

*HMOS and CHMOS are patented processes of Intel Corporation.

REFERENCES

1. S. Rosenberg, D. Crook, B. Euzent, "16th Annual Proceedings of the International Reliability Physics Symposium," pp 19–25, 1978.
2. J. Caywood, B. Euzent, B. Shiner, "Data Retention in EPROMs," 1980 IEEE International Reliability Physics Symposium.
3. S. Rosenberg, B. Euzent, "HMOS Reliability" Reliability Report RR-18, INTEL Corporation, 1979.
4. N. Mielke, "New EPROM Data-Loss Mechanisms," 1983. International Reliability Physics Symposium.
5. R.M. Alexander, "Calculating Failure Rates From Stress Data," April 1984 International Reliability Physics Symposium.

NOTE:
The methodology for calculating failure rates is detailed in Appendix A.

CERDIP Reliability Data Summary

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates. Data For CERDIP and plastic EPROMs is treated separately.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler failures occur. These "failures" are not a result of the specific test just completed but are nonetheless removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

2732A/P2732A

The Intel 2732A (CERDIP) is a 32K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P2732A is functionally identical to the 2732A except that it is housed in a windowless plastic package and is one-time programmable.

Number of Bits: 32,768
Organization: 4K x 8
Pin Out: 24 pin, JEDEC Approved Industry Standard
Die Size: 163 x 97 mil.
Process: HMOS-E
Cell Size: 11.5 x 8.75 μM
Programming Voltage: 21.0V
Technology NMOS

2732A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	16/23853	5/21395	1/2125	4/2162	—	—	—
1986	17/12941	15/12928	1/1495	0/1378	0/225	0/225	0/225
Total	23/36794	20/34323	2/3620	4/3540	0/225	0/225	0/225
	A	B	C	D			

2732A (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	12/3030	4/3016	5/1605	—
1986	4/1804	4/1668	—	0/150
Total	16/4834	8/4684	5/1605	0/150
	E	F	G	

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
7.09E + 06	0.3 B.I.	3.68E + 07	2.45E + 07	3		
1.13E + 05	0.3*VAF	5.84E + 06	3.89E + 06	0		
			Total 0.3 eV Failures =	3	0.0098	0.0147
7.09E + 06	0.6 B.I.	1.91E + 08	8.49E + 07	10		
1.33E + 06	0.6 Bake	3.61E + 09	1.43E + 09	28		
1.13E + 05	0.6 HVELT	3.03E + 06	1.35E + 06	0		
			Total 0.6 eV Failures =	38	0.0011	0.0027
7.09E + 06	1.0 B.I.	1.72E + 09	4.44E + 08	14		
1.13E + 05	1.0 HVELT	2.73E + 07	7.04E + 06	0		
			Total 1.0 eV Failures =	14	0.0009	0.0035
				Combined Failure Rate:	0.0118	0.0209
				FITs:	117.63	208.73

48 Hour BI Infant Mortality 0.062%

Theta Ja = 55°C/Watt

V_{CC} = 5.25 Volts

I_{CC} = 80 mA

Delta T = 23.1 C

T(55) = 351.2 K

T(70) = 366.2 K

T(125) = 421.2 K

T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors	
		55°C	70°C
BI/ELT Accel. Factors:	0.3	5.191645	3.459451
	0.6	26.95318	11.96780
	1.0	242.2981	62.61679
250° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	2722.141	1076.682
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 10.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 4 MBCG
3 Speed Degrade
6 SBCL
1 Leakage
3 Basic Function
2 Oxide
4 Contamination

B. 2 Oxide
2 SBCL
1 Speed Degrade
14 Contamination
1 MBCG

C. 2 SBCL

D. 4 SBCL

E. 12 SBCL
3 MBCL
1 MBCL

F. 7 SBCL
1 MBCL

G. 5 SBCL

2764A/P2764A

The Intel 2764A (CERDIP) is a 64K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P2764A is functionally identical to the 2764A except that it is housed in a windowless plastic package and is one-time programmable.

Number of Bits:	65,536
Organization:	8K x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	98 x 117 mils
Process:	HMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	NMOS

2764A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest 168 Hrs	125°C Dynamic Lifetest 500 Hrs	125°C Dynamic Lifetest 1K Hrs
1985	10/24277	1/24255	5/2450	1/2444
1986	6/17874	3/16758	2/1610	1/1607
Total	16/42151	4/41013	7/4060	2/4051
	A	B	C	D

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake 48 Hrs	250°C Data Retention Bake 168 Hrs	250°C Data Retention Bake 500 Hrs	200 Temp Cycles
1985	4/2718	3/2712	0/1424	—
1986	3/1806	0/1930	—	0/250
Total	7/4524	3/4642	0/1424	0/250
	E	F		

2764A (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours 55°C	Equivalent Hours 70°C	# Fail	Fail Rate %/1K Hrs (60% UCL) 55°C	Fail Rate %/1K Hrs (60% UCL) 70°C
8.29E + 06	0.3 B.I.	4.85E + 07	3.13E + 07	4		
0.00E + 00	0.3*VAF	0.00E + 00	0.00E + 00	0		
			Total 0.3 eV Failures =	4	0.0108	0.0167
8.29E + 06	0.6 B.I.	2.83E + 08	1.18E + 08	9		
1.25E + 06	0.6 Bake	3.39E + 09	1.34E + 09	9		
0.00E + 00	0.6 HVELT	0.00E + 00	0.00E + 00	0		
			Total 0.6 eV Failures =	18	0.0005	0.0014
8.29E + 06	1.0 B.I.	2.98E + 09	6.94E + 08	0		
0.00E + 00	1.0 HVELT	0.00E + 00	0.00E + 00	0		
			Total 1.0 eV Failures =	0	0.0000	0.0001
				Combined Failure Rate:	0.0114	0.0182
				FITs:	113.57	181.91

48 Hour BI Infant Mortality 0.038%

Theta Ja = 48°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 40 mA

Delta T = 10.08 C
T(55) = 338.2 K
T(70) = 353.2 K
T(125) = 408.2 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	Thermal Accel. Factors 70°C
BI/ELT Accel. Factors:	0.3	5.841606	3.773111
	0.6	34.12436	14.23636
	1.0	359.0109	83.62421
250° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	2722.141	1076.682
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 Decode Failure
8 Speed Degrade
1 Output
4 SBCG

B. 2 SBCG
1 SBCL
1 MBCG

C. 3 SBCG
3 Speed Degrade
1 SBCL

D. 1 SBCL
1 Speed Degrade

E. 6 SBCL/SBCG
1 Speed Degrade

F. 3 SBCL

27C64/87C64

The Intel 27C64 and 87C64 are low power 64k ultraviolet erasable and Electronically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one as their memory design and manufacturing processes are identical. The 87C64 incorporates an internal address latch, the 27C64 does not.

Number of Bits:	65,536
Organization:	8K x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	141 x 148 mils
Process:	CHMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	3/7651	3/7624	0/805	0/801	—	—	—
1986	0/4245	1/4234	0/460	0/460	0/200	0/199	0/187
Total	3/11896	4/11858	0/1265	0/1261	0/200	0/199	0/187
	A	B					

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	11/866	4/835	—	0/175
1986	1/785	3/783	15/513	1/135
Total	12/1651	7/1618	15/513	1/310
	C	D	E	F

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.47E + 06	0.3 B.I.	1.56E + 07	9.86E + 06	2		
9.56E + 04	0.3*VAF	3.31E + 07	2.10E + 07	0		
			Total 0.3 eV Failures =	2	0.0064	0.0101
2.47E + 06	0.6 B.I.	9.82E + 07	3.93E + 07	0		
2.95E + 05	0.6 Bake	8.03E + 08	3.18E + 08	33		
9.56E + 04	0.6 HVELT	3.79E + 06	1.52E + 06	0		
			Total 0.6 eV Failures =	33	0.0039	0.0098
2.47E + 06	1.0 B.I.	1.14E + 09	2.49E + 08	0		
9.56E + 04	1.0 HVELT	4.41E + 07	9.61E + 06	0		
			Total 1.0 eV Failures =	0	0.0001	0.0004
				Combined Failure Rate:	0.0103	0.0203
				FITs:	103.48	202.57

48 Hour BI Infant Mortality 0.025%

27C64/87C64 (Continued)

Theta Ja = 46°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 10 mA

Delta T = 2.415 C
T(55) = 330.5 K
T(70) = 345.5 K
T(125) = 400.5 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

Thermal Accel. Factors		55°C	70°C
BI/ELT	0.3	6.299620	3.988151
Accel.	0.6	39.68522	15.90535
Factors:	1.0	461.7228	100.5940
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 Oxide Breakdown
1 SBCL
1 MBCG

B. 2 Oxide Breakdown (13)
2 Speed Degrade (13)

C. 10 SBCL
1 MBCL
1 I_{CC} (STBY) Failure

D. 7 SBCL

E. 15 SBCL

F. SBCG (non-package related)

27128A/P27128A

The Intel 27128A (CERDIP) is a 128K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P27128A is functionally identical to the 27128A except that it is housed in a windowless plastic package and is one time programmable. These parts differ from the 27128 in that they require 12.5 Vpp vs. 21.0 Vpp and the process technology is HMOS II-E vs. HMOS-E.

Number of Bits:	131,072
Organization:	16K x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	169 x 117 mils
Process:	HMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	NMOS

27128A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	1/5502	0/336	0/275	0/270	—	—	—
1986	1/4914	0/1031	0/216	0/72	0/100	0/100	0/100
Total	2/10416	0/1367	0/491	0/342	0/100	0/100	0/100
	A						

27128A (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1985	0/389	0/389	0/388	—	—
1986	0/395	1/299	0/293	0/71	0/50
Total	0/784	1/688	0/681	0/71	0/50
		B			

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
4.98E + 05	0.3 B.I.	2.80E + 06	1.83E + 06	0		
5.00E + 04	0.3*VAF	1.55E + 07	1.01E + 07	0		
			Total 0.3 eV Failures =	0	0.0050	0.0077
4.98E + 05	0.6 B.I.	1.57E + 07	6.70E + 06	0		
3.46E + 05	0.6 Bake	9.43E + 08	3.73E + 08	0		
5.00E + 04	0.6 HVELT	1.58E + 06	6.73E + 05	0		
			Total 0.6 eV Failures =	0	0.0001	0.0002
4.98E + 05	1.0 B.I.	1.57E + 08	3.79E + 07	1		
5.00E + 04	1.0 HVELT	1.58E + 07	3.81E + 06	0		
			Total 1.0 eV Failures =	1	0.0012	0.0048
				Combined Failure Rate:	0.0063	0.0128
				FITs:	62.74	127.64

48 Hour BI Infant Mortality 0.019%

Theta Ja = 45°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 60 mA

Delta T = 14.17 C
T(55) = 342.3 K
T(70) = 357.3 K
T(125) = 412.3 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	5.621355	3.667994
Accel.	0.6	31.59964	13.45418
Factors:	1.0	315.8422	76.10777
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 FAB Defect (0.5)
1 MBCL
B. 1 MBCL

27256

Intel 27256 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). A plastic production version, the P27256, will be available in mid 1985.

Number of Bits:	262,144
Organization:	32K x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	180 x 193 mils
Process:	HMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	9/24204	7/23465	4/3497	1/3384	0/100	0/100	—
1986	9/15839	10/15810	0/1650	2/1380	0/239	0/233	1/106
Total	18/40043	17/39275	4/5147	3/4764	0/339	0/333	1/106
	A	B	C	D			E

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1985	16/3125	13/3103	10/1179	—	0/550
1986	32/1805	10/1773	0/129	0/129	1/300
Total	48/4930	23/4876	10/1308	0/129	1/850
	F	G	H		I

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
8.80E + 06	0.3 B.I.	4.66E + 07	3.09E + 07	2		
9.14E + 04	0.3*VAF	2.66E + 07	1.77E + 07	1		
			Total 0.3 eV Failures =	3	0.0057	0.0086
8.80E + 06	0.6 B.I.	2.47E + 08	1.09E + 08	14		
1.26E + 06	0.6 Bake	3.42E + 09	1.35E + 09	81		
9.14E + 04	0.6 HVELT	2.56E + 06	1.13E + 06	0		
			Total 0.6 eV Failures =	95	0.0027	0.0067
8.80E + 06	1.0 B.I.	2.28E + 09	5.79E + 08	8		
9.14E + 04	1.0 HVELT	2.37E + 07	6.01E + 06	0		
			Total 1.0 eV Failures =	8	0.0004	0.0016
				Combined Failure Rate:	0.0088	0.0169
				FITs:	87.85	169.27

48 Hour BI Infant Mortality 0.045%

27256 (Continued)

Theta Ja = 44°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 90 mA

Delta T = 20.79 C
T(55) = 348.9 K
T(70) = 363.9 K
T(125) = 418.9 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors	
		55°C	70°C
BI/ELT	0.3	5.296763	3.510907
Accel.	0.6	28.05570	12.32646
Factors:	1.0	259.0411	65.77555
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 7 Decode
3 Contamination
3 SBCL
1 SBCG
1 Basic Function
3 Speed Degrade

B. 8 SBCL
2 SBCG
1 Speed Degrade
6 Contamination

C. 1SBCG
1 MBCG
1 SBCL
1 MBCL

D. 1 Speed Degrade
1 SBCL
1 SBCG

E. 1 Oxide

F. 44 SBCL
4 MBCL

G. 22 SBCL
1 MBCL

H. 9 SBCL
1 MBCL

I. 1 Lifted Bond

27C256/N27C256

The Intel 27C256 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The N27C256 is functionally identical to the 27C256 except that it is housed in a windowless plastic leaded chip carrier (PLCC) package and is one-time programmable.

Number of Bits:	262,144
Organization:	32K x 8
Pin Out:	28 Pin JEDEC Approved (CERDIP), 32 Pin JEDEC Approved (PLCC)
Die Size:	199 x 216 mils
Process:	CHMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	CMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	0/1059	1/1044	2/400	0/397	0/275	0/272	1/269
1986	2/5724	1/5702	0/690	0/575	0/300	0/300	0/249
Total	2/6783	2/6746	2/1090	0/972	0/575	0/572	1/518
	A	B	C				D

27C256 (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	1/204	1/199	0/195	0/108
1986	0/772	0/771	0/638	0/153
Total	1/976	1/970	0/833	0/261
	E	F		

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
1.66E + 06	0.3 B.I.	1.05E + 07	6.65E + 06	2		
2.68E + 05	0.3*VAF	9.38E + 07	5.92E + 07	0		
			Total 0.3 eV Failures =	2	0.0030	0.0047
1.66E + 06	0.6 B.I.	6.70E + 07	2.67E + 07	1		
4.40E + 05	0.6 Bake	1.20E + 09	4.74E + 08	2		
2.68E + 05	0.6 HVELT	1.08E + 07	4.32E + 06	1		
			Total 0.6 eV Failures =	4	0.0004	0.0010
1.66E + 06	1.0 B.I.	7.89E + 08	1.71E + 08	1		
2.68E + 05	1.0 HVELT	1.28E + 08	2.76E + 07	0		
			Total 1.0 eV Failures =	1	0.0002	0.0010
			Combined Failure Rate:		0.0036	0.0068
			FITs:		36.06	67.68

48 Hour BI Infant Mortality 0.029%

Theta Ja = 36°C/Watt

V_{CC} = 5.25 Volts

I_{CC} = 8 mA

Delta T = 1.512 C

T(55) = 329.6 K

T(70) = 344.6 K

T(125) = 399.6 K

T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors	
		55°C	70°C
BI/ELT	0.3	6.357916	4.015194
Accel.	0.6	40.42309	16.12178
Factors:	1.0	476.1195	102.8857
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 Speed Degrade
1 Oxide Breakdown

B. 1 Contamination (1.0)
1 Decoder Failure

C. 1 SBCG
1 Decoder Failure

D. 1 SBCL

E. 1 SBCG

F. 1 SBCL

27512/27513

The Intel 27512 and 27513 are 512K ultraviolet erasable and Electronically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one since their design and manufacturing processes are identical. The 27512 is organized as a 64K x 8 device while the 27513 contains four separate 16K x 8 pages of memory.

Number of Bits:	524,288
Organization:	64K x 8 (27512), 16K x 8 x 4 pages (27513)
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	185 x 317 mils
Process:	HMOS II-E
Cell Size:	6 x 6 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	2/4074	1/3613	0/460	0/460	—	—	—
1986	8/12725	8/12709	2/1150	0/1032	0/53	0/53	0/53
Total	10/16799	9/16322	2/1610	0/1492	0/53	0/53	0/53
	A	B	C				

Table 2. Additional Qualification Tests

Year	Data Retention Bake		200 Temp Cycles
	48 Hrs	168 Hrs	
1985	2/516	2/512	—
1986	22/1535	8/1505	0/30
Total	24/2051	10/2017	0/30
	D	E	

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
3.24E + 06	0.3 B.I.	1.77E + 07	1.17E + 07	0		
2.65E + 04	0.3*VAF	7.98E + 06	5.25E + 0.6	0		
			Total 0.3 eV Failures =	0	0.0036	0.0054
3.24E + 06	0.6 B.I.	9.72E + 07	4.20E + 07	10		
3.40E + 05	0.6 Bake	9.27E + 08	3.67E + 08	34		
2.65E + 04	0.6 HVELT	7.95E + 05	3.43E + 05	0		
			Total 0.6 eV Failures =	44	0.0045	0.0114
3.24E + 06	1.0 B.I.	9.39E + 08	2.31E + 08	1		
2.65E + 04	1.0 HVELT	7.68E + 06	1.89E + 06	0		
			Total 1.0 eV Failures =	1	0.0002	0.0009
				Combined Failure Rate:	0.0083	0.0176
				FITs:	83.03	176.42

48 Hour BI Infant Mortality 0.059%

27512/27513 (Continued)

Theta Ja = 36°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 90 mA

Delta T = 17.01 C
T(55) = 345.1 K
T(70) = 360.1 K
T(125) = 415.1 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	5.477770	3.598834
Accel.	0.6	30.00596	12.95160
Factors:	1.0	289.7428	71.42870
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 6 SBCL
3 Speed Degrade
1 MBCG

B. 7 SBCL
1 MBCL
1 Contamination

C. 2 SBCL

D. 14 SBCL
10 MBCL

E. 7 SBCL
3 MBCG

27010/27011

(Preliminary)

The Intel 27010 and 27011 are 1Mbit ultraviolet erasable and Electrically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one since their design and manufacturing processes are identical. The 27010 is organized as a 128K x 8 device while the 27011 contains eight separate 16K x 8 pages of memory.

Number of Bits:	1,048,576
Organization:	128K x 8 (27010) 8 x 16K x 8 (27011)
Pin Out:	28 Pin (27011) Pending JEDEC Approval 32 Pin (27010) Pending JEDEC Approval
Die Size:	274 x 283 mils
Process:	HMOS II-E
Cell Size:	5 x 5 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest 168 Hrs	500 Hrs
1986	0/688	0/667	0/300

27010/27011 (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake		200 Temp Cycles
	48 Hrs	168 Hrs	
1986	2/109	2/104	0/35
	A	B	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 2 SBCL
B. 1 SBCL
1 V_{PP} Open

27210
(Preliminary)

The Intel 27210 is a 1Mbit ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). This device features wordwide (x16) outputs.

Number of Bits:	1,048,576
Organization:	64K x 16
Pin Out:	40 Pin JEDEC Approved Industry Standard
Die Size:	282 x 312 Mils
Process:	HMOS II-E
Cell Size:	5x5 μM
Programming Voltage:	12.5V
Techonology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	0/403	0/403	1/196	0/195	0/98	0/98	0/98
			A				

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1986	1/100	1/98	1/97	1/94	1/73
	B	C	D	E	F

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 1 SBCL
B. 1 SBCL
C. 1 SBCL
D. 1 SBCL
E. 1 SBCL
F. 1 Open Contact

Plastic Reliability Data Summary

INTRODUCTION

The following information is written to provide OTP (one time programmable) users with the description and reliability summary of Intel's plastic production EPROMs. It includes brief test descriptions, a description of plastic packaging compounds and the reliability data obtained during the qualification and subsequent product monitors of the P2732A, P2764A, N27C64/N87C64, P27128A, P27256 and N27C256 devices.

PLASTIC PACKAGE CHARACTERISTICS

The EPROM plastic package is composed of flame retardant plastic/epoxy. Intel uses Nitto HC-10, Type 2 epoxy which meets the rating requirements of US94V0 ⅛″ minimum. The die attach incorporates a silver-filled adhesive die attach on a silver spot plated leadframe. Bonding is accomplished through gold thermal compression bonding and lead finish is 60/40 solder dipped tin/lead.

EPROM ELECTRICAL CHARACTERISTICS

OTP EPROMs in plastic are tested to the same electrical/parametric levels as their counterparts in cerdip. The characteristics include input/output voltage levels, speeds, leakage, and power requirement characteristics over the full commercial temperature operating range of 0°C–70°C. Performance capabilities are identical to that of CERDIP EPROMs with speeds to 200 ns currently available.

RELIABILITY/QUALITY STRESSES

High Temperature 125°C Dynamic Lifetest (HTDL)—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and outputs are exercised but not monitored or loaded. A checkerboard data pattern is typically used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with failure analysis. In order to best determine long-term failure rates, all devices used for lifetesting are subjected to a standard Intel screening. The 48-hour burn-in results measure infant mortality and are not included in the failure rate calculations.

High Temperature Extended Lifetest (HTELT)—This test is also performed at 125°C but uses a smaller sample size. The parts are kept in the full active mode for the duration of the test with outputs driven. The test is intended to evaluate the long-term reliability of the product.

High Voltage 6.5V Extended Lifetest (HVELT)—This test is used to accelerate oxide breakdown failures. The test is set up identical to the one used for dynamic lifetest except for V_{CC} and V_{PP} which are raised to 6.5V. The acceleration factor for this configuration on Intel HMOS IIE product has been determined to be 55 and is applicable to the 0.3 eV failure mode components.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 99%+ program pattern to a 140°C bake with no applied bias. In addition to data retention, this test can also be used to detect mechanical reliability problems such as bond integrity or process instabilities. The test is sometimes referred to as a data retention bake test.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is treated as a distinct part of a product qualification. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products. The new Quick-Pulse Programming™ Algorithm has been extensively verified and the data easily surpasses the 99.5% programmability criteria of Intel's qualification requirements. Qualification results are presented in the following table:

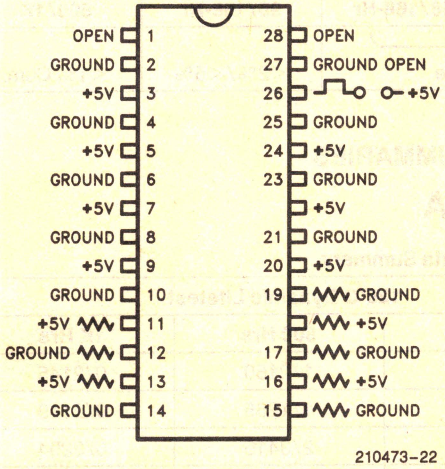
Product	Quality	# Fail	% Yield
P2764A	1800	0	100%
P27128A	1700	0	100%
P27256	8000	2*	99.97%

*Slow to program bits on both failures

MOISTURE RESISTANCE

Two types of moisture resistance testing are performed by Intel. The first is 85°C/85% relative humidity stressing and the second is steam stressing consisting of 121°C, 2 atm.

During the 85°C/85% relative humidity test, the devices are subjected to a high temperature, high humidity environment. The object of the test is to accelerate failure mechanisms through an electrolytic process. This is accomplished through a combination of moisture penetration of the plastic, voltage potentials and contamination which, if present, would combine with the moisture to act as an electrolyte. See Figure 1 for typical 85/85 Bias Diagram.

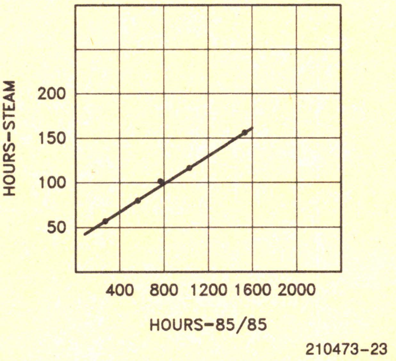


Pin	Pin Name (P2764A)	Stress
1	V_{PP}/N.C.	Open
2	A12/N.C.	Ground
3	A7	+5V
4	A6	Ground
5	A5	+5V
6	A4	Ground
7	A3	+5V
8	A2	Ground
9	A1	+5V
10	A0	Ground
11	O0	+5V
12	O1	Ground
13	O2	+5V
14	Ground	Ground
15	O3	Ground
16	O4	+5V
17	O5	Ground
18	O6	+5V
19	O7	Ground
20	$\overline{CE}$	+5V
21	A10	Ground
22	$\overline{OE}$	+5V
23	A11	Ground
24	A9	+5V
25	A8	Ground
26	N.C./V_{CC}	+5V/Open
27	$\overline{PGM}$/N.C.	Ground
28	V_{CC}/N.C.	Open

Figure 1. Typical 85/85 Bias Diagram

Steam stressing accelerates moisture penetration through the plastic package material to the surface of the die. The objective of this test is to accelerate failures of the device as a result of moisture on the die surface. Corrosion, as typically seen in plastic encapsulated devices, is a very minor contributor to the EPROM failure mechanisms. Through cleanliness in sort, assembly, contamination free plastics, and multi-layer passivation schemes, corrosion has all but been eliminated as a failure mechanism. However, due to the floating gate storage cell composition, EPROMs have a distinctive failure mode which requires special considerations and solutions. The floating gate itself is a highly phosphorous doped structure on which electrons are stored, thus creating the non-volatile memory cell. Passivation defects or marginalities can allow moisture penetration to a single EPROM cell causing oxide deterioration, thus showing up as a charge loss failure. This becomes the predominant failure mode for EPROMs, opposed to corrosion which historically has been the dominant plastic mode of failure. Intel has developed a proprietary, multi-layer passivation which has successfully solved this problem.

Intel has achieved excellent correlation of steam stressing to 85°C/85% RH performance as a result of extensive failure mechanism characterization. We have found, due to this correlation, that steam stressing is an effective and much more time efficient measurement of product moisture reliability.



Steam—85/85 Correlation

QUALITY/RELIABILITY STANDARDS

The table below contains Intel's current requirements for qualification for plastic OTP EPROMs. The failure rate criteria has been established based on a survey of major customers world-wide. Intel consistently meets or exceeds these requirements.

HTDL 48-Hr	HTELT 168/500-Hr	140°C Bake 48/168/500-Hr	HVELT 48/168-Hr	Steam 96/168-Hr	85/85 500/1K
<.05%	<200 FITs Combined Failure Rate			<2%/<5%	<1% Cum.

PRODUCT SPECIFIC RELIABILITY DATA SUMMARIES

P2732A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs
1985	17/14560	1/14393	1/2150	0/2145
1986	6/7366	2/7358	1/1265	0/1149
Total	23/21926	3/21751	2/3415	0/3294
	A	B	C	

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	96 Hrs	
1985	0/2594	0/2594	0/2594	0/2594	3/1649	7/1644	8/1476	0/703
1986	0/1290	0/1290	0/1290	1/1276	2/900	2/896	3/858	0/200
Total	0/3884	0/3884	0/3884	1/3870	5/2549	9/2540	11/2334	0/903
				D	E	F	G	

P2732A (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
5.39E + 06	0.3 B.I.	2.31E + 07	1.62E + 07	1		
0.00E + 00	0.3*VAF	0.00E + 00	0.00E + 00	0		
			Total 0.3 eV Failures =	1	0.0087	0.0125
5.39E + 06	0.6 B.I.	9.92E + 07	4.87E + 07	3		
1.94E + 06	0.6 Bake	1.53E + 08	6.04E + 07	1		
0.00E + 00	0.6 HVELT	0.00E + 00	0.00E + 00	0		
			Total 0.6 eV Failures =	4	0.0021	0.0048
5.39E + 06	1.0 B.I.	6.91E + 08	2.11E + 08	1		
0.00E + 00	1.0 HVELT	0.00E + 00	0.00E + 00	0		
			Total 1.0 eV Failures =	1	0.0003	0.0010
				Combined Failure Rate:	0.0111	0.0182
				FITs:	111.03	182.20

48 Hour BI Infant Mortality 0.10%

Theta Ja = 113° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 80 mA

Delta T = 47.46 C
T(55) = 375.6 K
T(70) = 390.6 K
T(125) = 445.6 K
T(140) = 413.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors	
		55°C	70°C
BI/ELT	0.3	4.288910	3.004446
Accel.	0.6	18.39475	9.026699
Factors:	1.0	128.1808	39.13346
140° Bake	0.3	N/A	N/A
Accel.	0.6	78.68867	31.12355
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 10.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 2 Speed Degrade (1.0)
1 Ass'y Defect (Bond)
19 SBCL
1 MBCG

B. 1 SBCL
1 Speed Degrade
1 SBCG

C. 1 SBCG
1 Contamination (1.0)

D. 1 SBCG

E. 1 Corrosion
1 Cracked Die
1 Leakage
2 Passivation Defects

F. 3 Corrosion
1 SBCL
1 Lifted Bond
4 Passivation Defects

G. 6 SBCL
1 Leakage
2 Contamination
2 Passivation Defect

P2764A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest 168 Hrs	125°C Dynamic Lifetest 500 Hrs	125°C Dynamic Lifetest 1K Hrs
1985	2/5740	0/3912	0/760	0/758
1986	3/5672	1/4837	0/805	0/688
Total	5/11412	1/8749	0/1565	0/1446
	A	B		

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake 48 Hrs	168 Hrs	500 Hrs	1K Hrs	Steam 168 Hrs	200 Temp Cycles
1985	0/816	0/816	0/816	0/814	—	
1986	0/903	0/903	0/903	0/903	10/1571	0/100
Total	0/1719	0/1719	0/1719	0/1717	10/1571	0/100

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours 55°C	Equivalent Hours 70°C	# Fail	Fail Rate %/1K Hrs (60% UCL) 55°C	Fail Rate %/1K Hrs (60% UCL) 70°C
2.29E + 06 0.00E + 00	03 B.I. 03*VAF	1.21E + 07 0.00E + 00	8.01E + 06 0.00E + 00	0 0		
Total 0.3 eV Failures =				0	0.0076	0.0114
2.29E + 06 8.60E + 05 0.00E + 00	0.6 B.I. 0.6 Bake 0.6 HVELT	6.34E + 07 6.76E + 07 0.00E + 00	2.80E + 07 2.68E + 07 0.00E + 00	1 0 0		
Total 0.6 eV Failures =				1	0.0015	0.0037
2.29E + 06 0.00E + 00	1.0 B.I. 1.0 HVELT	5.80E + 08 0.00E + 00	1.48E + 08 0.00E + 00	0 0		
Total 1.0 eV Failures =				0	0.0002	0.0006
Combined Failure Rate:					0.0093	0.0157
FITs:					92.91	157.40

48 Hour BI Infant Mortality 0.044%

P2764A (Continued)

Theta Ja = 103° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 40 mA

Delta T = 21.63 C
T(55) = 349.7 K
T(70) = 364.7 K
T(125) = 419.7 K
T(140) = 413.1 K

K = 8.62E-05 eV/K

Thermal Accel. Factors

		55°C	70°C
BI/ELT	0.3	5.258072	3.492002
Accel.	0.6	27.64732	12.19407
Factors:	1.0	252.7873	64.60234
140° Bake	0.3	N/A	N/A
Accel.	0.6	78.68867	31.12355
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 SBCL
2 Oxide

B. 1 SBCL

N27C64/N87C64

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest
		168 Hrs	500 Hrs	1K Hrs	500 Hrs
1986	0/300	0/300	0/150	0/150	0/140

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake		85°C/85% RH		Steam	200 Temp Cycles
	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	96 Hrs	
1986	0/297	0/297	1/300	0/298	1/300	0/234
			A		B	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 1 Basic Function

B. 1 Output

P27128A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	5/11068	3/11060	0/1530	2/1530	0/210	0/210	0/210
	A	B		C			

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	168 Hrs	
1986	0/642	0/622	1/608	0/645	4/1062	12/1058	13/4200	0/125
			D		E	F		

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.60E + 06	0.3 B.I.	1.27E + 07	8.62E + 06	0		
1.05E + 05	0.3*VAF	2.83 + 07	1.92E + 07	0		
Total 0.3 eV Failures =				0	0.0022	0.0033
2.60E + 06	0.6 B.I.	6.25E + 07	2.86E + 07	2		
3.07E + 05	0.6 Bake	2.42E + 07	9.56E + 06	1		
1.05E + 05	0.6 HVELT	2.52E + 06	1.16E + 06	0		
Total 0.6 eV Failures =				3	0.0047	0.0106
2.60E + 06	1.0 B.I.	5.21E + 08	1.41E + 08	3		
1.05E + 05	1.0 HVELT	2.10E + 07	5.71E + 06	0		
Total 1.0 eV Failures =				3	0.0008	0.0028
Combined Failure Rate:				3	0.0077	0.0167
FITs:					76.78	167.47

48 Hour BI Infant Mortality 0.045%

P27128A (Continued)

Theta Ja = 95° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 60 mA

Delta T = 29.92 C
T(55) = 358.0 K
T(70) = 373.0 K
T(125) = 428.0 K
T(140) = 413.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	Thermal Accel. Factors 70°C
BI/ELT	0.3	4.903250	3.316731
Accel.	0.6	24.04186	11.00070
Factors:	1.0	200.2688	54.41278
140° Bake	0.3	N/A	N/A
Accel.	0.6	78.68867	31.12355
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 Decode
1 Output
1 SBCL

B. 1 MBCG
1 MBCL
1 Speed Degrade

C. 2 Output

D. 1 SBCL

E. 1 SBCL
1 Decode
2 Open

F. 1 Output
3 Decode
3 Leakage
6 Open

P27256

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	2/1969	0/1964	0/345	0/345	—	—	—
1986	26/8075	3/8016	4/1035	1/913	1/96	0/95	0/95
Total	28/10044	3/9980	4/1380	1/1258	1/96	0/95	0/95
	A	B	C	D	E		

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	168 Hrs	
1985	0/487	0/487	0/487	0/478	2/298	8/296	—	—
1986	0/1405	0/1405	1/1405	2/1288	3/896	7/891	101/11972	0/175
Total	0/1892	0/1892	1/1892	2/1766	5/1194	15/1187	101/11972	
			F	G	H	I		

P27256 (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.28E + 06	0.3 B.I.	1.05E + 07	7.24E + 06	3		
4.75E + 04	0.3*VAF	1.20E + 07	8.28 + 06	0		
Total 0.3 eV Failures =				3	0.0185	0.0269
2.28E + 06	0.6 B.I.	4.85E + 07	2.29E + 07	5		
9.46E + 05	0.6 Bake	7.44E + 07	2.94E + 07	3		
4.75E + 04	0.6 HVELT	1.01E + 06	4.77E + 05	1		
Total 0.6 eV Failures =				9	0.0084	0.0198
2.28E + 06	1.0 B.I.	3.72E + 08	1.07E + 08	0		
4.75E + 04	1.0 HVELT	7.74E + 06	2.22E + 06	0		
Total 1.0 eV Failures =				0	0.0002	0.0008
Combined Failure Rate:					0.0272	0.0476
FITs:					271.85	475.55

48 Hour BI Infant Mortality 0.28%

Theta Ja = 90° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 80 mA

Delta T = 37.8 C
T(55) = 365.9 K
T(70) = 380.9 K
T(125) = 435.9 K
T(140) = 431.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	4.607027	3.167630
Accel.	0.6	21.22470	10.03388
Factors:	1.0	162.7056	46.67829
140° Bake	0.3	N/A	N/A
Accel.	0.6	78.68867	31.12355
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 24 SBCL
1 SBCG
3 Decode
B. 1 SBCL
2 Decode
C. 2 SBCG
1 MBCG
1 Decode
D. 1 SBCL
E. 1 SBCL
F. 1 SBCL
G. 1 SBCL
1 MBCL
H. 3 SBCL
2 Corrosion
I. 13 Corrosion
2 SBCL

N27C256

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	3/678	1/637	1/300	3/291	0/125	0/125	0/123
	A	B	C	D			

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake			85°C/85% RH		Steam		200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	500 Hrs	1000 Hrs	96 Hrs	168 Hrs	
1986	0/125	0/125	0/125	1/149	1/147	3/300	1/150	0/50
				E		F	G	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 2 Leakage
1 Open Pin
B. 1 Basic Function
C. 1 Basic Function
D. 2 Basic Function
1 Leakage
E. 1 Basic Function
F. 1 Basic Function
2 Leakage
G. 1 Basic Function

APPENDIX A
Failure Rate Calculations for 60% Upper Confidence Level

Step 1. Accumulate data from 48 hours of burn-in through lifetest of each lot. (Note: 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation.)

Step 2. Determine the failure mechanism for each failure and assign an activation energy (E_A) corresponding to each failure mechanism. (See Table 1 below.)

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours from 48 hours of burn-in through lifetest.

Example: 125°C Burn-In/Lifetest and a 2 lot sample

$$\frac{X}{Y} = \frac{\#\text{ failures}}{\text{total }\#\text{ devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

Device Hours = (Number of Devices) (Number of Hours)

$$\begin{aligned}\text{Total Device Hours} &= 1201\ (168\text{ hrs} - 48\text{ hrs}) + 1200\ (500\text{ hrs} - 168\text{ hrs}) \\ &\quad + 1098\ (1000\text{ hrs} - 500\text{ hrs}) + 1093\ (2000\text{ hrs} - 1000\text{ hrs}) \\ &= 1201\ (120\text{ hrs}) + 1200\ (332\text{ hrs}) + 1098\ (500\text{ hrs}) \\ &\quad + 1093\ (1000\text{ hrs}) \\ &= 2.185 \times 10^6\text{ Device Hours}\end{aligned}$$

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \bullet \exp\left[\frac{E_A}{KT}\right]$$

$K = 8.617 \times 10^{-5}$ eV/°Kelvin (Boltzmann's constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A \bullet \exp\left[\frac{E_A}{KT_1}\right]}{A \bullet \exp\left[\frac{E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

$$R_1 = R_2 \bullet \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398.15°K$, $T_1 = 328.15°K$

$$R_2 = .024\, R_1, \text{ or } R_1 = 41.7\, R_2$$

Therefore, 1 hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy E_A = 0.6 eV. Then 41.7 is the thermal acceleration factor for ΔT.

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:
The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the desired and actual burn-in/lifetest temperatures.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\,(IV\ @\ T_{Ambient}) + T_{Ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	#Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

Using the data table and the equation below, the failure rates for individual failure mechanisms and the total combined failure rate can be predicted. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL:

$$\%\ \text{Fail/1K Hours} = \left[\frac{1.049\ (\#\text{failures for a particular } E_A) + 1.0305}{\text{Equivalent Hrs @ } T_1}\right]\left[10^5\right]$$

Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient} = 125°C$ and I_{CC} active is 65 mA at $T_{Ambient} = 55°C$.

Also assume that $\theta_{JA} = 35°C/W$.

Then,

$$T_2 = (35°C/W)\ (57\ mA)\ (5V) + 125°C$$

$$\approx 135°C = 408.15°K$$

$$T_1 = (35°C/W)\ (60\ mA)\ (5V) + 55°C$$

$$\approx 65°C = 338.15°K$$

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C % Fail/ 1K Hrs
0.3	2.185×10^6	5.85	1.278×10^7	0	0.0081
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
			Total Combined Failure Rate =		0.0126
			=		126 FITs

Example 2:

Assume that an additional lot of 800 HMOS*IIE devices is burned in using a 6.5V lifetest. Using Table 2 below, a voltage acceleration factor of 55 results from a 20% overstress (5.5V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0/800	1/800	0/799

$$\text{Device Hours} = 800\ (48\ hrs - 0\ hrs) + 800\ (168\ hrs - 48\ hrs) + 799\ (500\ hrs - 168\ hrs)$$
$$= 3.997 \times 10^5$$

Table 2. Time-Dependent Oxide Failure Accelerations

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/CM)	Acceleration Factor at ___% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5×10^7
HMOS*E	5	700	0.714	3.2	10	320	99,500
HMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8
CHMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8

ASSUMES:
1. No Bias Generators
2. Depletion Loads

*HMOS & CHMOS are patented processes of Intel Corporation.

Since this voltage accelerated stress is used to predict an oxide breakdown failure rate, the 5.5V burn-in/lifetest 55°C equivalent hours for $E_A = 0.3$ eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours as follows:

125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C
5.5V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 x 55)	1.286×10^8
Total Equivalent $E_A = 0.3$ eV Device Hours =				1.414×10^8

The following failure rate predictions include the total equivalent 55°C, $E_A = 0.3$ eV device hours found above:

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C	# Fail	55°C % Fail/ 1K Hours
0.3	2.185×10^6	5.85	—	—	—
0.3 + 55(1)	3.997×10^5	(5.85 x 55)	1.414×10^8	1	0.0015
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
				Total Combined Failure Rate =	0.0060
				=	60 FITs

NOTES:

(1) The notation 0.3 + 55 is used to show that 6.5V and 5.5V burn-in/lifetest equivalent hours have been combined.

(2) Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.

APPENDIX B
EPROM Bit Maps and Die Photos

							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	A11
							1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0	A3
							0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	A2
							0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	A1
A 10	A 9	A 8	A 7	A 6	A 5	A 4	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	A0
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1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
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1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
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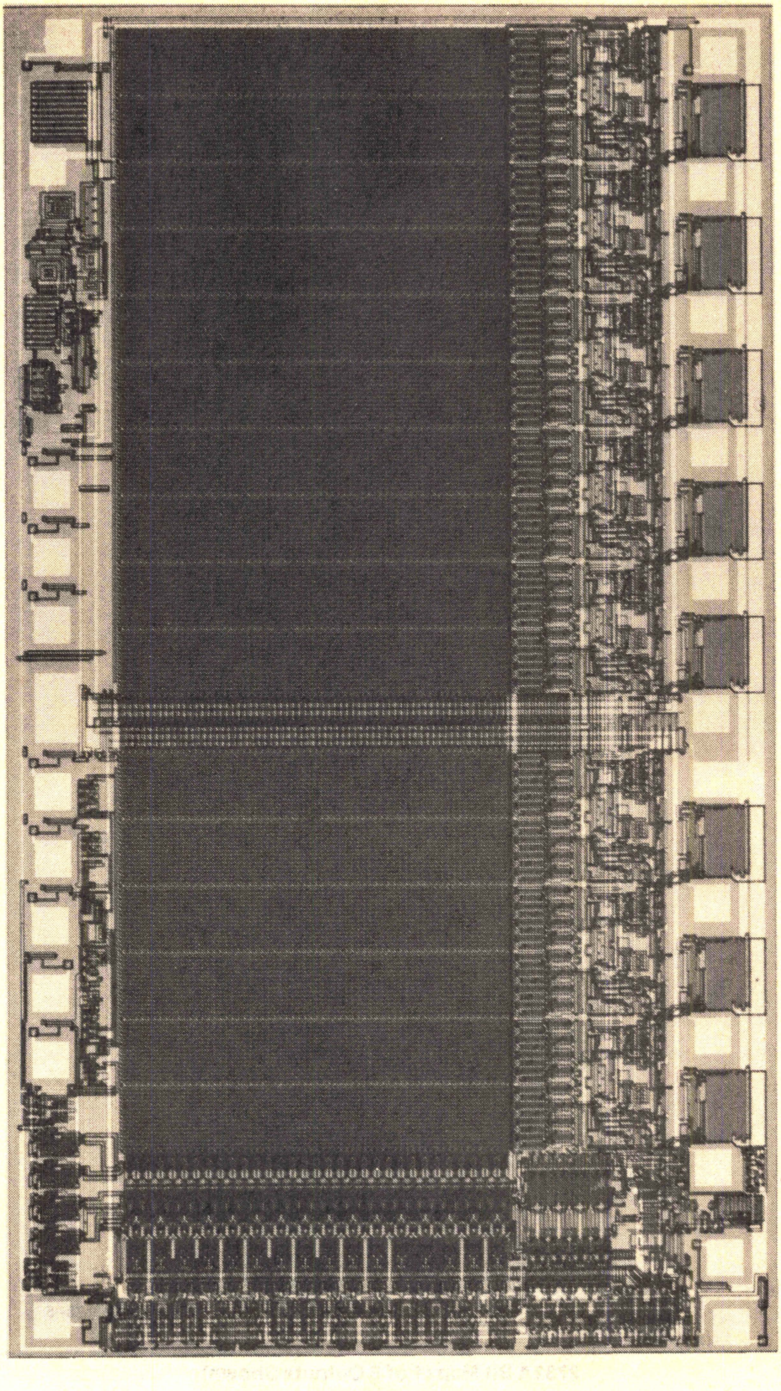
1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

210473-5

2732A Bit Map (1 of 8 Outputs Shown)



210473–6

2732A Die Photograph

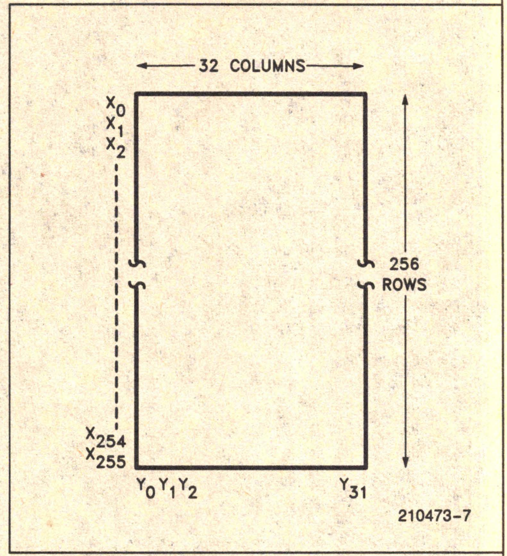
Column Selects

	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}	Y_{16}	Y_{17}	Y_{18}	Y_{19}	Y_{20}	Y_{21}	Y_{22}	Y_{23}	Y_{24}	Y_{25}	Y_{26}	Y_{27}	Y_{28}	Y_{29}	Y_{30}	Y_{31}
A_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
A_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A_0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A_{10}	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A_{11}	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

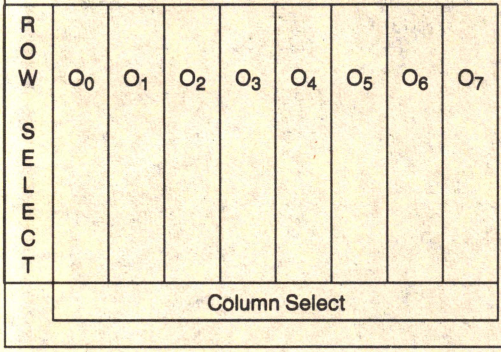
Row Selects

	X_0	X_1	X_2	X_3	X_4	X_5	X_{253}	X_{254}	X_{255}
A_7	0	0	0	0	0	0	1	1	1
A_6	0	0	0	0	0	0	1	1	1
A_5	0	0	0	0	0	0	1	1	1
A_4	0	0	0	0	0	0	1	1	1
A_3	0	0	0	0	0	0	1	1	1
A_{12}	0	0	0	0	1	1	1	1	1
A_9	0	0	1	1	0	0	0	1	1
A_8	0	1	0	1	0	1	1	0	1

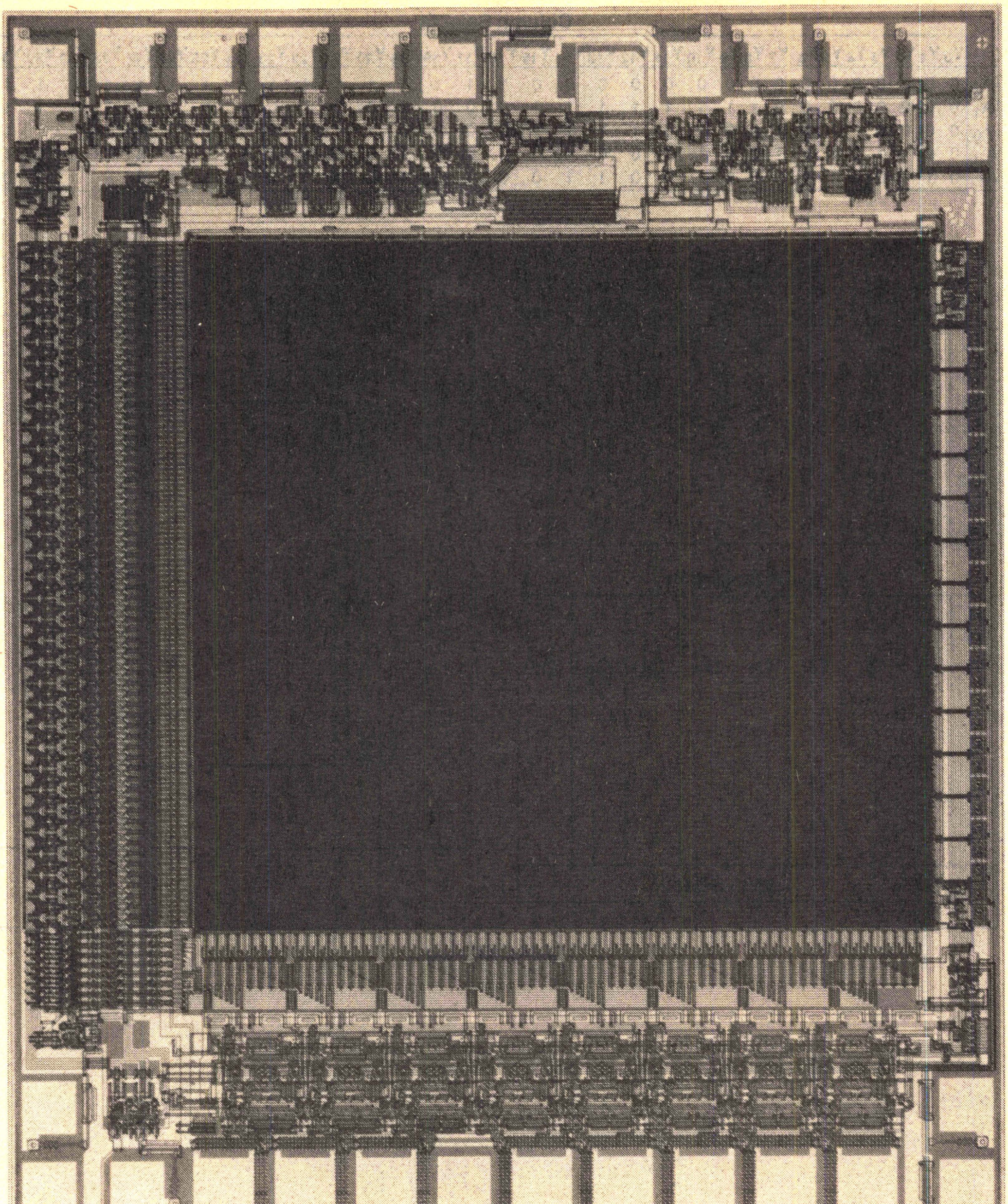
Bit Map for One Output (Same for All Outputs)


32 COLUMNS
X_0
X_1
X_2
256 ROWS
X_{254}
X_{255}
Y_0 Y_1 Y_2
Y_{31}
210473–7

Array Organization


ROW SELECT
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
Column Select

2764A Bit Map



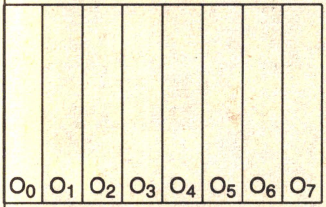
210473–8

2764A Die Photograph

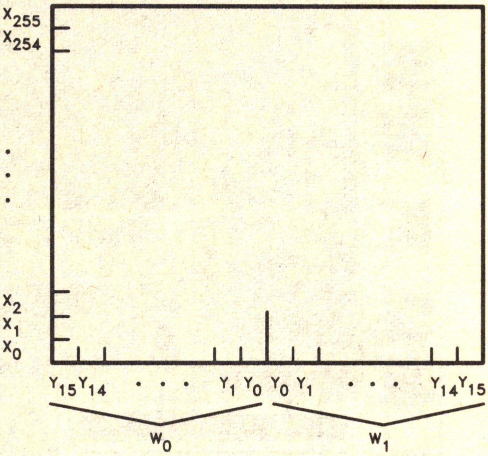
Address Decoding

	X Decode			Z Decode			R Decode			Y Decode				W Decode	
	A_{12}	A_7	A_6	A_{11}	A_9	A_8	A_5	A_4		A_{10}	A_0	A_1	A_3		A_2
X_0	0	0	0	0	0	0	0	0	Y_0	0	0	0	0	W_0	0
X_1	0	0	0	0	0	0	0	1	Y_1	0	0	0	1	W_1	1
X_2	0	0	0	0	0	0	1	0	Y_2	0	0	1	0		
•					•				•						
•					•				•						
•					•				•						
X_{254}	1	1	1	1	1	1	1	0	Y_{14}	1	1	1	0		
X_{255}	1	1	1	1	1	1	1	1	Y_{15}	1	1	1	1		

Array Organization

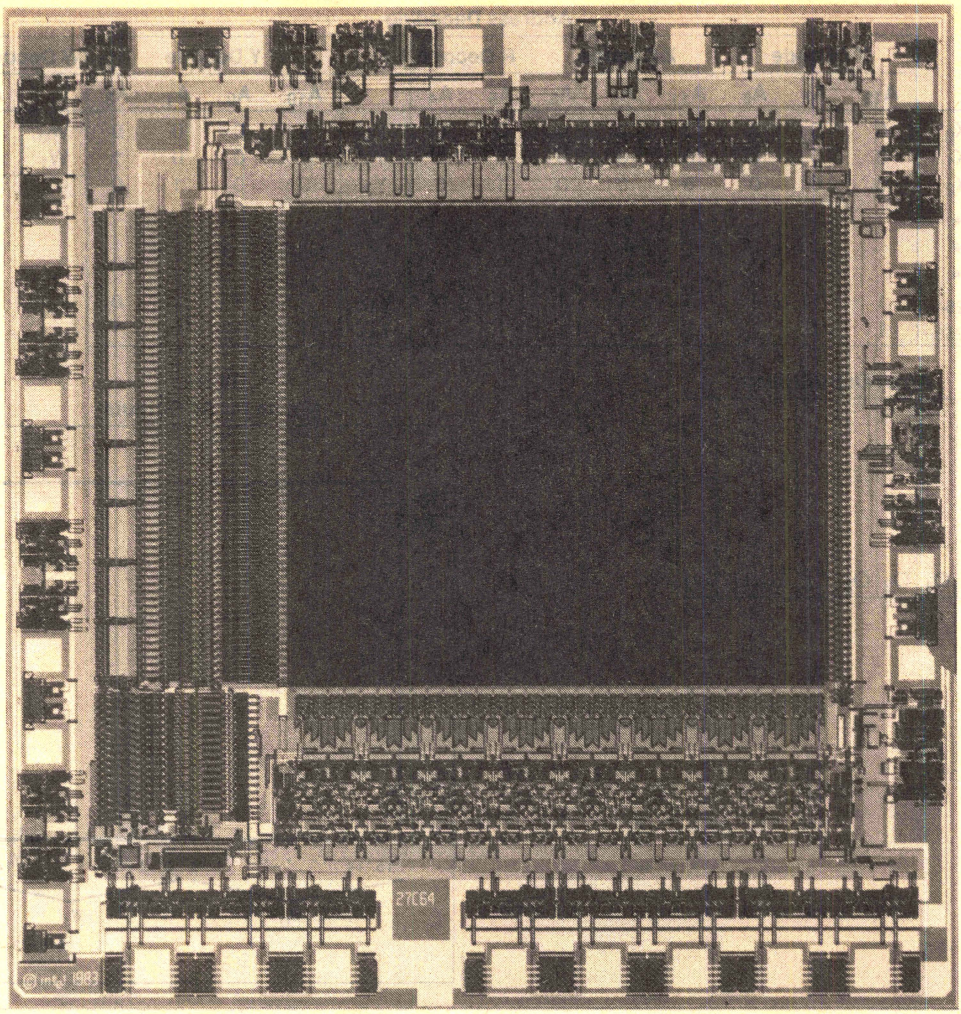

O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7

Bit Map
(Same for All Outputs)


X_{255}
X_{254}
X_2
X_1
X_0
Y_{15} Y_{14} • • • Y_1 Y_0
Y_0 Y_1 • • • Y_{14} Y_{15}
W_0
W_1

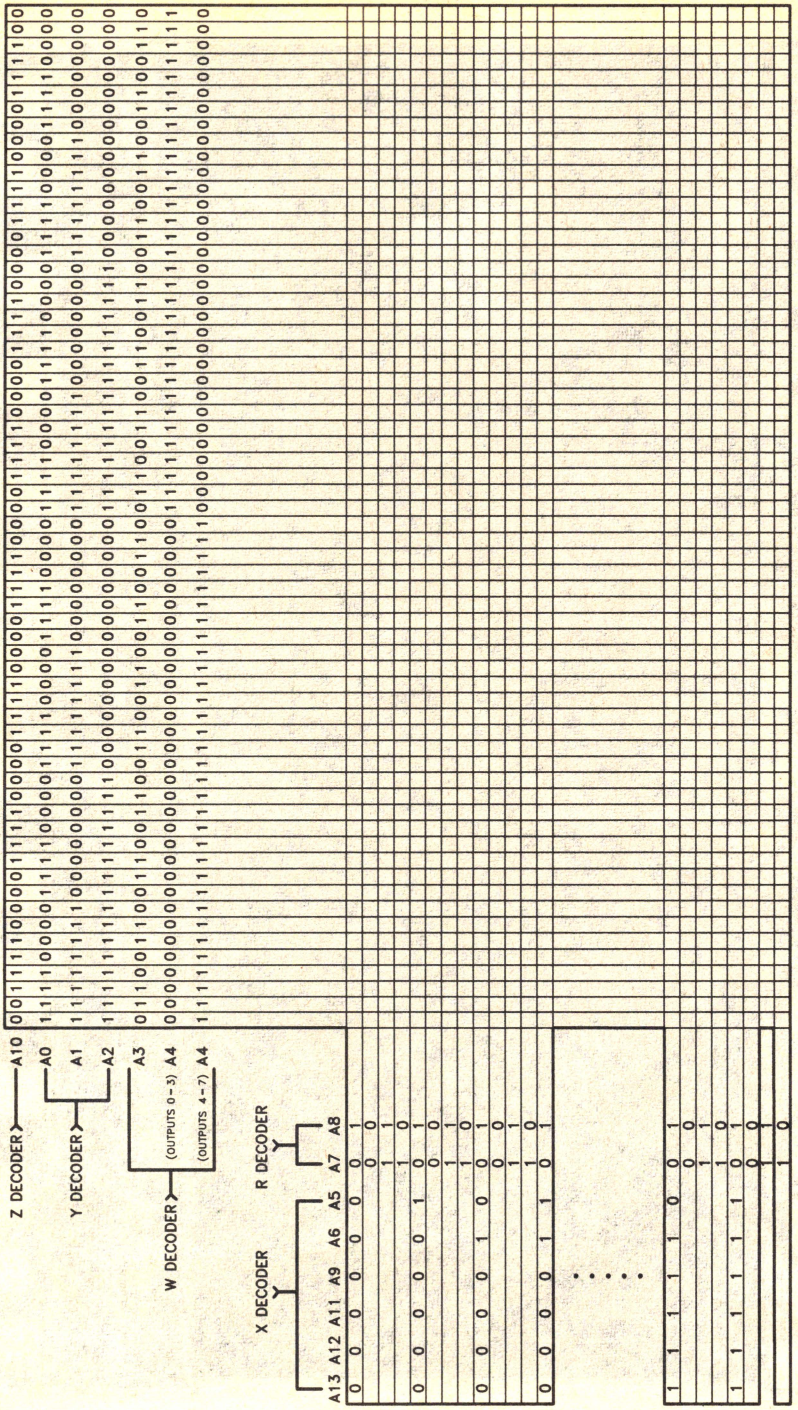
210473-9

27C64 Bit Map

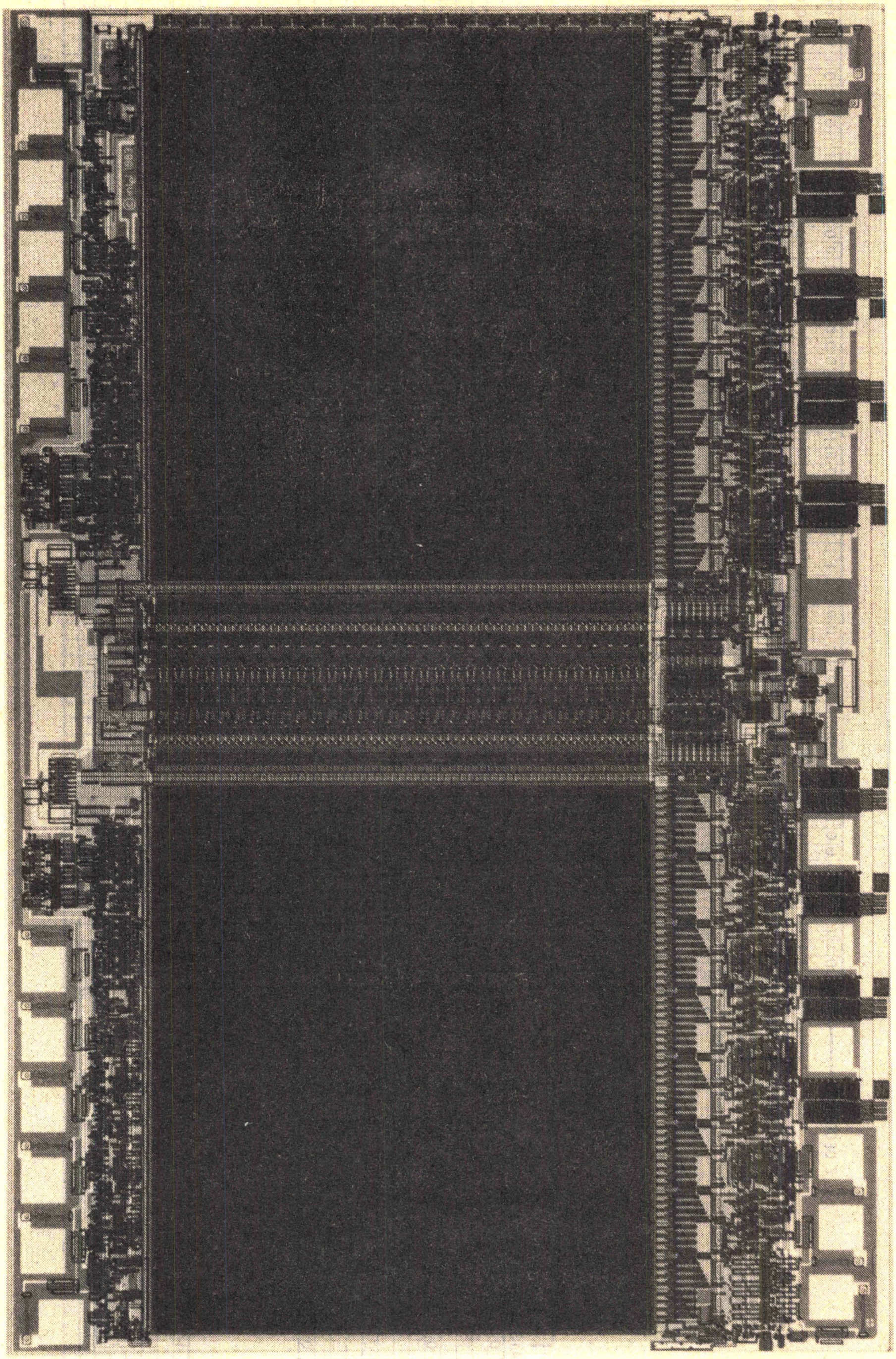

27C64
© intel 1983

210473-10

27C64 Die Photograph


Z DECODER
A10 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0
Y DECODER
A0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0
A1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
A2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
W DECODER
A3 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0
(OUTPUTS 0–3) A4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
(OUTPUTS 4–7) A4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
R DECODER
A8 1 0 1 0 1 0 1 0 1 0 1 0 1 … 1 0 1 0 1 0 1 0
A7 0 0 1 1 0 0 1 1 0 0 1 1 0 … 0 0 1 1 0 0 1 1
X DECODER
A5 0 1 0 1 … 0 1
A6 0 0 1 1 … 1 1
A9 0 0 0 0 … 1 1
A11 0 0 0 0 … 1 1
A12 0 0 0 0 … 1 1
A13 0 0 0 0 … 1 1
210473-14

27128A Bit Map



210473–15

27128A Die Photograph

Address Decoding

Y Decode

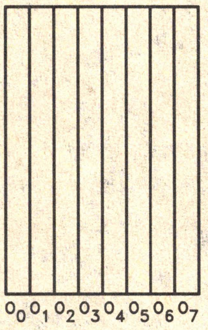
	A4	A10	A1	A2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•		•		
•		•		
•		•		
Y_{15}	1	1	1	1

W Decode

	A0	A3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

	X Decode						R Decode		
	A14	A13	A12	A8	A7	A6	A11	A9	A5
X_0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	1	0
•				•					
•				•					
•				•					
X_{511}	1	1	1	1	1	1	1	1	1

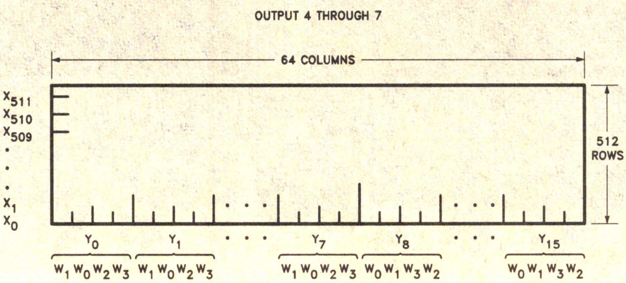
Array Organization



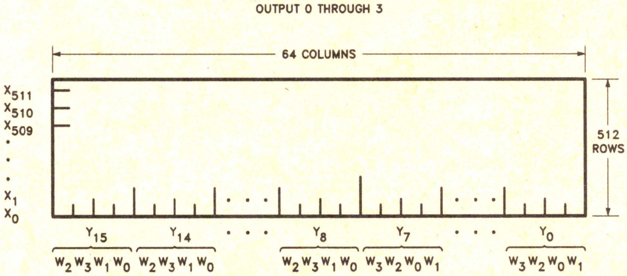
O0 O1 O2 O3 O4 O5 O6 O7

210473-16

Bit Map



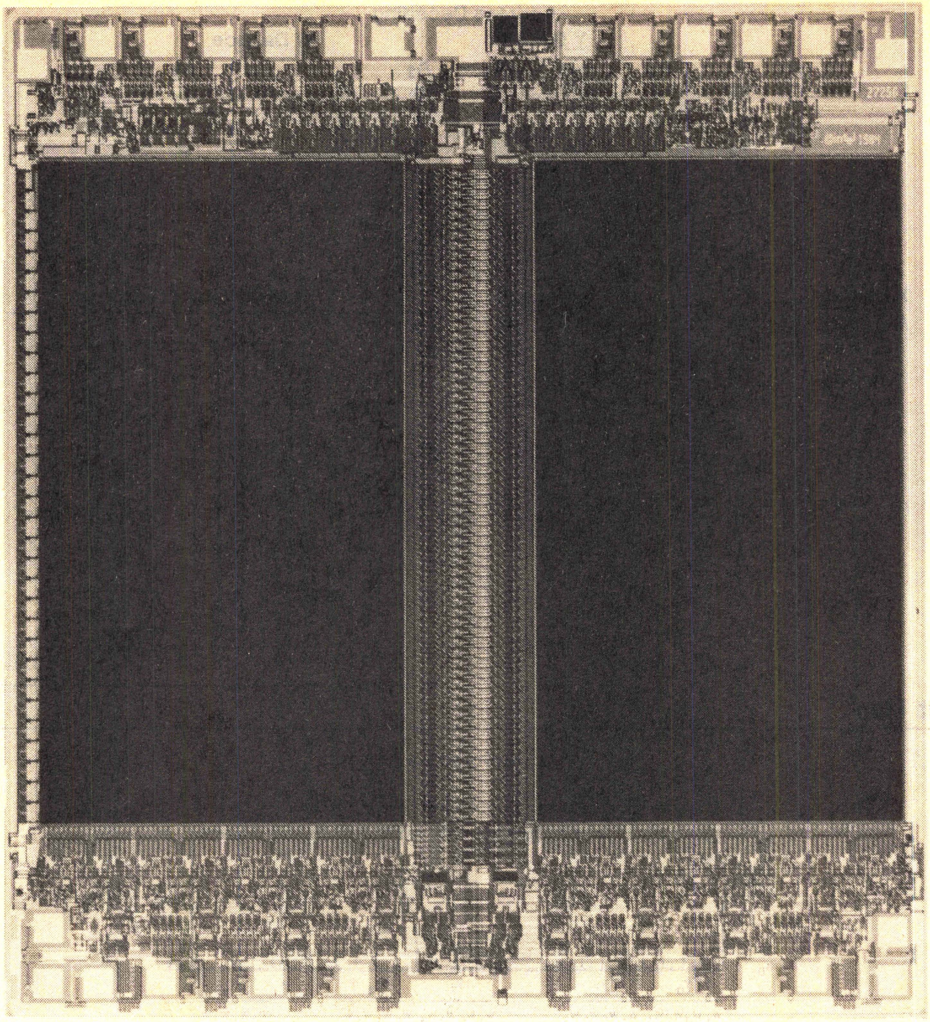
OUTPUT 4 THROUGH 7
64 COLUMNS
512 ROWS
X511
X510
X509
X1
X0
Y0
Y1
Y7
Y8
Y15
W1 W0 W2 W3
W1 W0 W2 W3
W1 W0 W2 W3
W0 W1 W3 W2
W0 W1 W3 W2



OUTPUT 0 THROUGH 3
64 COLUMNS
512 ROWS
X511
X510
X509
X1
X0
Y15
Y14
Y8
Y7
Y0
W2 W3 W1 W0
W2 W3 W1 W0
W2 W3 W1 W0
W3 W2 W0 W1
W3 W2 W0 W1

210473-17

27256 Bit Map



210473-18

27256 Die Photograph

Address Decoding

4 Decode

	A_2	A_1	A_0	A_{10}
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

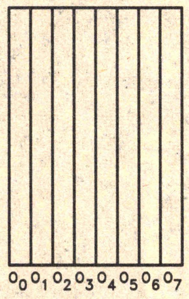
W Decode

	A_4	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

X Decode

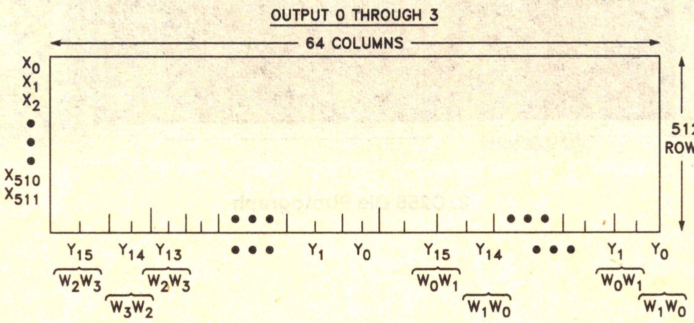
	A_{14}	A_{13}	A_{12}	A_7	A_6	A_5	A_{11}	A_9	A_8
X_0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	1	0
•									
•									
X_{510}	1	1	1	1	1	1	1	1	0
X_{511}	1	1	1	1	1	1	1	1	1

Array Organization

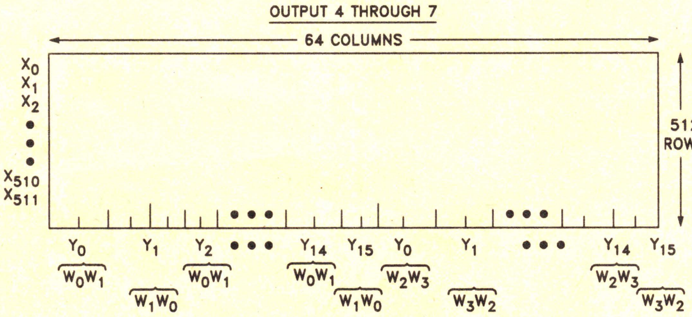

O_0 O_1 O_2 O_3 O_4 O_5 O_6 O_7

210473-16

Bit Map

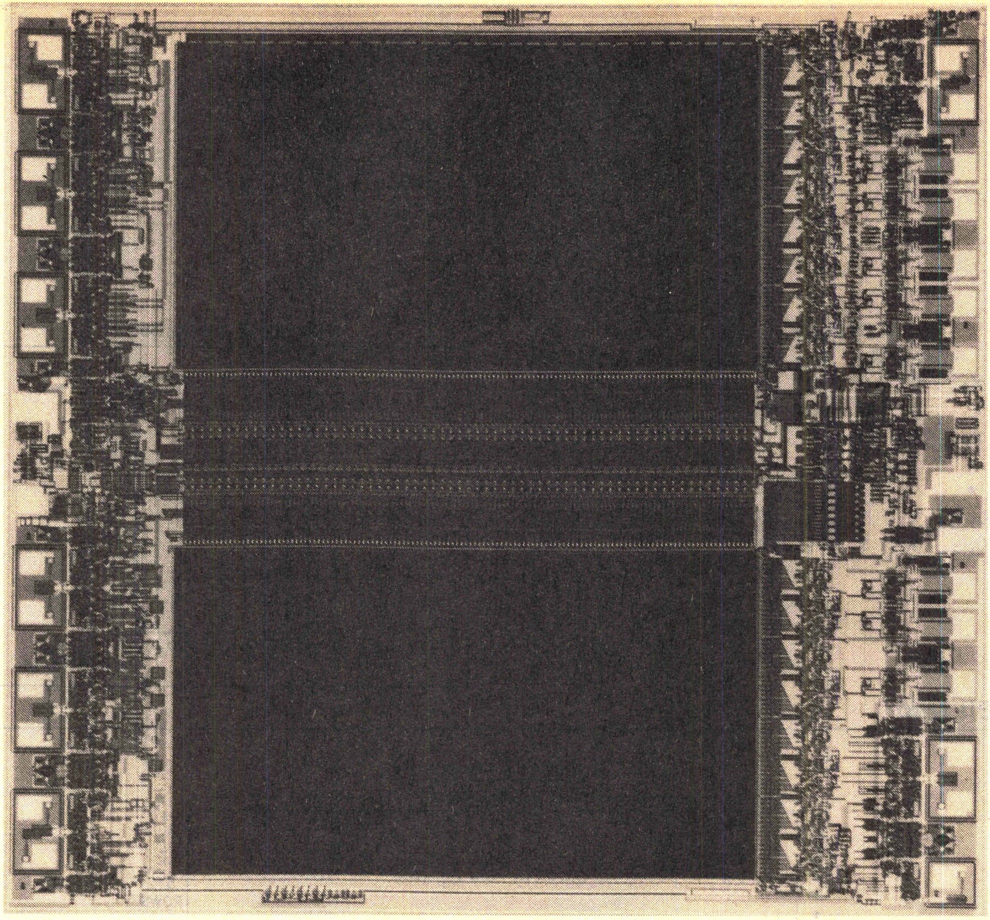

OUTPUT 0 THROUGH 3
64 COLUMNS
512 ROWS
X_0
X_1
X_2
X_{510}
X_{511}
Y_{15} Y_{14} Y_{13} • • • Y_1 Y_0 Y_{15} Y_{14} • • • Y_1 Y_0
W_2W_3
W_3W_2
W_2W_3
W_0W_1
W_1W_0
W_0W_1
W_1W_0

210473-24


OUTPUT 4 THROUGH 7
64 COLUMNS
512 ROWS
X_0
X_1
X_2
X_{510}
X_{511}
Y_0 Y_1 Y_2 • • • Y_{14} Y_{15} Y_0 Y_1 • • • Y_{14} Y_{15}
W_0W_1
W_1W_0
W_0W_1
W_0W_1
W_1W_0
W_2W_3
W_3W_2
W_2W_3
W_3W_2

210473-25

27C256 Bit Map



210473-26

27C256 Die Photograph

Address Decoding

Y Decode

	A_4	A_{10}	A_1	A_2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•		•		
•		•		
•		•		
Y_{15}	1	1	1	1

W Decode

	A_0	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

X Decode / R Decode

	X Decode							R Decode		
	A_{15}	A_{14}	A_{13}	A_{12}	A_8	A_7	A_6	A_{11}	A_9	A_5
X_0	0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	0	1	0
•			•				•			•
•			•				•			•
•			•				•			•
X_{1023}	1	1	1	1	1	1	1	1	1	1

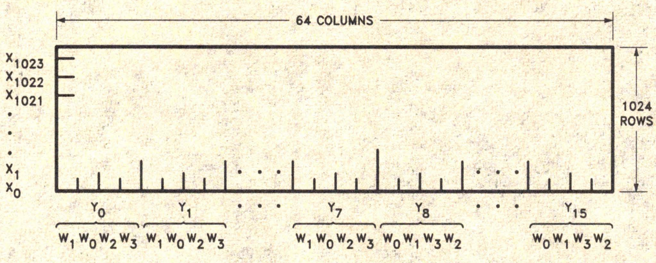
Array Organization

O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7

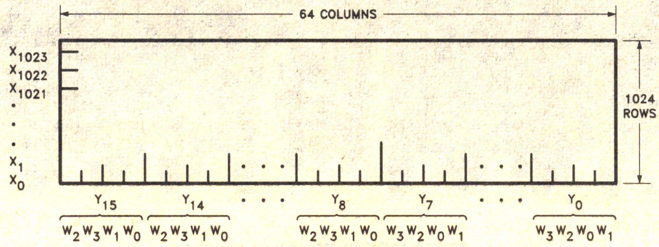
210473-19

Bit Map

OUTPUT 4 THROUGH 7

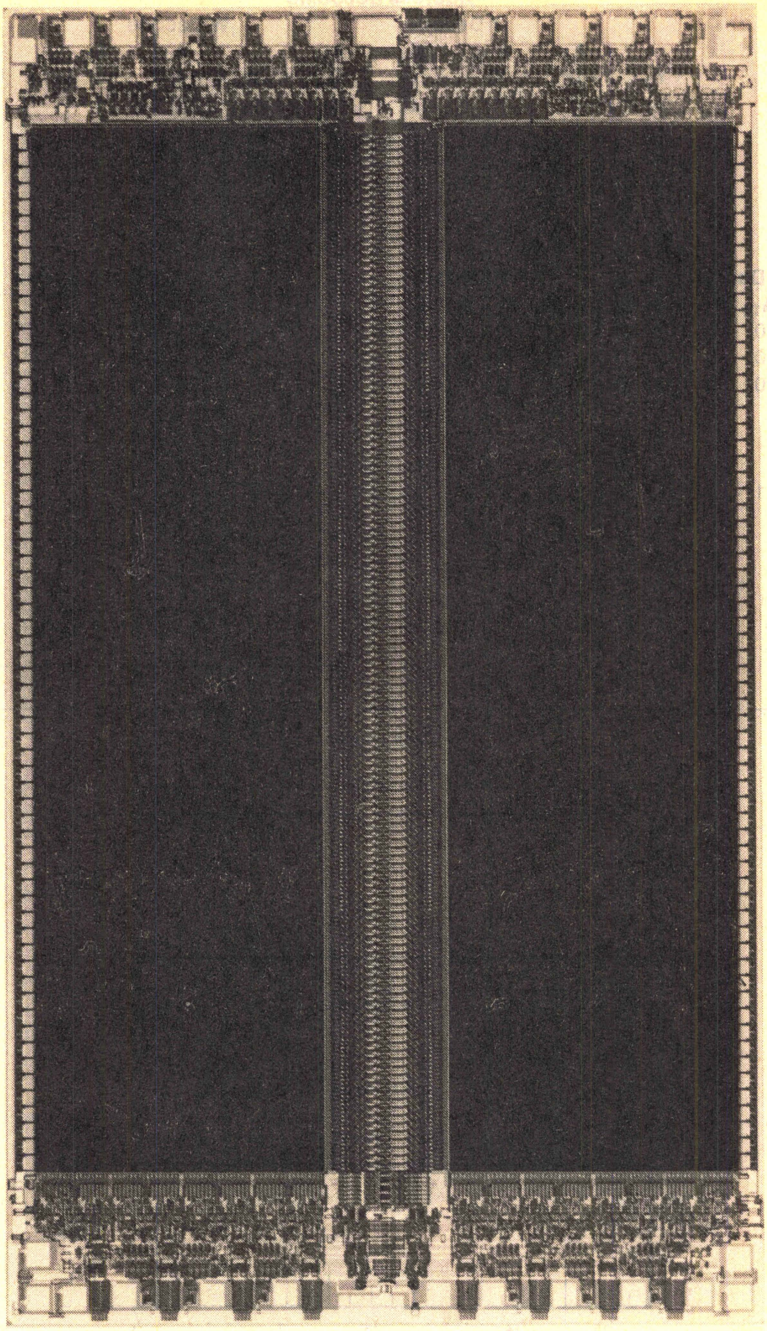

64 COLUMNS
1024 ROWS
X_{1023}
X_{1022}
X_{1021}
X_1
X_0
Y_0
Y_1
Y_7
Y_8
Y_{15}
$W_1 W_0 W_2 W_3$
$W_1 W_0 W_2 W_3$
$W_1 W_0 W_2 W_3$
$W_0 W_1 W_3 W_2$
$W_0 W_1 W_3 W_2$

OUTPUT 0 THROUGH 3


64 COLUMNS
1024 ROWS
X_{1023}
X_{1022}
X_{1021}
X_1
X_0
Y_{15}
Y_{14}
Y_8
Y_7
Y_0
$W_2 W_3 W_1 W_0$
$W_2 W_3 W_1 W_0$
$W_2 W_3 W_1 W_0$
$W_3 W_2 W_0 W_1$
$W_3 W_2 W_0 W_1$

210473-20

27512/27513 Bit Map



210473–21

27512/27513 Die Photograph

27010 Row Decoding

Row	A_3	A_4	A_{12}	A_{15}	A_{16}	A_{14}	A_{11}	A_{13}	A_9	A_8
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

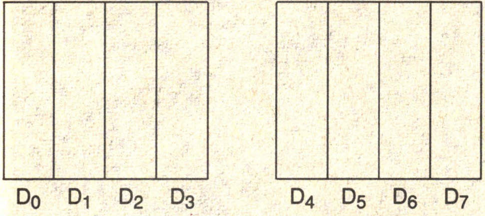
X Decode: A_{16}, A_{15}, A_{14}, A_{12}, A_{11}, A_4 and A_3
R Decode: A_{13}, A_9 and A_8

27010 Column Decoding

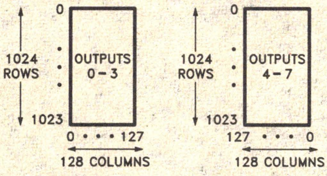
Column	A_2	A_1	A_7	A_6	A_5	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_7, A_6 and A_5
Z Decode: A_{10}

27010 Array Organization


D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7

27010 Row & Column Layout


0
1024 ROWS
OUTPUTS 0 – 3
1023
0 • • • 127
128 COLUMNS
0
1024 ROWS
OUTPUTS 4 – 7
1023
127 • • • 0
128 COLUMNS

210473–27

Figure 5. 27010 Bit Map

27011 Row Decoding

Row	$\overline{D_0}$	$\overline{D_1}$	A_6	A_7	A_{12}	A_8	$\overline{D_2}$	A_9	A_{13}	A_{11}
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

X Decode: D_2, D_1, D_0, A_{12}, A_8, A_7 and A_6
R Decode: A_{13}, A_{11} and A_9

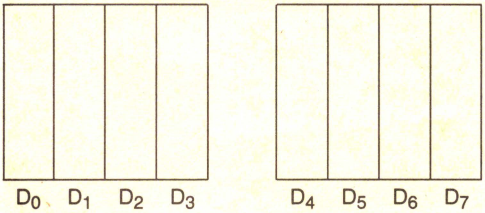
NOTE:
$\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ are complemented page-select write input data.
e.g., $\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ = 000 corresponds to page data 07H.

27011 Column Decoding

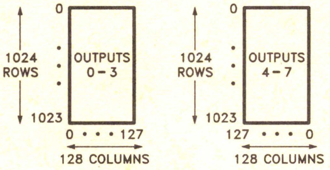
Column	A_2	A_1	A_5	A_4	A_3	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_5, A_4 and A_3
Z Decode: A_{10}

27011 Array Organization

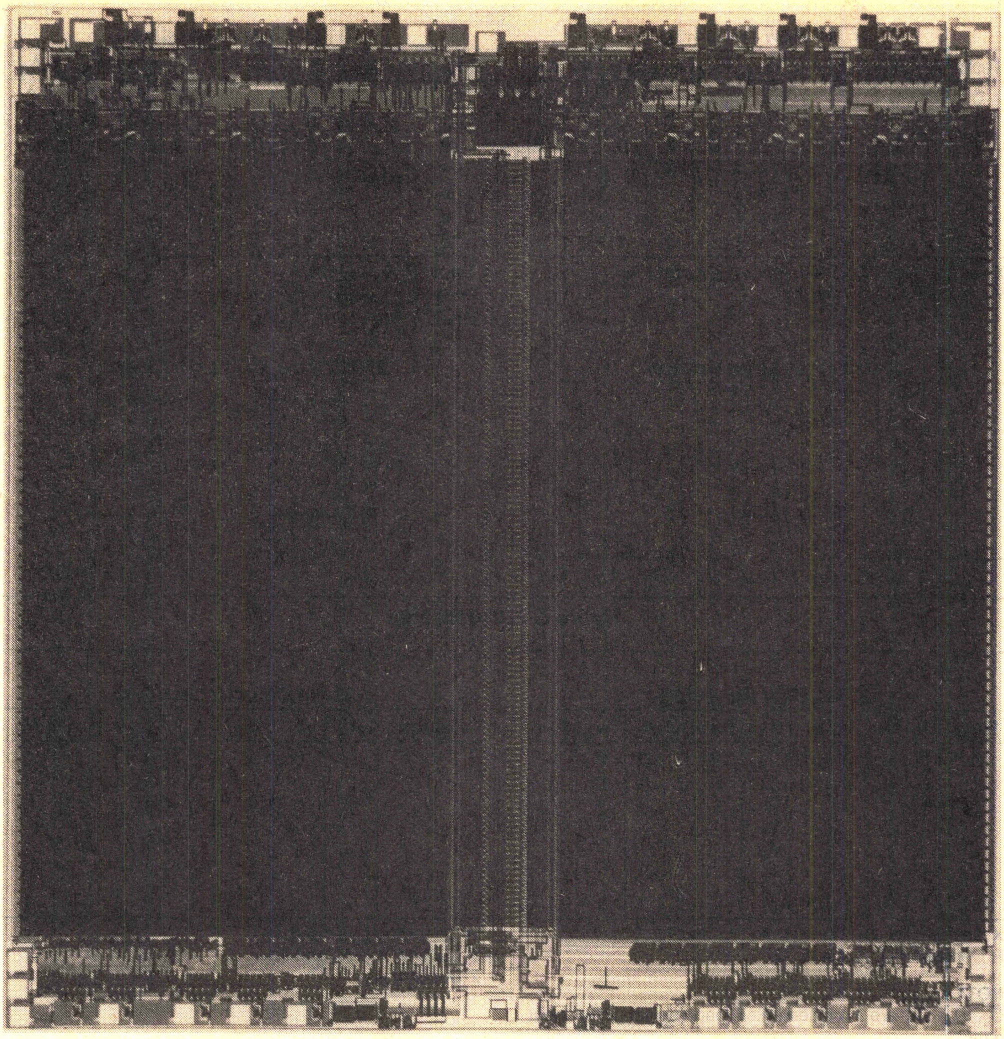

D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7

27011 Row and Column Layout


0
1024 ROWS
OUTPUTS 0 – 3
1023
0 • • • 127
128 COLUMNS
0
1024 ROWS
OUTPUTS 4 – 7
1023
127 • • • 0
128 COLUMNS

210473–28

Figure 6. 27011 Bit Map



210473-29

27010/27011 Die Photograph

27210 Row Decoding

Row	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_{15}	A_{14}	A_{13}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0
•					•				
•					•				
•					•				
511	1	1	1	1	1	1	1	1	1

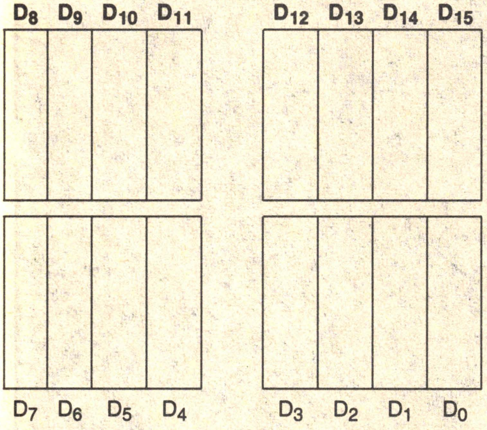
R Decode: A_{15}, A_{14} and A_{13}
X Decode: A_{12}, A_{11}, A_{10}, A_9, A_8 and A_7

27210 Column Decoding

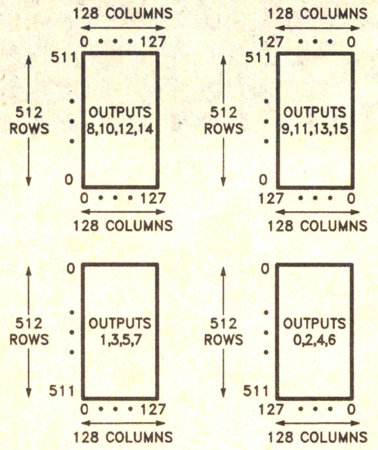
Y Decode	A_3	A_2	A_1	A_0	W Decode	A_6	A_5	A_4
Y_0	0	0	0	0	W_0	0	0	0
Y_1	0	0	0	1	W_1	0	0	1
Y_2	0	0	1	0	W_2	0	1	0
•		•			•		•	
•		•			•		•	
•		•			•		•	
Y_{15}	1	1	1	1	W_7	1	1	1

Column	W		Y	Column	W		Y
0	W_0	>	Y_{15}	64	W_4	>	Y_{15}
1	W_1			65	W_5		
2	W_1	>	Y_{14}	66	W_5	>	Y_{14}
3	W_0			67	W_4		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
30	W_1	>	Y_0	94	W_5	>	Y_0
31	W_0			95	W_4		
32	W_2	>	Y_0	96	W_6	>	Y_0
33	W_3			97	W_7		
34	W_3	>	Y_1	98	W_7	>	Y_1
35	W_2			99	W_6		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
62	W_3	>	Y_{15}	126	W_7	>	Y_{15}
63	W_2			127	W_6		

27210 Array Organization

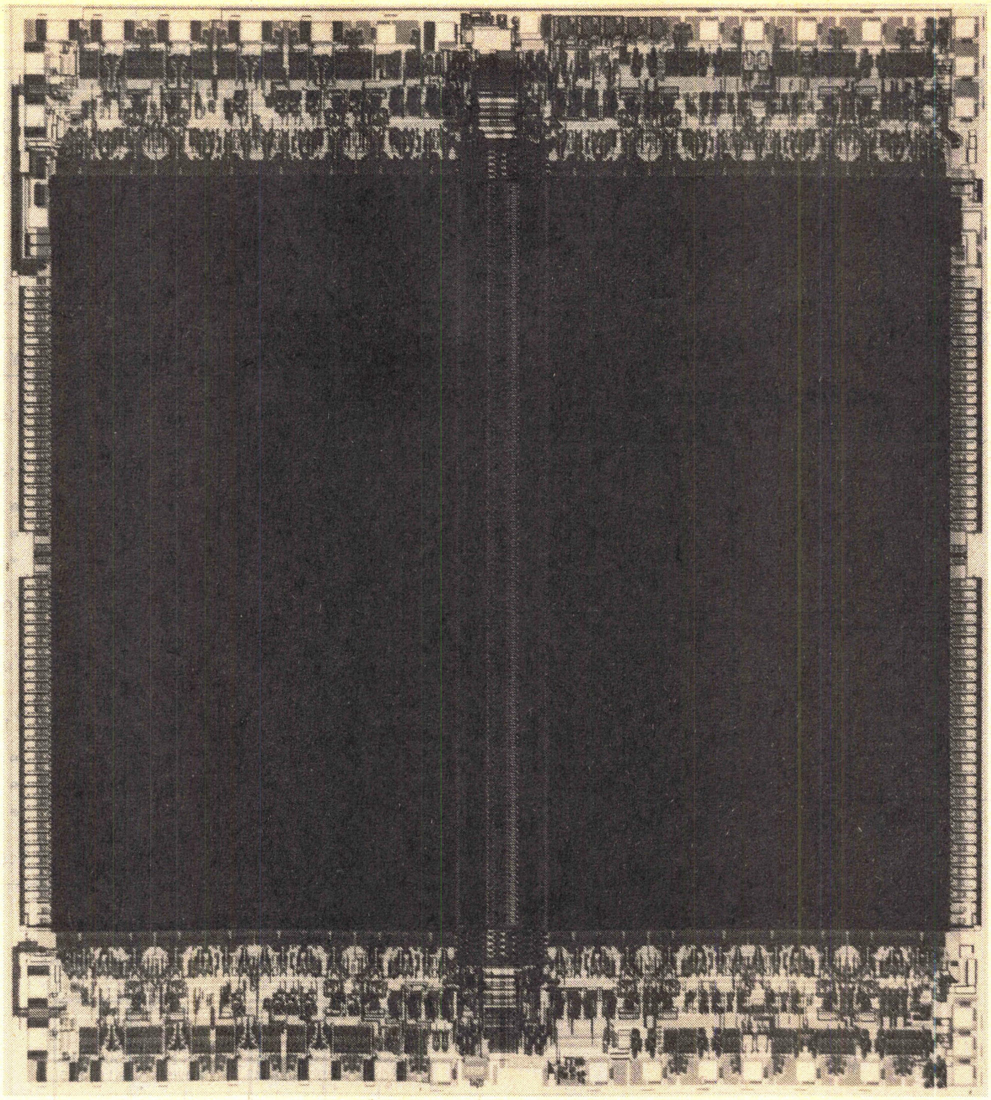

D8 D9 D10 D11
D12 D13 D14 D15
D7 D6 D5 D4
D3 D2 D1 D0

27210 Row & Column Layout


128 COLUMNS
0 • • • 127
511
512 ROWS
OUTPUTS 8,10,12,14
0
0 • • • 127
128 COLUMNS
128 COLUMNS
127 • • • 0
511
512 ROWS
OUTPUTS 9,11,13,15
0
127 • • • 0
128 COLUMNS
0
512 ROWS
OUTPUTS 1,3,5,7
511
0 • • • 127
128 COLUMNS
0
512 ROWS
OUTPUTS 0,2,4,6
511
127 • • • 0
128 COLUMNS

210473-30

Figure 9. 27210 Bit Map



210473-31

27010 Die Photograph

intel

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EPROMs Adapt To Emerging Developments In Technologies, Configurations, Packages

BY
LAWRENCE PALLEY
EPROM MARKETING MANAGER
INTEL CORPORATION

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EPROMs Adapt To Emerging Developments In Technologies, Configurations, Packages

CMOS EPROMs Evolve To Meet Growing System Needs

By Lawrence Palley

Changes in digital-system-memory architectures and production methodologies are driving changes in the traditional EPROM market. An accelerated transition to systems with easily run, built-in feature sets (programs) requires denser components for compactness. At the same time, an increasing focus on "design for manufacturability" requires components with lower costs and high reliability. In both cases, alternatives are being derived with EPROMs that are now evolving to meet a growing variety of system needs. This evolution is exemplified by CMOS technologies, plastic packaging and page-addressed design configurations.

This author is EPROM Marketing Manager at Intel Corp., Folsom, California.

The use of digital computing is now extending beyond those with engineering or technical backgrounds. Today, the power of data processing must be accessible to businessmen, consumers, and non-electronic technicians. Quick and reliable execution of canned application programs is a must. Instructions for electronic-system operation must be readily accessible and the barrier of working with the machine reduced.

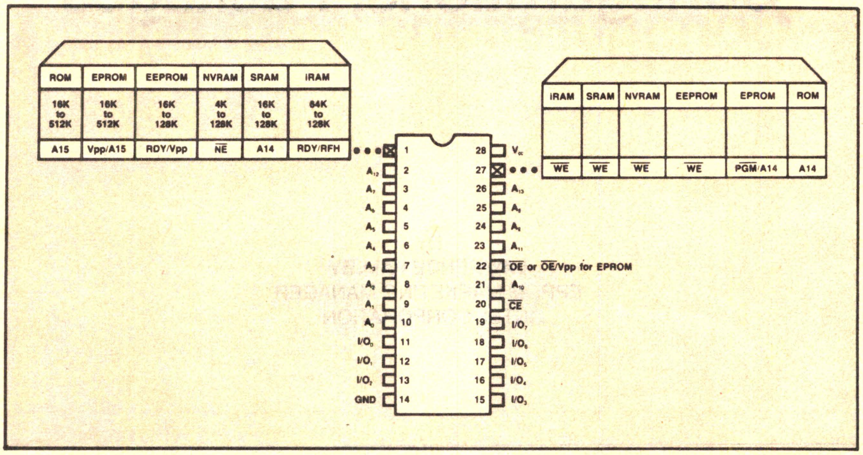
An analogy can be made with the automobile. Early cars were difficult to operate. Users had to understand the operation of the engine and drive mechanics. They had to go through extensive start-up procedures (open the choke, turn the crank, etc.). And when the automobile frequently broke down, the user generally had to know how to fix it.

Today, cars include many "user-friendly" features-automatic transmissions, electronic ignition, etc., which make them simple to use. In general, drivers have little interest in the automobile's inner engine and mechanical workings. They want to use the car for its benefit (getting around town) and expect it to accomplish its purpose reliably.

Computing Arena

A similar situation has occurred in the computing arena. Large amounts of software have been incorporated integrally into digital equipment. Such integral software now includes bootstrap programs, operting systems, diagnostics, instructions on use, and even dedicated applications. Users need no longer be trained on the inner workings of the computer, but rather focus on obtaining the desired output. All the operations are made simpler by the software.

Various methods have been used to incorporate this software into systems, but the most common has been an extension of the concept of downloading disk-based software to RAM. More recently, the placement of this software in non-volatile semiconductor memories has increased (converting software into firmware).


ROM
EPROM
EEPROM
NVRAM
SRAM
IRAM
16K to 512K
16K to 512K
16K to 128K
4K to 128K
16K to 128K
64K to 128K
A15
Vpp/A15
RDY/Vpp
$\overline{NE}$
A14
RDY/RFH
IRAM
SRAM
NVRAM
EEPROM
EPROM
ROM
$\overline{WE}$
$\overline{WE}$
$\overline{WE}$
$\overline{WE}$
$\overline{PGM}$/A14
A14
1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
I/O_0 11
I/O_1 12
I/O_2 13
GND 14
28 V_{cc}
27
26 A_{13}
25 A_8
24 A_9
23 A_{11}
22 $\overline{OE}$ or $\overline{OE}$/Vpp for EPROM
21 A_{10}
20 $\overline{CE}$
19 I/O_7
18 I/O_6
17 I/O_5
16 I/O_4
15 I/O_3

The universal memory site pin configuration enables designers to mix and match ROMs, EPROMs, EEPROMs, NVRAMs, IRAMs and static RAMs by simply changing jumper connections.

The firmware alternative offers substantial benefits to both users and manufacturers. To run a program the user can use dedicated keys on the keyboard. The microprocessor then directly accesses the program, and does not have to encounter problems such as lost or erased program disks.

Aiding The Manufacturer

To the manufacturer, adding diagnostics and documentation to the firmware enables quick debugging of system problems and reduces customer questions on operation. The addition of applications software also enables the manufacturer to sell a complete, integrated system, specifically tailored to his customer base.

One additional, and less obvious advantage to the manufacturer is the added level of software security maintained by firmware. Not only is the software further removed from illegal copying, but it is also removed from the inadvertent user, one who could erase or alter it into an unusable form.

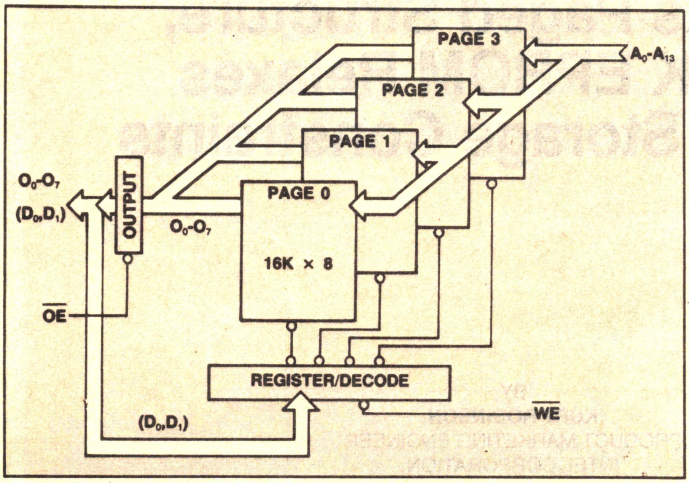
Firmware-intensive systems, with ROM or EPROM, have been extensively used in applications with realtime-processing needs. Instruments, telecommunications equipment, and industrial controllers use large amounts of firmware to perform their various tasks. Additionally, they incorporate diagnostics and menu-driven operator instructions to simplify operation.

One of the older limitations on adding firmware to a system was its usage of the processor's memory space. Earlier 8-bit processors were only capable of addressing 64 kbytes of program or data directly. A 32-kbyte applications program would use half of this area. Therefore, the best use of this area was to implement it with RAM and rely on disk memory for the firmware. Programs would then be swapped in and out of this memory space.

New processors, using 16-bit internal architectures, are able to address much larger memory spaces. Typically, these processors address upward of 1 Mbyte directly. A fixed 256-kbyte non-volatile memory system, using four 27512 EPROMs for instance, would leave more than enough RAM memory for directly accessible data storage.

An alternative for microcontrollers and 8-bit microprocessors is to use a page-addressed system such as that designed into the 27513 EPROM. This device effectively fits 64 kbytes of firmware into a 16-kbyte address space. Processors and controllers with 64-kbyte address limits can expand a 16-kbyte built-in feature set (stored in a 27128 EPROM) to 64 kbytes, without hardware modification.

The ease of hardware upgrade, from 27128 to 27513, is made possible by the continuing use of the 28-pin universal-memory site. This site enables designers to mix and match their choice of ROMs, EPROMs, NVRAMs, iRAMs, and static RAMs by changing jumper considerations. The universal socket has provisions for address, data, and function pins on all these devices. Memory sizes up to 512 kbits (or 64 kbytes) are provided for with 16 address pins. Read access to the memories is simplified using the site's two-line control architecture.



Intel's 27513 EPROM incorporates a page-addressed system that puts 64 kbytes of firmware into a 16-kbyte address space without hardware modification.

The universal-memory site offers flexibility to designers. A memory board, designed with these sockets, can be used on multiple systems.

High-Volume Production

A major change for EPROMs has been their move from prototyping memories to memories used in production. Their overall cost effectiveness vs. ROM alternatives has increased as the technology has matured. Plastic-packaging technology for EPROMs promises to continue this transition.

Plastic is an advantage for high-volume production where auto-insertion equipment is used. The plastic package will not chip or crack. The windowless package also means that no covering must be applied to prevent erasure when exposed to ambient ultraviolet light.

The plastic-production EPROM (sometimes called OTP) is shipped in an unprogrammed state so that it can be programmed during the actual production run. It offers the same advantages of a windowed EPROM in production-inventory flexibility, fast production startup and reduced ROM obsolescence risk. It also comes at a reduced cost from the windowed version.

CMOS Invasion

The traditional CMOS applications in low-power or portable systems can now be designed with EPROMs. Intel's 27C64 requires less than a third of the active power of NMOS EPROMs and an order of magnitude less power when in the standby mode. The use of the CMOS EPROMs eliminates the need for complex and costly power-switching circuitry, as needed with NMOS EPROMs in these applications.

The high voltages (higher than V_{cc}) used to program EPROMs require CMOS designs to pay special attention to latch-up characteristics. Intel's CHMOS-EPROM fabrication process uses EPI processing and guard-ring structures to reduce latch-up susceptibility to high voltages and input/output noise spikes. Specifications guarantee latch-up immunity to more than 1-V margins around all power supply voltages, and currents in excess of 100 mA. ●

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With Its Paged Structure, A 512K EPROM Relaxes System Storage Constraints

BY

KURT ROBINSON

PRODUCT MARKETING ENGINEER

INTEL CORPORATION

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With its paged structure, a 512k EPROM relaxes system storage constraints

The limits imposed by the addressing range of today's 8-bit microprocessors are removed by a page-addressed EPROM that acts like four 128-kbit chips.

Inventive system designers know that advanced software features could prolong the usefulness of their 8-bit microprocessor-based systems. Though the idea is an attractive one, adding those changes to program memory would often strain the 64-kbyte addressing range of the microprocessor.

Today's 512-kbit EPROMs have the higher capacity but would consume the entire address space of the 8-bit machines. A new twist—a 512-kbit EPROM organized as four 16-kbyte pages—quadruples the program storage available to an 8-bit system. Indeed, 16-bit systems can benefit from using it.

As important, the entire chip looks to the system like a 128-kbit EPROM, which it can easily replace. Upgrading a system in this way entails little or no software modification, while building a new one with the device reduces circuit complexity and permits the use of less costly and more mature system components.

The byte-wide 27513 is a paged version of the 27512 512-kbit EPROM. Only 14 of its 16 address bits are needed to access it s full 64 kbytes, since it reserves on-chip latches for the two highest-order bits. Its 16-kbyte page size satisfies a variety of system requirements. A smaller page would entail too frequent page changes. A larger one would leave too little room for addressing RAM—which in a reprepresentative 8085-based system requires 48 kbytes of the microprocessor's 64-kbyte address space (Fig. 1). In fact, the microprocessor treats the EPROM as if it were a fourth bank of 16-kbyte RAM and selects it by writing to a 2-to-4 decoder.

Kurt Robinson, Intel Corp.

Kurt Robinson has served for five years with Intel's nonvolatile memory division, which recently moved to Folsom, Calif. Starting as an EPROM product engineer, he later joined the programmable memory marketing group as an applications engineer. Subsequently he advanced to senior product marketing engineer. His BSEE is from Cornell and his MBA from the University of Santa Clara.

The main difference

The primary operational difference between the paged 512-kbit device and linearly addressed EPROMs, including the 27512, lies in page selection. First the microprocessor sends the EPROM 2-bit page data over the lowest-order data bits, D_0 and D_1. Next it enables the memory by setting the Chip Enable ($\overline{CE}$) line low via the 2-to-4 decoder. Then it brings the Write Enable line ($\overline{WE}$) low also, thus clocking the page data into the chip's 2-bit address latch. Thereafter the newly selected 16-kbyte page can be accessed during conventional EPROM read cycles. The address inputs during page selection are in a "don't care" state.

During power-up, the EPROM automatically resets itself to page 0 as if the data 00 were being written into D_1 and D_0. A circuit for clearing the page latch remains active until V_{CC} exceeds

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4 V. Above that level, system control signals remain sufficiently stable to avoid inadvertent page selection.

The 4-V level is also low enough to prevent a low-going power-supply glitch from accidentally clearing the page latch. The worst-case voltage for V_{CC} is 4.5 V. The 4 V that clears the page also sets a 500-mV noise margin against supply undershoot, without presenting any danger of resetting the current page to 0.

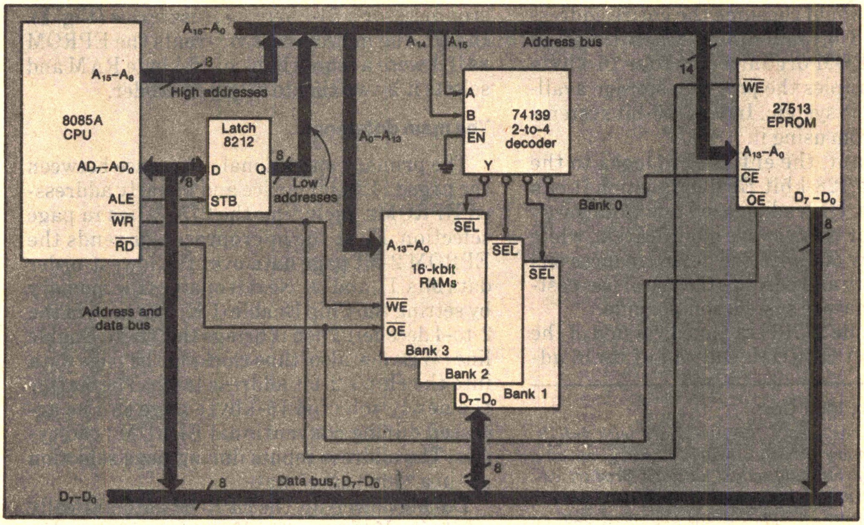
Programming the 27513 utilizes a proprietary algorithm supplied with all 12.5-V HMOS EPROMs, including the 27512. This algorithm creates 1-ms programming pulses until the byte has been verified, after which it gives a programming overpulse margin of three times the number of initial pulses. A page-select write operation is included at the start of the program and at every subsequent page boundary thereafter. (Fig. 2).

The chip's programming voltage, V_{PP}, is multiplexed with the Output Enable line ($\overline{\text{OE}}$), and the combined line ($\overline{\text{OE}}/V_{PP}$) is brought to 12.5 V for programming and to a TTL low level for verification, as in a normal read. If the chip is disabled ($\overline{\text{CE}}$ goes to a TTL high) while $\overline{\text{OE}}/V_{PP}$ is at 12.5 V, programming stops.

After each page has been programmed, it undergoes a page-selection write operation, with the write parameters tested in a manner similar to that for static RAMs. Because the chip's page latch is a write-only register, the programmed data is not read back. Instead the memory must be checked for a successful page change. Unique data must appear in at least one physical address on each page; checking that address on each page and finding the unique data confirms that the page programming was successful. Though testing of the write cycle entails reading from specific addresses, an actual write operation is independent of the address inputs.

Simple to substitute

The EPROM chip has a socket footprint almost identical to that of a 128k EPROM, meaning that it can easily be substituted for the smaller device in an existing system. However, some changes in board design are required. For example, the 512k EPROM assigns pin 27 to the Write Enable control signal, as in the JEDEC standard for byte-wide RAMs. In contrast, a



1. An 8085-based system equipped with 48 kbytes of RAM has room only for a 16-kbyte block of EPROM. But the 27513 EPROM packs four such blocks into the space previously occupied by a 128-kbit part. The EPROM resides in memory space from 0000_{16} to $3FFF_{16}$; the RAM occupies addresses 4000_{16} to $FFFF_{16}$.

128k EPROM's pin 27 is set for the program function and is tied to 5 V or V_{CC}. The origin of the Write Enable signal of the 27513 varies, since the chip encounters situations in which code and data must share the same memory map but are selected independently through dedicated selection lines or decoded status signals from the processor.

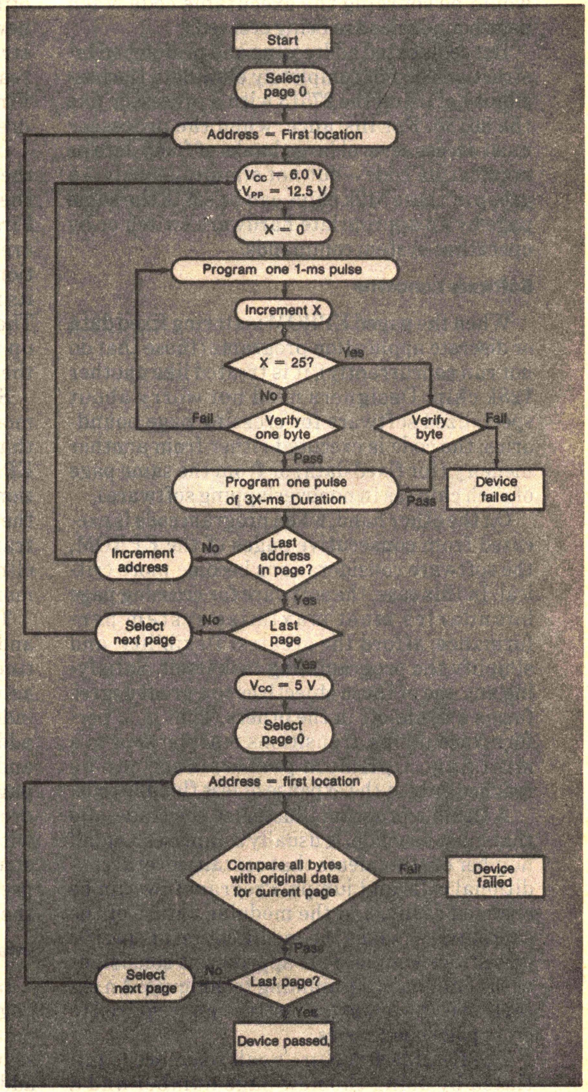
Upgrading a circuit to the 512k EPROM from one designed for a 128k EPROM is dramatically simplified if the socket has been laid out according to the so-called universal site for byte-wide memories. That arrangement brings address and control lines close to the socket, so that different configurations can be selected through jumpers. Designers can access V_{CC} (for tying the program pin of 64k and 128k EPROMs to 5 V) and $\overline{\text{WE}}$ (for byte-wide RAMs) through the universal pin 27. Thus if the socket follows this standard arrangement, the 27513 can be substituted for lower-capacity devices by changing just one jumper.

Superior 16-bit control, too

The paged EPROM can solve the limited addressing range of both 8-bit and 16-bit microprocessor-based systems. That holds true especially for firmware-intensive jobs that tax the 16-bit chip's seemingly adequate addressing range of a megabyte or more assigned to EPROM.

For example, a system tackling frequent transactions can actually eat up most of its total memory address space, which can reach about 16 Mbytes. It may use high-order address lines for specialized I/O and still have enough room for a megabyte each of RAM and EPROM. The code changes required to modify the extremely complex functions of transaction processing might cause even the megabyte of EPROM to overflow. With the 27513, code can be chopped to more manageable levels or rearranged into different memory configurations.

The 512k chip is not suited to all 16-bit systems. Indeed, executing code in the consecutive pages of the segmented chip poses a real challenge to the software programmer of, say, the 80186, which has internal segmented addresses. A high-performance processor like that also prefetches several instructions, making it difficult to know which page in the paged 512k chip


Start
Select page 0
Address = First location
V_CC = 6.0 V
V_PP = 12.5 V
X = 0
Program one 1-ms pulse
Increment X
X = 25?
Yes
No
Fail
Verify one byte
Verify byte
Fail
Pass
Program one pulse of 3X-ms Duration
Pass
Device failed
Increment address
No
Last address in page?
Yes
Select next page
No
Last page
Yes
V_CC = 5 V
Select page 0
Address = first location
Compare all bytes with original data for current page
Fail
Device failed
Pass
Select next page
No
Last page?
Yes
Device passed

2. A proprietary programming algorithm performs a page-selection write operation at the end of each page in the 27513. The algorithm generates 1-ms pulses until 8 bits have been verified; an overpulse that lasts three times longer than the number of initial pulses gives an extra program margin.

would be sourcing the executable code when page boundaries are being crossed.

But segmented addressing and prefetched instructions do not completely eliminate the possibility of using the 27513 with a processor like the 80186. For instance, when the processor must access several large banks of fixed data or application code—but not simultaneously—a group of these 512k chips can be set to the same page by an appropriate hardware switch or by operating-system commands.

Software concerns

When the paged EPROM is storing fixed data or discrete application programs (those that do not run concurrently), it is treated like another 128k chip. Designers need not worry about specialized software for crossing page boundaries; the code is executed either from another memory (for fixed data) or from the same page of each chip (as in nonoverlapping software).

On the other hand, when program code is executed from consecutive pages of the EPROM, the software considerations become more critical. In this case, the software for crossing page boundaries must maximize system performance, afford the greatest flexibility, and simplify the programming task itself. Satisfying any one of those objectives to a great degree forms a trade-off in the others. That is, if performance jumps, transitions must be kept to a minimum. Optimum performance can be reached only at the expense of less flexible code.

A flexible program illustrates the trade-offs that must be made. It usually comprises a small number of statements that contain several conditional calls and jumps. Program flow can be changed easily, and the modular nature of the subroutines makes the modification of specific operations simple. This approach is consistent with common programming techniques. An exception is the few extra instructions required to cross page boundaries.

The flexible structure's call sequence is initiated by using the new page number and a lookup table, called offset, for the subroutine address (Fig. 3a). The command Call is issued and the new page selected. However, the current page number remains unchanged. Next, the subroutine Call Address is obtained from the new-page lookup table, as indexed by the offset table. After a jump to Call Address in the new page, a return is made by jumping to the instruction RETR. The current page number is read, and the chip is reset to the previous page. Finally the program goes back to Return Address in the original page.

If the program branches to a new section of the program and there is no need to return to the previous page, a jump sequence begins. First, the offset table and the new page number are loaded, and the program moves to instruction JUMPR. The new page is now selected and its number stored in the current page location. The jump address is found in the new page lookup table, based on the offset table. A jump is then made to Jump Address in the new page.

Subroutine lookup tables are essential to this most advanced method of page selection, one that involves storing the lookup tables in the EPROM chip itself and reserving a small section of RAM for page-selection code. Although the technique demands more code for the page transitions, the overall amount is reduced by eliminating redundant instructions for common subroutines.

The look-up tables contain the page number and the offset address from which a given routine is called. Within the page containing the actual subroutine code, another lookup table, indexed by the offset value, holds the physical address of the routine. Thus the page number and offset information contained in the other pages remain constant, but the physical address of the actual subroutine can be relocated within its page, even if the code changes. The instructions for handling the page transitions are preloaded into a reserved section of RAM when the system is initialized.

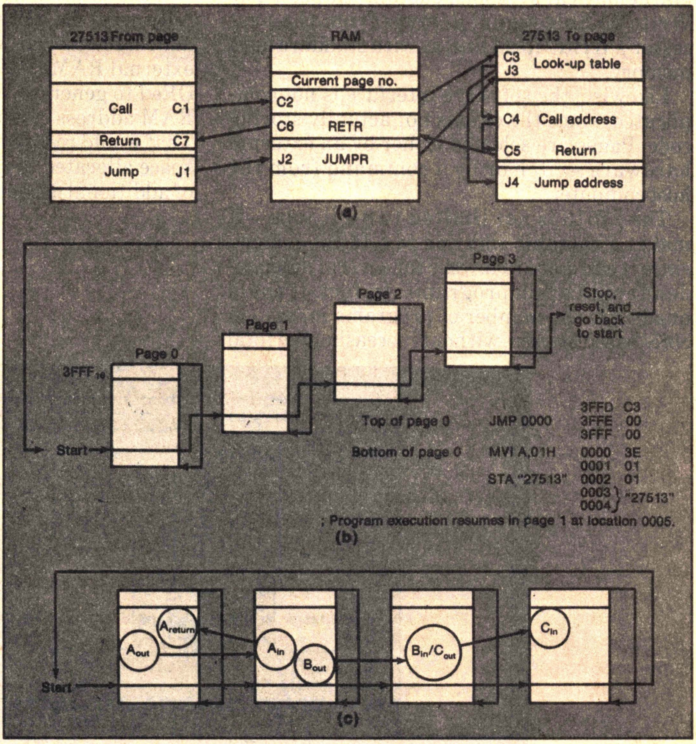
Interrupts anywhere

Interrupt routines can be executed from any page of the EPROM if the current page information is retained. After the interrupt has been serviced, the EPROM is reset to the page and address that were current when the interrupt occurred. Here again, the instructions for handling the page transitions and for calling the interrupt subroutine are preloaded into reserved RAM.

As with the flexible programming structure, designers are typically trying to make their program code more efficient by squeezing the greatest number of operations into each instruction. Those are critical concerns for systems that place program code in standard 128-kbit EPROMs, but they become much more relaxed when seen in terms of the 27513's fourfold increase in capacity. Some designers might choose straight-line programming where jumps and calls are avoided. The 27513 excels in that situation, i.e. where flexibility and compactness of code are sacrificed for an overall increase in execution speed (Fig. 3b). A true straight-line program contains no calls or jumps; the code for any repeated function is replicated each time.

Though a program that uses no branching may appear impractical, another approach that places all subroutines in the same page as the call and jump commands that refer to them is not impractical. With that technique, frequent operations are stored on every page—but only once. In either case, page transitions occur only at the end of a page or when the program is jumping back to the beginning. Small instruction sets at the start and end of each page actually shift the pages.

If the page transitions occur frequently but at relatively few points in the program, another scheme—one of moderate complexity—duplicates the set of instructions at the straight-line


27513 From page
Call C1
Return C7
Jump J1
RAM
Current page no.
C2
C6 RETR
J2 JUMPR
27513 To page
C3
J3
Look-up table
C4 Call address
C5 Return
J4 Jump address
(a)
Page 0
Page 1
Page 2
Page 3
3FFF$_{16}$
Start
Stop, reset, and go back to start
(b)
Start
A_{out}
A_{return}
A_{in}
B_{out}
B_{in}/C_{out}
C_{in}
(c)

```
Top of page 0      JMP 0000        3FFD  C3
                                   3FFE  00
                                   3FFF  00
Bottom of page 0   MVI A,01H       0000  3E
                                   0001  01
                   STA "27513"     0002  01
                                   0003 } "27513"
                                   0004 }
; Program execution resumes in page 1 at location 0005.
```

3. The program structure of the 27513 can take three forms. A flexible program requires more code for page transitions and eliminates redundant instructions for frequently called subroutines (a). The straight-line approach affords the fastest performance (b). A modification of that structure maintains the speed but adds branching code to deal with jumps between page boundaries (c).

program's page boundaries. In that manner, page transitions occur through dedicated portals of code (Fig. 3c).

Enlarging fixed storage

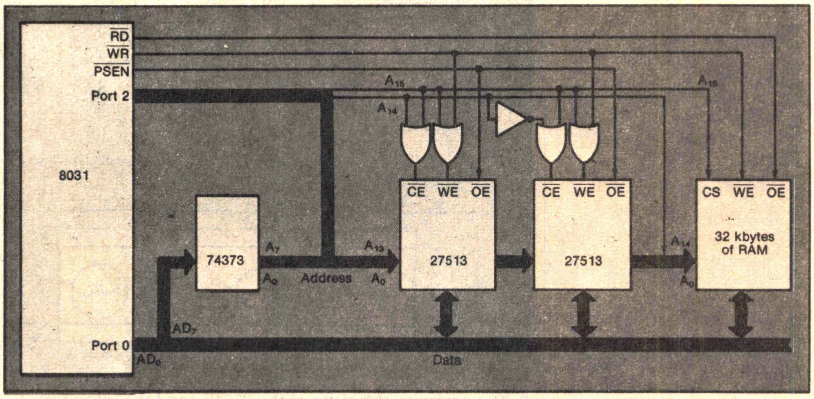
Though the 512k chip will undoubtedly be called to duty for code-expanding missions in popular 8-bit processors, its hardware interface proves equally suitable for applications requiring more storage of fixed data. Suppose that the chip is substituting for several 128-kbit EPROMs in an 8051-based dot-matrix printer. The chip itself provides enough extra storage space that designers can add three new character sets (for example, scientific marks, mathematical symbols, custom shapes). The Write Enable signal derives from the processor's Write/Read line, as with standard data memory.

Likewise, the software interface is not complicated, since the chip is not actually storing code. Pages are selected either by an external hardware switch or by a command from the host computer.

The 27513 is not limited to 8-bit jobs—it makes a valuable addition to a 16-bit system, since it can store firmware for several independent application programs. In fact, it could quadruple the number of programs in, say, an 8088-based system, without increasing the total amount of physical address space allocated to EPROM. And because the programs are not used simultaneously, the system interface is simple. Each program is selected in much the same manner as for the 8051 character-set storage application.

Even a complex chore, such as storing firmware-intensive 8031 applications, need not be a formidable task with the chip (Fig. 4). The 8031 has a special $\overline{PSEN}$(Program Store Enable) signal to enable the output of external program memory. Because data cannot be written to the standard program memory, the designer must make sure that the 27513 is subjected to the necessary page-selection write operation.

If the external data memory of the 8031 is not fully used, the EPROM chip's page latch can be addressed as if it were a lower-order bank of external RAM. The A_{15} and $\overline{WR}$ signals can be ORed to generate $\overline{WE}$; alternatively, a specific RAM address can be decoded to generate $\overline{WE}$. That would reduce the amount of RAM address space allocated to the 27513 but at the expense of additional decoding circuitry.□



4. Although some processors do not make a perfect match for the 27513, provision can be made for the EPROM's requirements. Here the memory's page latch is addressed as if the chip were a low-order bank of external RAM. ORing the processor's A_{15} and $\overline{WR}$ signals generates the 27513's $\overline{WE}$ signal; line A_{15} determines whether the RAM or EPROMs are selected. Chip-enable signals for the 27513s are decoded from lines A_{14} and A_{15}.

Use simple circuits, algorithms to program 512k-bit EPROMs

Simple interface circuitry and programming algorithms let you program the 27512 and 27513 512k-bit EPROMs rapidly and reliably.

Kurt Robinson, *Intel Corp*

Although the latest high-capacity, 512k-bit EPROMs are a logical extension of previous, smaller-capacity EPROMs, you'll need new hardware and software to program them, because the chip-select and programming lines are slightly more complex than those of the earlier devices. You can use some simple interface circuitry and programming algorithms to program 512k-bit 27512 and 27513 EPROMs rapidly and reliably.

To program the 512k-bit EPROMs, you need to use a synthesis of the techniques developed for lower-capacity EPROMs. The 512k-bit EPROMs' programming modes are identical to those of 32k-bit EPROMs, and their algorithms are compatible with those of 256k-bit EPROMs. Further, the 512k-bit EPROMs' multiplexed programming-supply/output-enable pin makes their read and program-verify modes identical, because you must bring $\overline{OE}/V_{PP}$ to a TTL low to enable data output.

Note that because of its page-addressed scheme, the 27513 has slightly different programming requirements from those of the 27512: When you program the 27513, you must select a new page at each 16k-byte boundary. **Table 1** gives the operating modes for 512k-bit EPROMs, including the 27513's page-select write mode.

TABLE 1—512k-BIT-EPROM OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	$\overline{WE}$ (27)	V_{CC} (28)	OUTPUTS (13, 15-19)	INPUT/ OUTPUTS (11, 12)
READ	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	V_{IH}	V_{CC}	HIGH Z	HIGH Z
STANDBY	V_{IH}	X	X	V_{CC}	HIGH Z	HIGH Z
INTELLIGENT PROGRAMMING	V_{IL}	V_{PP}	V_{IH}	V_{CC}	D_{IN}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	V_{IH}	V_{CC}	HIGH Z	HIGH Z
PAGE-SELECT WRITE*	V_{IL}	V_{IH}	V_{IL}		HIGH Z	PAGE D_{IN}

NOTES:
X CAN BE V_{IH} OR V_{IL}.
ADDRESSES ARE DON'T CARE FOR PAGE SELECTION.
*PAGE-ADDRESSED DEVICE (27513) ONLY

PAGE D_{IN}
PAGE-SELECTION DATA

INPUT/OUTPUT (PIN) PAGE SELECTION	D_1/O_1 (12)	D_0/O_0 (11)
SELECT PAGE 0	V_{IL}	V_{IL}
SELECT PAGE 1	V_{IL}	V_{IH}
SELECT PAGE 2	V_{IH}	V_{IL}
SELECT PAGE 3	V_{IH}	V_{IH}

As with earlier large-capacity EPROMs, the 512k-bit EPROMs' adaptive-programming algorithms require you to raise the standard 5V supply (V_{CC}) to 6V during programming and to supply a higher voltage to the programming pin. This higher supply voltage ensures

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The 512k-bit EPROMs' programming modes are identical to those of 32k-bit EPROMs.

that the EPROM will have an adequate programming margin.

Of course, most systems provide EPROM V_{CC} power through the 5V supply common to all components. Because other components are typically not guaranteed to operate at higher voltages, you'll need to implement an isolation circuit for EPROM V_{CC} during EPROM programming. Such a circuit is similar to the circuit required to switch programming-supply pins to high voltage.

The most important difference between programming 512k-bit EPROMs and programming other types of EPROMs is that the V_{PP} and $\overline{OE}$ functions are multiplexed in the 512k-bit devices. For example, the $\overline{OE}/V_{PP}$ lines bused to 512k-bit EPROMs select one of three levels: high voltage (for programming), TTL high, and TTL low (both during read operations). In contrast, V_{PP}-switching circuits for programming 256k-bit EPROMs select one of two constant, dc levels: either V_{CC} (in read modes) or high voltage (during programming). The circuit in **Fig 1** accomplishes the switching task for 512k-bit EPROMs.

Fig 2 shows 512k-bit EPROM-programming waveforms, including appropriate control signals, for the switching circuitry. Although the software that drives these signals is fairly straightforward, the sequence in

Page-addressing mandates EPROM-specific software

Page-addressing creates problems in writing the software that you burn into the 512k-bit 27513 EPROM. Fortunately, you can solve these problems by adding simple instructions to your programs. These assembler macroinstructions (macros) allow continuous code execution across page boundaries and simplify programs that exceed the 16k-byte page length.

Crossing boundaries

There are three basic applications for a page-addressed EPROM. In the simplest of these applications, a 27513 directly replaces 128k-bit EPROMs with a fourfold expansion of memory pages. The operating system treats each page as if it were a standard 128k-bit EPROM. Because the operating system uses the code contained in different pages independently, it needs no page transitions during execution of the chosen application program. Consequently, no special page-handling instructions need to be incorporated into the application code.

The other two schemes are page-handling schemes that involve executing a single program across page boundaries. The simplest boundary crossings occur when 8-bit µPs have code requirements that exceed their 64k-byte addressing ranges. A 16k-byte EPROM page allows you to transcend the 64k-byte boundary, while still leaving room for other types of memory.

Fourfold increase

Because the 27513 has four times the capacity of a standard 128k-bit EPROM, you can use a different program structure with the 27513. The abundant code space allows you to unfold the program from a typical structured program to a purely straight-line organization. With this approach, you duplicate subroutines everywhere they are needed in the main program flow, eliminating all jumps and calls—especially those from one page to another. The resulting straight-line flow offers the highest performance. Code for handling page transitions occurs only at page boundaries, and the program loops back to the beginning when it reaches the end of the fourth page. A generalized 27513 structure for the page-handling code is

- Program execution begins a few locations up from the starting address of the page.
- The last instruction in each page is a jump to the beginning of that page.
- The code at the beginning of the page instructs the processor to select a new page.
- The next instruction executes from the next physical address (but actually from the next page). This address is the same physical address as the starting location in the previous page.

The third paging method pro-

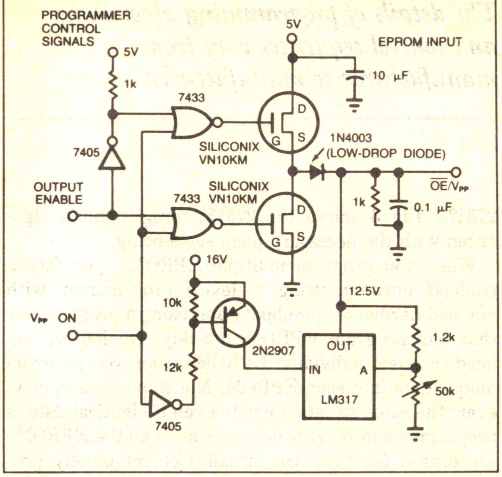

Fig 1—This level-selecting circuit provides *the fast, clean switching you need to program and verify 512k-bit EPROMs.*

which the signals are applied depends on the programming algorithm the manufacturer specifies.

For example, Intel's programming algorithm initially tracks the number of 1-msec pulses required for the first successful verification. The algorithm then requires that you multiply the interval by 3 to yield a single overpulse. This overpulse boosts the memory cells in that byte to the highest programming margin the chip can withstand without degradation.

Except for some extra steps that handle page transitions, the programming algorithm for the page-addressed EPROM (the 27513) is identical to the algorithm for the continuously addressed EPROM (the

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duces the most flexible structure, but its complexity creates the greatest need for standard assembler macros for generating the page-changing code. This approach is most consistent with standard structured-programming techniques. Characteristics of structured programs include modularized routines, numerous jumps and calls, and ready servicing of interrupts. You'll need software tools to generate special code whenever a jump or call involves crossing page boundaries. The tools also must relocate the physical addresses and associated memory pages when the program is modified.

In this approach, the foundation for structured programs consists of a look-up table, three subroutines, and a register or stack location for tracking the current page. The look-up table holds the page number and the physical address (within the selected page) for the routine being called or jumped to. The three subroutines, duplicated in each page (or loaded into RAM), perform jumps, calls, and returns from calls. Generalized descriptions for these subroutines are

- *Call*—You call this routine instead of calling a subroutine directly. The routine requires a look-up-table pointer associated with the subroutine you want to jump to. Because the program must return to the original page, *Call* stores the current page in a current-page register or RAM location. *Call* gets the page number and relative physical address of the called routine and issues commands to change to the new page. *Call*'s remaining instructions are executed from a new page (which implies that *Call* occupies identical physical addresses in each page). Finally, *Call* jumps to the physical address of the called routine.
- *Jump* is exactly like *Call* except that you unconditionally jump to it instead of calling it. Before jumping to the routine's physical address within the new page, *Jump* updates the current page register (or stack location) to the page number of the new page, which you just selected.
- *Return*—You jump to this routine instead of simply executing a return instruction to return from a subroutine call. *Return* obtains the previous page number from the current-page register. (Note that the current-page information was not changed when the *Call* routine executed.) *Return* issues instructions to reselect the previous page. Finally, because you called the *Call* routine initially, *Return* executes a standard return command and resets the program counter to the proper return address.

The details of programming algorithms and control sequences vary from manufacturer to manufacturer.

27512). **Fig 3** shows the 27513's programming algorithm with the necessary page sequencing.

When you program multiple EPROMs, you face a tradeoff between using a device programmer with minimal hardware complexity and using a programmer that will program EPROMs quickly. Obviously, you need to select individual EPROMs when you program unique data into each EPROM. Not so obviously, however, the same situation exists even if identical data is programmed into every device. Unless all the EPROMs are erased (as they are initially) or completely programmed (as they are in the end), they will produce different data during the intermediate stages of adaptive-programming processes. When you read from more than one device at the intermediate stages of adaptive programming, the partially programmed EPROMs will contend for the data bus.

Separate $\overline{\text{CE}}$s reduce complexity

Because of the 2-line output control employed on the 512k-bit EPROMs, you have the choice of isolating the EPROMs with either separate $\overline{\text{CE}}$ or separate $\overline{\text{OE}}/\text{V}_{\text{PP}}$ control lines. It's better to have separate $\overline{\text{CE}}$s, because they eliminate additional complexity in the circuitry needed to switch between the programming-supply voltage (V_{PP}) and output enable ($\overline{\text{OE}}$) functions. Sepa-

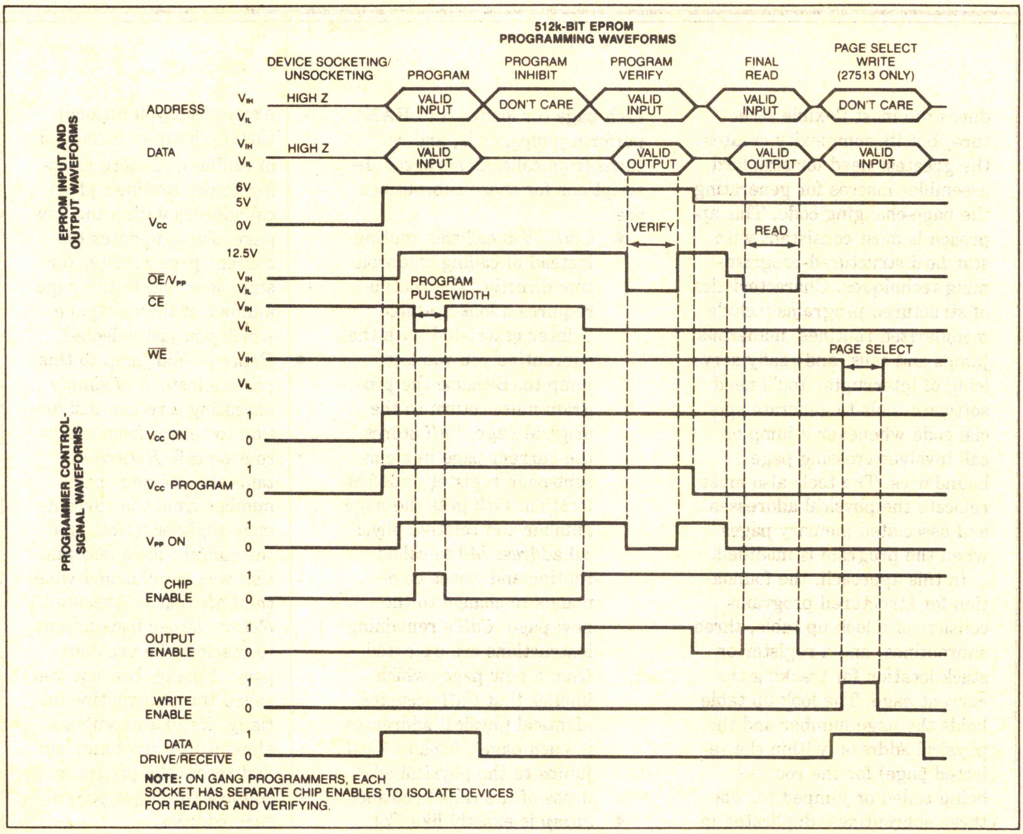
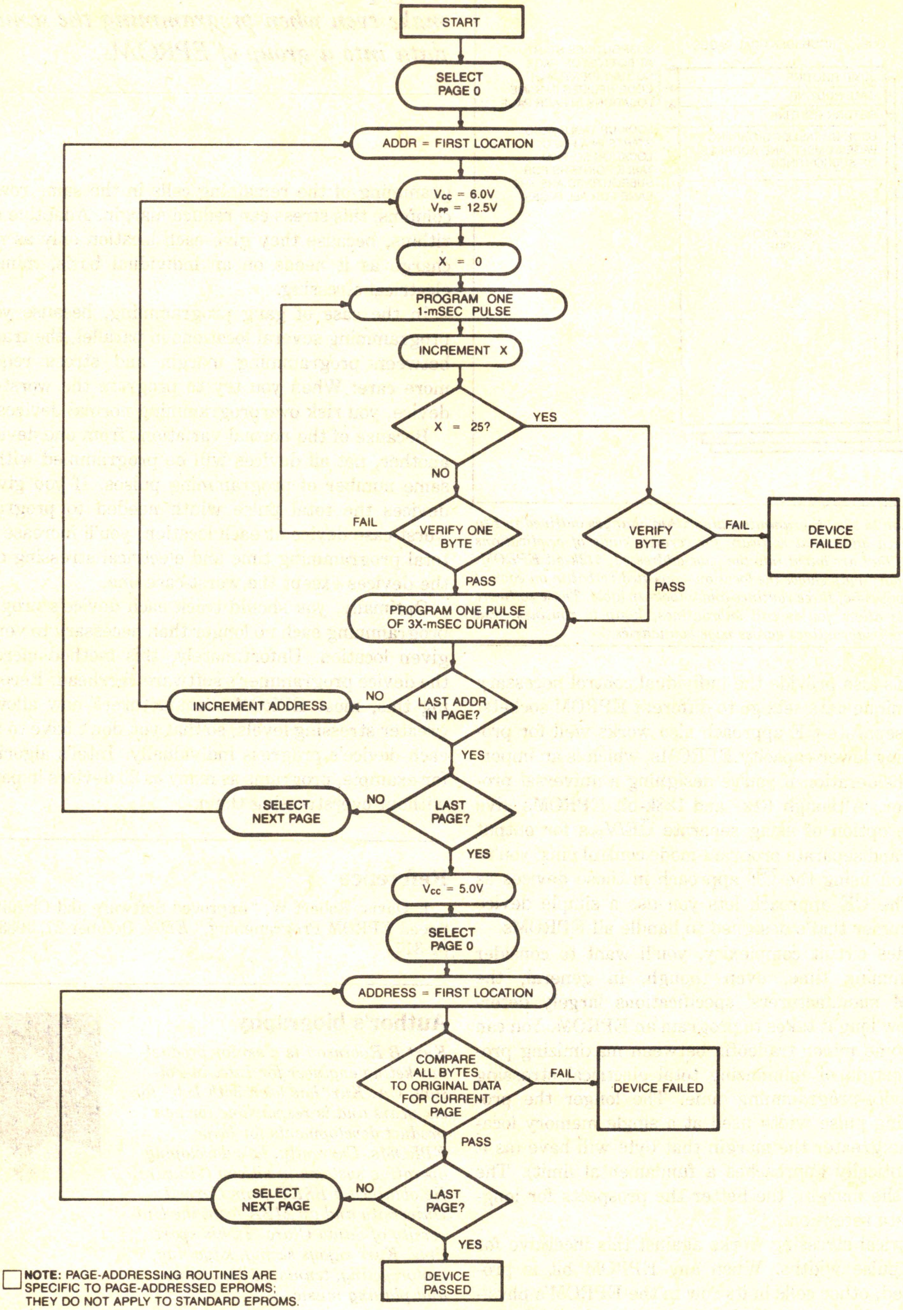
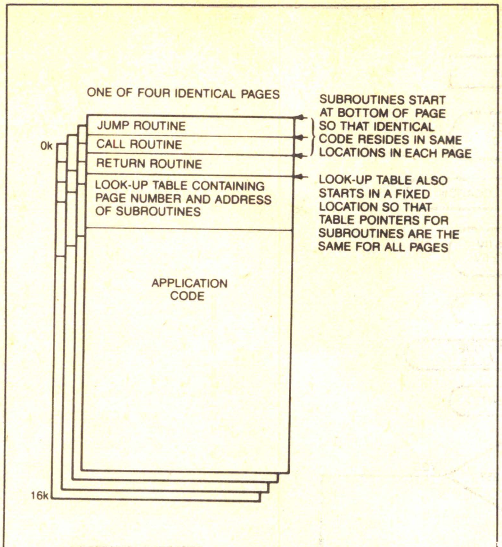

512k-BIT EPROM PROGRAMMING WAVEFORMS
DEVICE SOCKETING/ UNSOCKETING
PROGRAM
PROGRAM INHIBIT
PROGRAM VERIFY
FINAL READ
PAGE SELECT WRITE (27513 ONLY)
EPROM INPUT AND OUTPUT WAVEFORMS
ADDRESS
DATA
VIH
VIL
HIGH Z
VALID INPUT
DON'T CARE
VALID INPUT
VALID INPUT
DON'T CARE
HIGH Z
VALID INPUT
VALID OUTPUT
VALID OUTPUT
VALID INPUT
6V
5V
0V
VCC
12.5V
VERIFY
READ
OE/VPP
CE
PROGRAM PULSEWIDTH
WE
PAGE SELECT
PROGRAMMER CONTROL-SIGNAL WAVEFORMS
VCC ON
VCC PROGRAM
VPP ON
CHIP ENABLE
OUTPUT ENABLE
WRITE ENABLE
DATA DRIVE/RECEIVE
1
0
NOTE: ON GANG PROGRAMMERS, EACH SOCKET HAS SEPARATE CHIP ENABLES TO ISOLATE DEVICES FOR READING AND VERIFYING.

***Fig 2—Although the signals for programming 512k-bit** EPROMs are fairly straightforward, the sequence in which you apply the signals depends on the programming algorithm the manufacturer specifies. (These waveforms apply to Intel chips.)*


START
SELECT PAGE 0
ADDR = FIRST LOCATION
V_{CC} = 6.0V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1-mSEC PULSE
INCREMENT X
X = 25?
YES
NO
FAIL
VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-mSEC DURATION
INCREMENT ADDRESS
NO
LAST ADDR IN PAGE?
YES
SELECT NEXT PAGE
NO
LAST PAGE?
YES
V_{CC} = 5.0V
SELECT PAGE 0
ADDRESS = FIRST LOCATION
COMPARE ALL BYTES TO ORIGINAL DATA FOR CURRENT PAGE
FAIL
DEVICE FAILED
PASS
SELECT NEXT PAGE
NO
LAST PAGE?
YES
DEVICE PASSED

☐ **NOTE:** PAGE-ADDRESSING ROUTINES ARE SPECIFIC TO PAGE-ADDRESSED EPROMS; THEY DO NOT APPLY TO STANDARD EPROMS.

***Fig 3—This flowchart illustrates the additions** you must make to the programming algorithm to accommodate the page-addressed, 512k-bit EPROM (the 27513). The shaded steps of the flowchart select a new page when appropriate.*


ONE OF FOUR IDENTICAL PAGES
0k
JUMP ROUTINE
CALL ROUTINE
RETURN ROUTINE
LOOK-UP TABLE CONTAINING PAGE NUMBER AND ADDRESS OF SUBROUTINES
APPLICATION CODE
16k
SUBROUTINES START AT BOTTOM OF PAGE SO THAT IDENTICAL CODE RESIDES IN SAME LOCATIONS IN EACH PAGE
LOOK-UP TABLE ALSO STARTS IN A FIXED LOCATION SO THAT TABLE POINTERS FOR SUBROUTINES ARE THE SAME FOR ALL PAGES

***In addition to the programming-algorithm changes** outlined in **Fig** 3, you need additional software for certain kinds of applications programs that are burnt into the page-addressed, 512k-bit EPROM. This memory map shows the location—repeated verbatim on each of the four pages—of three routines and a look-up table. These software constructs allow you to call subroutines, jump to routines, and return from subroutines across page boundaries.*

rate $\overline{\text{CE}}$s also provide the individual control necessary when unique data sets go to different EPROM sockets.

The separate-$\overline{\text{CE}}$ approach also works well for programming lower-capacity EPROMs, which is an important consideration if you're designing a universal programmer. Although 64k- and 128k-bit EPROMs give you the option of using separate $\overline{\text{OE}}/V_{PP}$s for output control and separate program-mode control pins, you're better off using the $\overline{\text{CE}}$ approach in those devices as well. The $\overline{\text{CE}}$ approach lets you use a simple device programmer that's designed to handle all EPROMs.

Besides circuit complexity, you'll want to consider programming time, even though, in general, the EPROM manufacturers' specifications largely determine how long it takes to program an EPROM. You can make some minor tradeoffs between maximizing program margin or minimizing total electrical stressing and device-programming time. The longer the programming pulse width used at a single memory location, the greater the margin that byte will have (as it asymptotically approaches a fundamental limit). The higher the margin, the better the prospects for long-term data retention.

Electrical stressing works against this incentive for longer pulse widths. When any EPROM bit is programmed, other cells in its row in the EPROM's physical array of memory cells are also subjected to high gate voltage. Likewise, cells in the same column are subjected to high drain voltage. The first cells to be programmed are subsequently stressed during the programming of the remaining cells in the same rows or columns; this stress can reduce margin. Adaptive algorithms, because they give each location only as much charge as it needs on an individual basis, minimize electrical stressing.

Gang programmers have extra decisions to make even when programming the same data into a group of EPROMs.

In the case of gang programming, because you're programming several locations in parallel, the tradeoff between programming margin and stress requires more care: When you try to program the worst-case device, you risk overprogramming normal devices.

Because of the normal variations from one device to another, not all devices will be programmed with the same number of programming pulses. If you give all devices the total pulse width needed to program a worst-case device at each location, you'll increase both total programming time and electrical stressing on all the devices except the worst-case one.

Optimally, you should track each device's progress, programming each no longer than necessary to verify a given location. Unfortunately, this method increases the device programmer's software overhead. Recognizing this, most EPROM manufacturers now allow for greater stressing levels, so that you don't have to track each device's progress individually. Intel's algorithm, for example, programs as many as 20 devices in parallel without overstressing them. **EDN**

Reference

1. Davis, Robert W, "Improved Software and Circuits Speed EPROM Programming," *EDN*, October 27, 1983, pg 315.

Author's biography

Kurt B Robinson is a senior product-marketing engineer for Intel in Folsom, CA. Kurt has been with Intel for six years and is responsible for new product developments for large EPROMs. Currently, he's developing operating systems in silicon (siliware). He obtained a BSEE from Cornell University and an MBA from the University of Santa Clara. In his spare time, Kurt enjoys skiing, kayaking, motorcycling, tennis, sailboarding, and playing music.

Marriage Of CMOS And PLCC Sparking Rapid Change In Mounting Memories

By Alan Hanson

The surge in circuit complexity over the past year or two has pushed the standard DIP size beyond workable dimensions, and rendered it obsolete where high lead count is required.

Meanwhile, the semiconductor industry's shift to CMOS processing for memories, as well as other ICs, is helping usher in the era of surface-mountable packages. Chief among these packages for memories is the plastic-leaded chip carrier (PLCC).

The technology for surface mountables and CMOS processing emerged from shaky beginnings. Although surface-mount packaging has been available for nearly two decades, its potential has just begun to be realized.

Several technical problems hampered its early acceptance: the need for automated factory equipment; prohibitively high packaging costs; and the lack of necessary construction tools.

As of 1984, only 6 percent of all components used in the United States were surface-mount types. Industry analysts predict, however, that with the increase in packaging options, the availability of development tools and the rising demand for surface-mountable devices, more than 25 percent of components will be surface mounted by 1988. And an estimated 128 million of the 600 million PLCCs manufactured in 1988 are expected to be memories.

CMOS has had to fight a similar battle. Prohibitively high cost, inherently low performance (metal gates) and lack of a complete lineup of products necessary to provide low-power system solutions were the chief reasons for CMOS' slow start. But, these problems have now been overcome and the number of products combining CMOS technology and surface-mount packages is accelerating rapidly.

PLCC Inroads

The decision to move from insertion (through-hole) to surface-mount technology is not an easy one. The available options are somewhat confusing:

- Are space constraints a problem?
- Is more functionality required?
- Will surface mounting make a more competitive product?
- Will manufacturing-cost savings be realized?
- Is the proper assembly equipment already available?
- Do components meet JEDEC standards?
- Will socketing be required?

The drive for smaller, more functional and more competitive products is forcing many engineers to scale down existing designs; to strive for VLSI solutions; and to use PLCC packages and other surface-mount packaging options, which can reduce board size dramatically.

Decisions as to which surface-mount option to use are usually based on board-size restrictions. In general, PLCCs minimize the area footprint on a board for lead counts ranging from 28 to 124.

One example of the space-saving ability of a PLCC package is Intel's new 32-lead PLCC package which it is developing for its 64k and 256k CHMOS EPROMS. The PLCC measures 0.45 × 0.55 inch, whereas the 28-pin DIP that would normally be used here measures 1.4 × 0.6 inch. The reduction in area footprint is 70 percent.

The contact area for chip leads can be closer for a PLCC device because the mounting holes mandatory for insertion devices are eliminated. Surface mounting also allows components to be placed and soldered on both sides of a pc board where through-hole mounting is not employed. Depending on the complexity and type of components required in the board layout, a 35- to 60-percent reduction in board size is possible.

To minimize total chip requirements, manufacturers of products such as EPROMs are incorporating an address latch on the address and data pins to allow direct interface with a microcontroller or microprocessor. This eliminates the need for an external latch, as well as reducing board size.

Surface-mount elements can also reduce component weight as much as 75 percent.

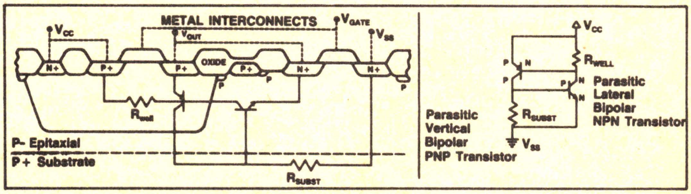
Lightweight PLCC packages tend to be ideal for high-vibration industrial and automotive applications, as well as for portable applications.

Surface mounting requires a substantial investment in capital equipment. New techniques for soldering components to boards (i.e., vapor phase or wave soldering) must be considered and automated machinery such as pick-and-place assemblers must be employed—new pick-and-place machinery employing vacuum pickup has been developed to handle the wide array of different sized packages available for surface mounting.

Today, many different machines are available. Their processing capacity ranges anywhere from 500 to 500,000 devices per hour. (Surface-mounting technology is even used in small-volume, custom facilities, such as for making portable medical equipment, where the devices are manually soldered to boards.)

The benefits of factory-automated assembly are numerous. Less floor space is required. Since raw materials are contained in smaller packages, storage space is diminished. Lighter-weight components reduce shipping and handling expenses. Space-saving benefits can be achieved in the layout of the assembly equipment itself. Some manufacturers have been able to reduce the required factory floor space by as much as 25 percent. Other cost savings include a reduced labor force, the ability to maintain a no-shutdown assembly, improved reliability and reduction of inspection and rework.

These benefits must outweigh, of course, the costs of automating the factory, as well as the cost of restructuring and retraining.



This CMOS EPROM combines both n-channel and p-channel transistors onto a p-type epitaxial substrate to reduce greatly current requirements as compared with an NMOS counterpart.

Electronic Engineering Times — Monday, September 30, 1985

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Order Number: 295007-001

When choosing between packaging alternatives, consideration should always be given to industry-wide standardization to avoid unnecessary design mismatching and insure upgradeability. For example, the 32-lead PLCC package was chosen for high-density EPROMs because as much as 512 kbits of address space is easily contained within this package size. Furthermore, PLCC devices with as many as 124 J-type leads have been registered with JEDEC, the standard-setting body for the industry.

A J-type lead extends out of the four sides of a PLCC package and is tucked under the body into small pockets. It was chosen as the industry-standard lead type as opposed to gull wing for several reasons. A minimum-area footprint is best achieved with a J-lead—gull wings extend horizontally out from the body of the package, increasing the required area footprint of the component. Because of their extended leads, gull-wing devices are also at greater risk to damage during assembly or transporting.

J-type leads are also more aptly suited for socketing, which may be particularly important for memory components subject to periodic updates. The J-lead PLCC does, however, have its drawbacks, the most noticeable being the difficulty encountered in inspecting solder joints.

The next step for design engineers who have decided to use PLCC components is to investigate the available process-technology alternatives.

CMOS And PLCC Packaging

Applications ideal for both CMOS parts and PLCC packages lie in low-power portable products in space-constrained environments. Examples can easily be found in the automotive, telecommunication and portable-instrument markets.

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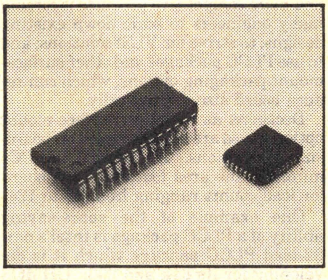
CMOS' greatest strength lies in its low-power properties. For example, Intel's 27C64 CHMOS EPROM, which combines both n-channel and p-channel transistors onto a p-type epitaxial substrate, maintains a maximum operating current of 10 mA, standby current of 100 mA and offers 200-ns total access time. Its NMOS counterpart would require six times more active current, 200 times greater standby current and would offer no improvement to total access time.



Both the 28-pin DIP and 32-lead PLCC can hold anywhere from 32k to 512k EPROMs. But, the carrier is roughly a third smaller.

PLCC packages are essential in portable applications because of their space-saving and lightweight features. Minimizing component packaging size, however, achieves little if used in conjunction with bulky power supplies, batteries and cooling devices. Because of its low-power requirements, CMOS helps minimize the need for large power supplies and cooling devices, as well as enhancing PLCC-device reliability.

Because of their reduced package size and plastic construction, PLCCs are poor heat conductors compared with the larger DIP packages. So heat-related breakdowns are more likely—heat dissipation is generally a function of package material, length and construction of leads, package surface area and, of course, the power consumed by the devices.

In improving the overall integrity and reliability of surface-mountable components, methods must be employed to deal with thermal-management problems. The chief way to accomplish this for PLCCs is to reduce the resistance to heat flow from the active junction to the atmosphere.

Thermal resistance ranges from about 40C° per watt for a 68-lead PLCC package to more than 100C° per watt for the 20-lead device. Copper alloy leads, modified substrate materials, and special heat sinks are being used at the package and board levels to maximize heat conduction.

In VLSI applications where increased device functionality is required, thermal management becomes an acute problem. As functionality increases, power demands likewise increase. The resulting higher operating temperatures may result in severe degradation to device operation and performance.

CMOS offers a solution to thermal-management problems. For example, the 27C64, with a maximum operating current of 10 mA, generates 50 mW of heat—a sixth the amount of its NMOS counterpart.

Depending on the particular design and application, special heat-sink designs and/or cooling fans can be reduced or even eliminated with CMOS parts.

CMOS is particularly valuable in extended-temperature environments, such as automotive engine-control applications where operating temperatures range from −40°C to 80°C and as high as 125°C. In these applications, CMOS may be the only way to provide reliable device operation.

CMOS also brings to a PLCC package wider V_{CC} tolerances and HMOS compatability.

Support tools such as testing, soldering and programming equipment have also become available for CMOS-based surface-mount designs. **EET**

E^2PROMs (In-Circuit Programmable Writable Memories)

5

2817A
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- **5 Volt Only Operation**
- **On-Chip Latches for Direct Microprocessor Interface**
- **Automatic Byte-Erase-before-Write**
- **Self Timed Byte Write**
- **Fast Read Access Time:**
  — 2817A-1 200 ns max
- **Write Protect Circuit to Preserve Data on Power Up and Power Down**
- **10,000 Erase/Write Cycles per Byte**
- **Reliable Intel HMOS*-E FLOTOX Cell Design Technology**
- **READY/$\overline{\text{BUSY}}$ Line for End-of-Write Signal**
- **10 Year Data Retention For Each Write**
- **Available in 28-Pin, Plastic and Cerdip Packages, and 32-Lead PLCC**
  (See Packaging Spec, Order #231369.)

The Intel 2817A is a 16,384 bit Electrically Erasable Programmable Read Only Memory. In addition, it offers a high degree of integrated functionality which enables in-circuit byte writes to be performed with minimal hardware and software overhead. The Intel 2817A is a product of Intel's advanced E²PROM technology and uses the powerful HMOS*-E process for reliable, non-volatile data storage.

*HMOS is a patented process of Intel Corporation.

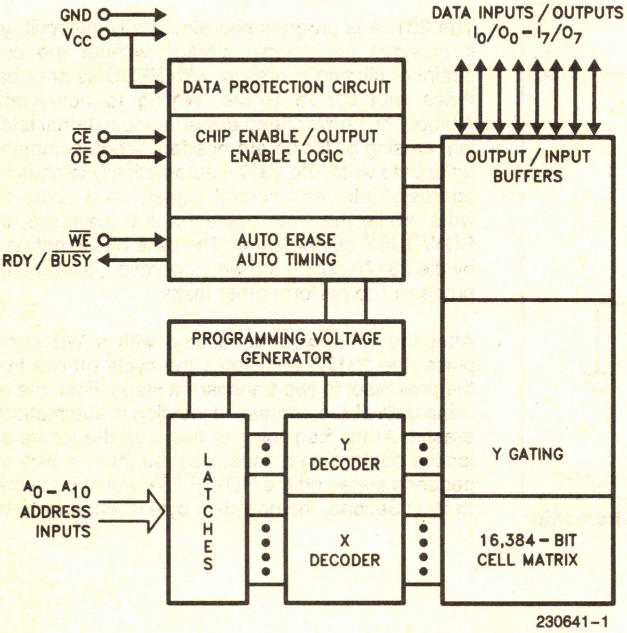
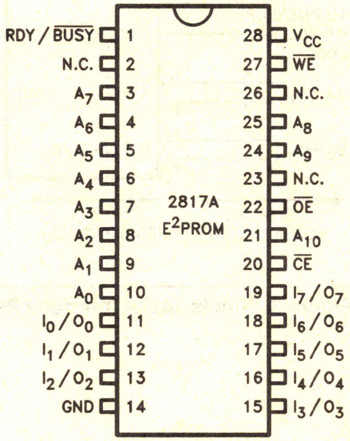

GND
VCC
DATA INPUTS / OUTPUTS
I0/O0 – I7/O7
DATA PROTECTION CIRCUIT
CE
OE
CHIP ENABLE / OUTPUT ENABLE LOGIC
OUTPUT / INPUT BUFFERS
WE
RDY / BUSY
AUTO ERASE AUTO TIMING
PROGRAMMING VOLTAGE GENERATOR
LATCHES
Y DECODER
Y GATING
A0 – A10 ADDRESS INPUTS
X DECODER
16,384 – BIT CELL MATRIX
230641-1

Figure 1. 2817A Functional Block Diagram

PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
O_0–O_7	DATA OUTPUTS
I_0–I_7	DATA INPUTS
RDY/$\overline{\text{BUSY}}$	DEVICE READY/BUSY
N.C.	NO CONNECT
$\overline{\text{WE}}$	WRITE ENABLE


RDY / BUSY 1
N.C. 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I0/O0 11
I1/O1 12
I2/O2 13
GND 14
28 VCC
27 WE
26 N.C.
25 A8
24 A9
23 N.C.
22 OE
21 A10
20 CE
19 I7/O7
18 I6/O6
17 I5/O5
16 I4/O4
15 I3/O3
2817A
E²PROM

230641-2

Figure 2. 2817A Pin Configuration

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. **November 1986**

© Intel Corporation, 1986

Order Number: 230641-005

The Intel 2817A incorporates all the interfacing hardware logic and the secondary voltage supply required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the 2817A signals 'Ready'. With a transparent erase before write, the user benefits by saving an erase command which contributes to efficient usage of system processing time. On chip latching further enhances system performance.

The Intel 2817A's exceptionally fast read access time makes it compatible with high performance microprocessor applications. It uses Intel's proven 2-line control architecture which eliminates bus contention in a system environment. Combining these features with the 2817A's open drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E^2 memory—available to the designer today.

The density, and level of integrated control, makes the Intel 2817A suitable for users requiring low hardware overhead, high system performance, minimal board space and design ease. Designing with, and using the 2817A, is extremely cost effective since all of the required programming voltage and interfacing hardware required for other E^2PROM devices has been eliminated. See Figures 1, 2, and 3 for the Intel 2817A's block diagram, pinout, and simple interface requirements.

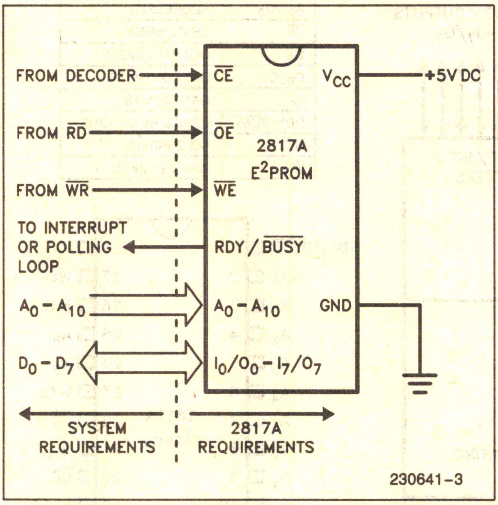


Figure 3. Simple 2817A Interface Requirements

DEVICE OPERATION

The Intel 2817A has 3 basic modes of user operation which are detailed in Table 1. All modes are designed to enhance the 2817A's functionality to the user and provide total Intel E^2PROM microprocessor compatibility.

Table 1. $V_{CC} = +5V$

Pin Mode	$\overline{\text{CE}}$ (20)	$\overline{\text{OE}}$ (22)	$\overline{\text{WE}}$ (27)	$I_0/O_0-I_7/O_7$ (11–13, 15–19)	RDY/$\overline{\text{BUSY}}$ (1)
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	High Z	Hi-Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}

NOTE:
RDY/$\overline{\text{BUSY}}$ is an open-drain output with $I_{OL} = 2.1$ ma.

The Write Mode

The 2817A is programmed electrically in-circuit, yet it provides non-volatile storage without the constraint of ultraviolet erasure with EPROMs or of batteries with CMOS RAMs. Writing to non-volatile memory has never been easier as no external latching, erasing or timing are needed. When commanded to byte write, the 2817A automatically latches the address, data, and control signals, and starts the write. While the write operation is in progress, the RDY/$\overline{\text{BUSY}}$ output is low. The data bus is not used by the 2817A during the write operation, allowing the processor to perform other tasks.

After the write cycle is initiated with a $\overline{\text{WE}}$ strobe pulse, the 2817A completes the cycle off-line from the processor in two transparent steps. First, the existing data at the addressed location is automatically erased. At the beginning of this step the inputs are locked out, the data lines are brought to a high impedance state and the RDY/$\overline{\text{BUSY}}$ signal is lowered to V_{OL}. Second, the new data byte is written into the device. At the end of this process, the 2817A raises its RDY/$\overline{\text{BUSY}}$ signal to V_{OH} to notify the processor that the write cycle is complete and that the device is ready for read or write access.

The write endurance is 10^4 cycles, that is, a minimum of 10,000 write cycles can be reliably performed on each byte.

The Read Mode

One aspect of the 2817A's high performance is its fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMs and static RAMs. The Intel 2817A can be selected using decoded system address lines to $\overline{\text{CE}}$ and then the device can be read, within the device selection time, using the processor's $\overline{\text{RD}}$ signal connected to $\overline{\text{OE}}$.

Read retention for data written into the 2817A is greater than 10 years.

The Standby Mode

The 2817A has a standby mode which reduces the maximum active current from 100 mA to 45 mA. This offers the user power supply cost benefits when designing a system with Intel 2817A's. This mode occurs when the device is deselected ($\overline{\text{CE}} = V_{IH}$). The data pins are put into the high impedance state regardless of the signals applied to $\overline{\text{OE}}$ and $\overline{\text{WE}}$ concurrent with the reading and writing of other devices.

On-Chip Data Protection on V_{CC} Power Up and Power Down

An erase/write of a byte in the 2817A is accomplished with input signals $\overline{\text{CE}}$, $\overline{\text{WE}} = V_{IL}$. During system ($V_{CC}$) power up and power down, this condition may be present as V_{CC} ramps up to or down from its steady state value of 5 volts. To prevent the possibility of an inadvertent byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if V_{CC} falls below 3.5 volts (V_{LKO}).

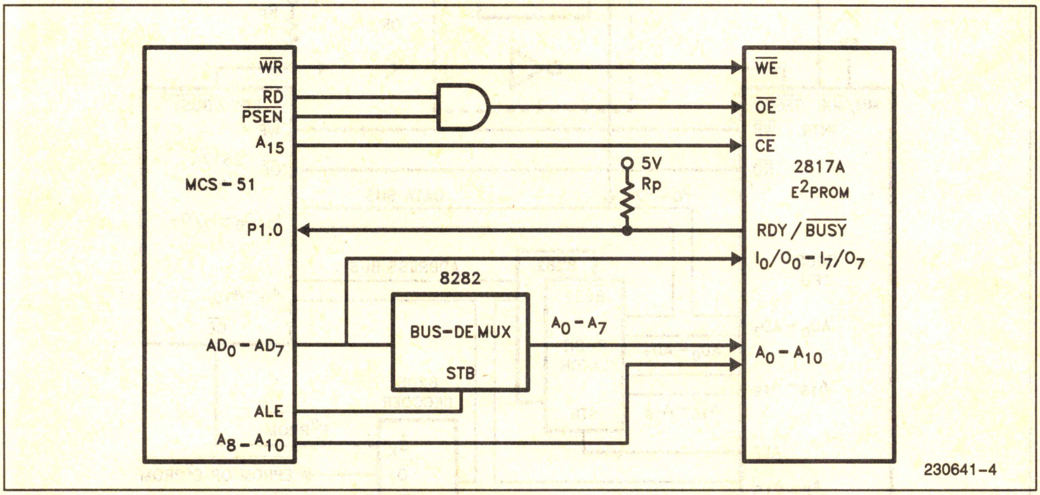


Figure 4. 2817A E²PROM as Remotely-Alterable Non-Volatile Program Code Memory in an MCS®-51 System

System Implementation

The 2817A is compatible with Intel MCS®-51 Microcomputer and the iAPX 86/88, 186/188, and 286 microprocessor families. The 2817A requires no interface circuitry. Figure 4 shows an example of the 2817A used as program storage memory in an MCS-51 single-chip microcomputer system. The MCS-51 program code is modified or upgraded remotely without having to remove the E²PROM from the system.

The Intel 8282 8-bit latch shown in Figure 4 is used to de-multiplex addresses A0–A7. (The latch is typically required in an MCS-51 system.) The ANDing of signals PSEN and RD allows both program code and external data for the MCS-51 to be fetched/read from the 2817A E²PROM. The MCS-51 determines when a given write cycle has been completed by reading port bit P1.0 which is connected to the 2817A's RDY/BUSY output.

Application Note AP-158 shows a complete schematic diagram of an 8088-based system design example. Included in AP-158 are various hardware design options for different applications and a number of 8088 code software routines for remote down-

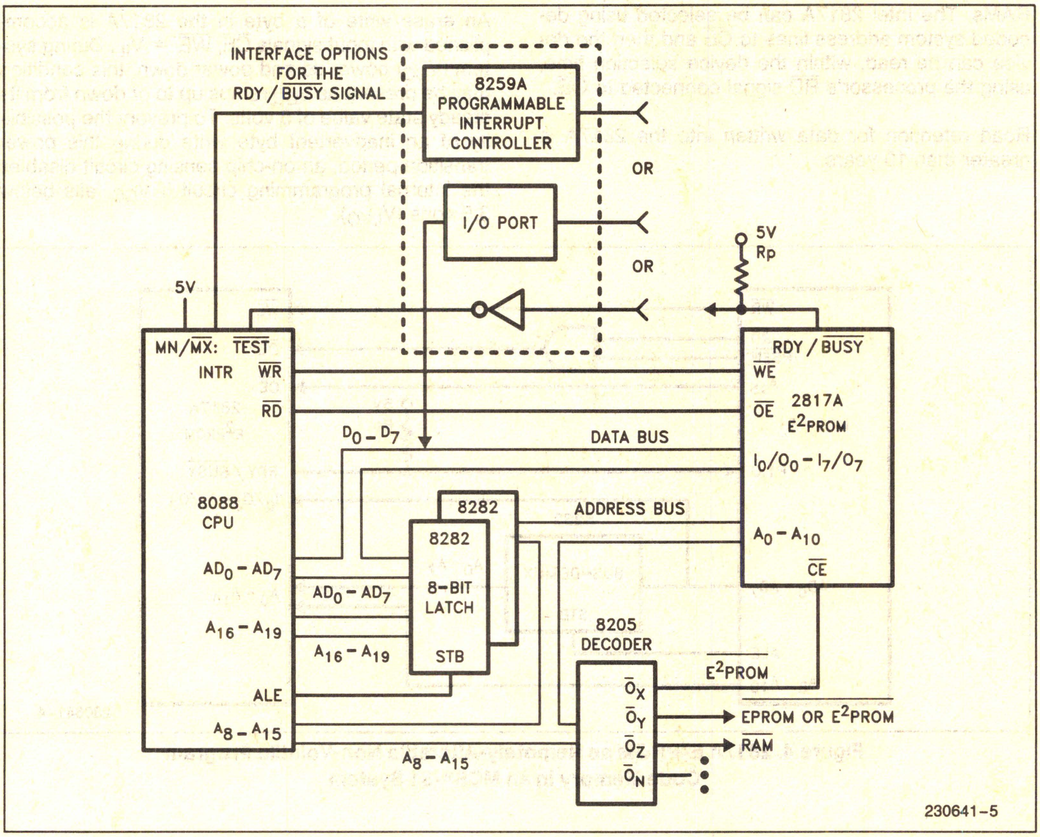

INTERFACE OPTIONS
FOR THE
RDY / BUSY SIGNAL
8259A
PROGRAMMABLE
INTERRUPT
CONTROLLER
OR
I/O PORT
OR
5V
Rp
5V
MN/MX: TEST
INTR
WR
RD
8088
CPU
AD0 – AD7
A16 – A19
ALE
A8 – A15
D0 – D7
DATA BUS
8282
8282
8-BIT
LATCH
STB
AD0 – AD7
A16 – A19
ADDRESS BUS
RDY / BUSY
WE
OE
2817A
E2PROM
I0/O0 – I7/O7
A0 – A10
CE
8205
DECODER
OX
OY
OZ
ON
E2PROM
EPROM OR E2PROM
RAM
A8 – A15
230641-5

Figure 5. 2817A/8088 Interface Example

loading applications, and for using the 8259A Programmable Interrupt Controller and the 8251A Programmable Communications Interface.

Interfacing to the Intel 8088 is similar to the MCS-51 interface. The difference lies in the use of the 8259A (Programmable Interrupt Controller). The Ready line can be connected to any of the interrupt request ins in order to interrupt the processor. (See Figure 5.) Alternatively, it can be polled through an I/O port or connected through an inverter to $\overline{\text{TEST}}$ on the Intel 8088.

Using RDY/$\overline{\text{BUSY}}$

The RDY/$\overline{\text{BUSY}}$ pin is an open-drain output which allows two or more RDY/$\overline{\text{BUSY}}$ signals to be OR-tied together. To calculate the value of the pullup resistor for the RDY/$\overline{\text{BUSY}}$ output, the following formula can be used:

$$R_P = \frac{4.6\text{V}}{2.1\text{ ma} - I_{IL}}$$

where I_{IL} = the total V_{IL} input current of all devices connected to the RDY/$\overline{\text{BUSY}}$ line.

A typical pull-up resistor value for the RDY/$\overline{\text{BUSY}}$ output is 3.0KΩ, assuming that the input sink current (I_{IL}) of the input(s) being driven is less than 0.5 ma.

Applications

The Intel 2817A is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a character-oriented or graphics terminal is an example where user defined functions, such as protocol, color, screen attributes and character fonts can be keyed in by the user. Calibration constants can be stored in the 2817A with a smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics would be included. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, can be stored in the 2817A. Additional applications include accumulated totals for dollars, energy consumption, volume and even the logging of service performed on computer boards or systems for documentation purposes.

The Intel 2817A is cost effective for lower density E^{2}PROM applications and can therefore be used to provide a lower system cost to the user. The 2817A user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and Quality Assurance. System designers will find the 2817A reduces design time by a sizeable factor due to the integration of timing, logic and latching.

The 2817A will also open up new applications in environments where flexible parameters/data storage could not be implemented before. Applications with board space constraints are ideal for the 2817A due to the on-chip integration of all functions required.

In Application Note AP-158 a comprehensive discussion of four major application areas for E^{2}PROMs is given:

1. Remote Firmware Downloading
2. System Re-Configuration (system parameter storage)
3. Maintenance Logging
4. Electronic Message Storage

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . $-10°C$ to $+85°C$

Storage Temperature . . . . $-65°C$ to $+125°C$

All Input or Output Voltages with
Respect to Ground . . . . $+6V$ to $-0.3V$

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ AND WRITE

Temperature Range	0°C–70°C
V_{CC} Power Supply	5V ± 5%

D.C. CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
I_{CCA}	V_{CC} Current (Active)		100	mA	$\overline{OE} = \overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
I_{CCS}	V_{CC} Current (Standby)		45	mA	$\overline{CE} = V_{IH}$
I_{CCW}	V_{CC} Current (Write)		110	mA	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1	0.8	V	-1.0V spikes $\leq$ 20 ns OK
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{LKO}	V_{CC} Level for Write Lockout	3.5	4.65	V	

NOTE:
1. This parameter only sampled and not 100% tested.

CAPACITANCE $T_A = 25°C, f = 1 MHz$

Symbol	Parameter	Typ	Max	Units	Test Conditions
C_{IN}(1)	Input Capacitance	5	15	pF	$V_{IN} = 0V$
C_{OUT}(1)	Output Capacitance		10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. TEST CONDITIONS

Output Load . . . . .1 TTL gate + C_L = 100 pF

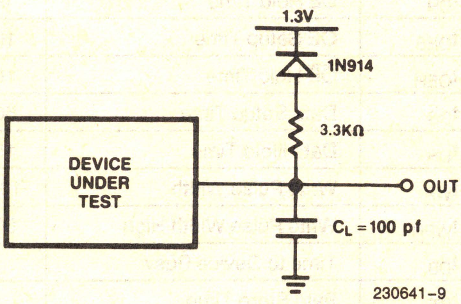
Input Rise and Fall Times (10% to 90%) . . . . .20 ns

Input Pulse Levels . . . . .0.45V to 2.4V

Input Timing Reference Level 1.5V

Output Timing Reference Level . . . . . .0.8V and 2.0V

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. CHARACTERISTICS

READ

Symbol	Parameter	2817A-1, 2817A-2 Limits		2817A 2817A-25 Limits		2817A-3 Limits		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	200		250		350		ns
t_{ACC}	Address to Output Delay		200		250		350	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		350	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100		120	ns
t_{DF}(1)	$\overline{OE}$ High to Output Not Driven	0	45	0	60	0	60	ns
t_{OH}	Output Hold from Addresses	0	0	0				ns

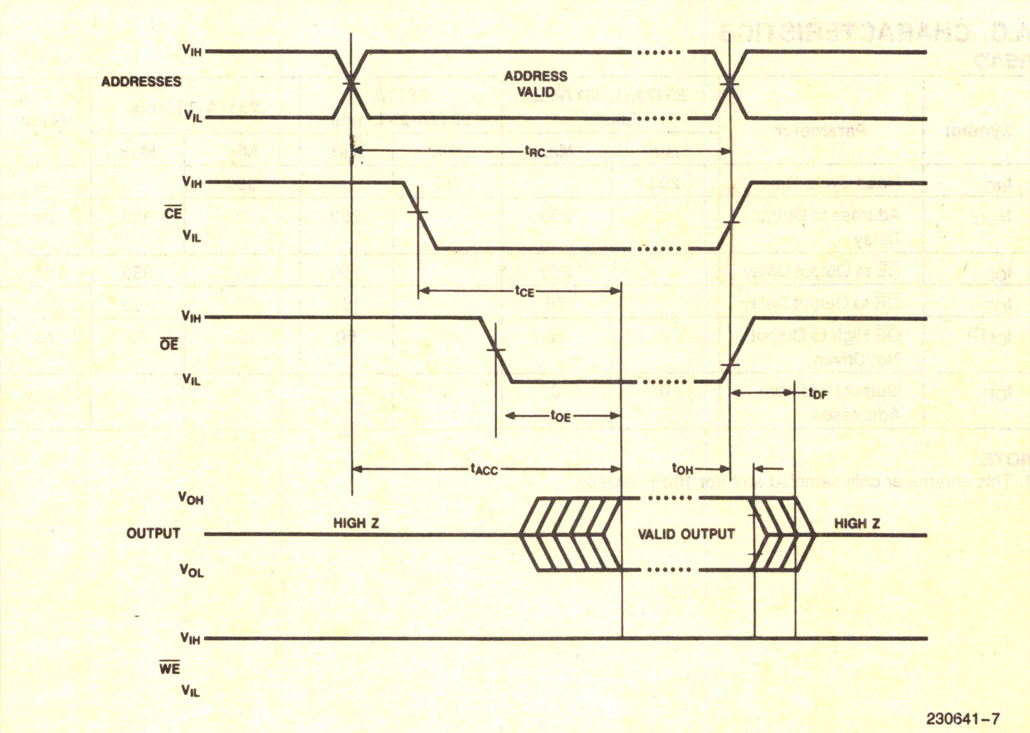
NOTE:
1. This parameter only sampled and not 100% tested.

A.C. CHARACTERISTICS (Continued)

WRITE

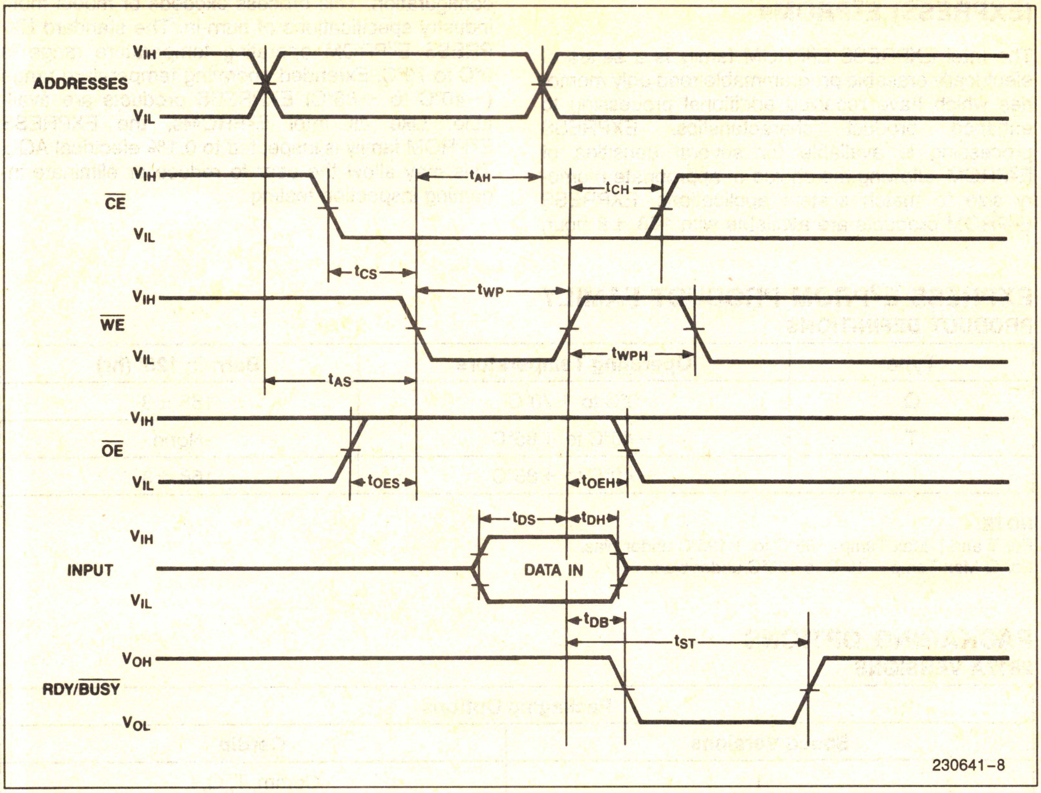
Symbol	Parameter	2817A-1 2817A-25		2817A-2 2817A		2817A-3		Units
		Min	Max	Min	Max	Min	Max	
t_{AS}	Address to Write Setup Time	10		10		10		ns
t_{AH}	Address Hold Time	50		50		50		ns
t_{CS}	$\overline{CE}$ to Write Setup Time	20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	15		15		15		ns
t_{WP}	Write Pulse Width	100		100		150		ns
t_{WPH}	Write Pulse Width High	50		50		50		ns
t_{DB}	Time to Device Busy		120		120		120	ns
t_{ST}	Byte Store Time		10		10		20	ms

A.C. WAVEFORMS FOR READ CYCLE


VIH
ADDRESSES
VIL
ADDRESS VALID
tRC
VIH
CE
VIL
tCE
VIH
OE
VIL
tOE
tDF
tACC
tOH
VOH
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
VOL
VIH
WE
VIL

230641-7

A.C. WAVEFORM FOR BYTE WRITE CYCLE


V_{IH}
ADDRESSES
V_{IL}
V_{IH}
CE
V_{IL}
t_{AH}
t_{CH}
t_{CS}
t_{WP}
V_{IH}
WE
V_{IL}
t_{WPH}
t_{AS}
V_{IH}
OE
V_{IL}
t_{OES}
t_{OEH}
t_{DS}
t_{DH}
V_{IH}
INPUT
DATA IN
V_{IL}
t_{DB}
t_{ST}
V_{OH}
RDY/BUSY
V_{OL}
230641-8

AVAILABLE LITERATURE

The Intel E²PROM family of devices, 2864A and 2817A, is supported by Application Notes. Topics covered range from Intel E²PROM Technology and Reliability to Design considerations and Applications support for Designers implementing large arrays of E²PROMs.

These notes and more are available in the Memory Components Handbook (Order No. 210830) or the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051. To obtain this book contact your local Field Sales office. Your Field Applications Engineer is available to discuss all aspects of the Intel E² product line with you.

EXTENDED TEMPERATURE (EXPRESS) E²PROMs

The Intel EXPRESS E²PROM family is a series of electrically erasable programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of E²PROM, allowing the choice of appropriate memory size to match system applications. EXPRESS E²PROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS E²PROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel E²PROMs, the EXPRESS E²PROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS E²PROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125° (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

NOTE:
For T and L Max Temp −65°C to +125°C under bias.
For Q Max Temp −10°C to 125°C under bias.

PACKAGING OPTIONS

2817A VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
−1	Comm, T, Q, L
−2	Comm, T, Q, L
−25	Comm, T, Q, L
−STD	Comm, T, Q, L
−3	Comm, T, Q, L

NOTE:
Comm = Commercial (0°C–70°C) devices.

2864A

64K (8K x 8) ELECTRICALLY ERASABLE PROM

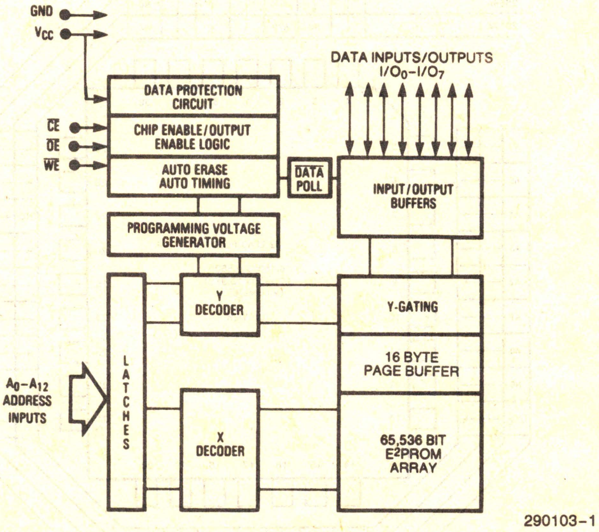
- **5 Volt Only Operation**
- **On-Chip Latches for Direct Microprocessor Interface**
- **16 Byte Page Mode**
  - **1 to 16 Byte Page Write**
  - **Self-Timed Page Store**
  - **Automatic Byte/Page ERASE before STORE**
- **Fast Read Access Time**
- **Socket Compatible with the Intel 2817A**
- **$\overline{\text{DATA}}$ Polling for End-of-Write Detection**
- **10 Year Data Retention for Each STORE**
- **Available in 28-Pin Cerdip, 28-Pin Plastic DIP, and 32-Lead Plastic Leaded Chip Carrier (PLCC) Packages**
  (See Packaging Spec, Order #231369.)

The Intel 2864A is a 5 Volt only 8K × 8 E^{2}PROM, providing 65,536 bits of completely Non-Volatile storage. A high degree of integration promotes low hardware and software overhead, and ease of use for the designer. Fast read access time makes the 2864A compatible with high performance microprocessor applications.

Writing to the Intel 2864A is as easy as writing to a byte-wide static RAM. Standard microprocessor write control signals can be used. Address and data are latched by the $\overline{\text{WE}}$ pulse or $\overline{\text{CE}}$ pulse during a write cycle. Once a write operation is started, on-chip circuitry automatically erases the storage location before writing the data. All write operation timing is done on-chip, freeing the system bus for other tasks during the write period.

The Intel 2864A page mode feature allows programming of up to 16 bytes with a single write cycle, significantly improving write time over previous E^{2}PROMs. $\overline{\text{DATA}}$ Polling is used to determine when the write operation is complete. $\overline{\text{DATA}}$ Polling is a software technique that does not require any additional hardware to detect the end of a write cycle.

The Intel 2864A is fully socket compatible with the 2817A. See Figures 1, 2, and 3 for the 2864A block diagram, pinout, and simple feature interface requirements.


GND
V_{CC}
DATA INPUTS/OUTPUTS
I/O_0–I/O_7
DATA PROTECTION CIRCUIT
$\overline{\text{CE}}$
$\overline{\text{OE}}$
$\overline{\text{WE}}$
CHIP ENABLE/OUTPUT ENABLE LOGIC
AUTO ERASE AUTO TIMING
DATA POLL
INPUT/OUTPUT BUFFERS
PROGRAMMING VOLTAGE GENERATOR
Y DECODER
Y-GATING
16 BYTE PAGE BUFFER
A_0–A_{12} ADDRESS INPUTS
LATCHES
X DECODER
65,536 BIT E^{2}PROM ARRAY

290103-1

Figure 1. 2864A Functional Block Diagram

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.

November 1986
Order Number: 290103-002

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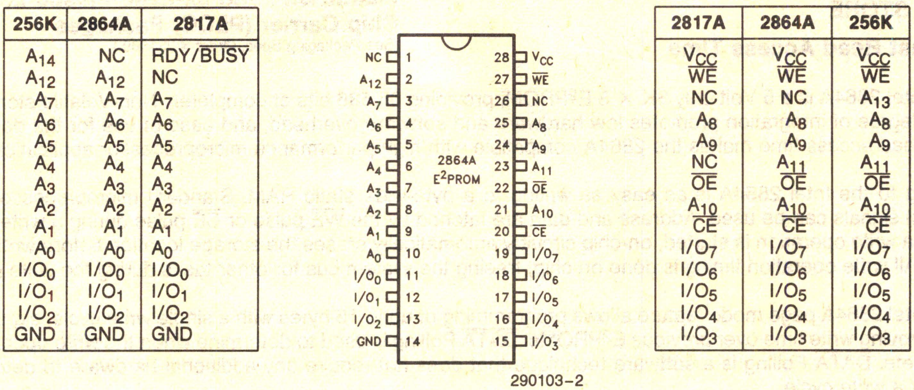
Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Data Outputs
I_0–I_7	Data Inputs
NC	No Connect
$\overline{WE}$	Write Enable



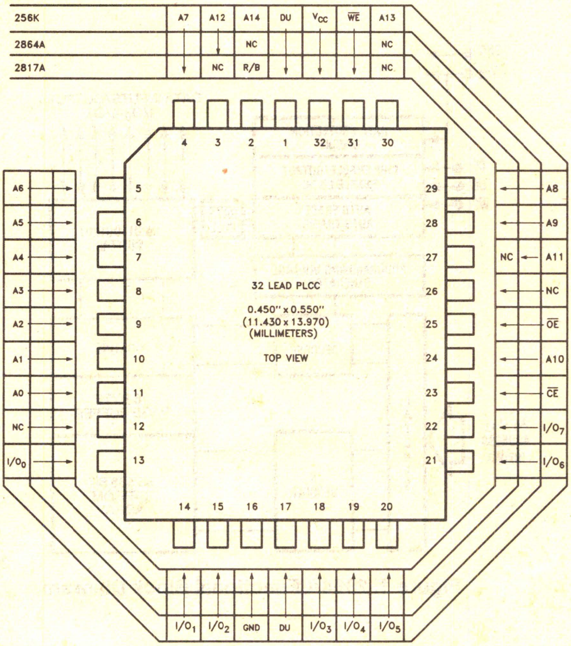
256K	2864A	2817A
A_{14}	NC	RDY/$\overline{BUSY}$
A_{12}	A_{12}	NC
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
I/O_0	I/O_0	I/O_0
I/O_1	I/O_1	I/O_1
I/O_2	I/O_2	I/O_2
GND	GND	GND

2817A	2864A	256K
V_{CC}	V_{CC}	V_{CC}
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
NC	NC	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
NC	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
I/O_7	I/O_7	I/O_7
I/O_6	I/O_6	I/O_6
I/O_5	I/O_5	I/O_5
I/O_4	I/O_4	I/O_4
I/O_3	I/O_3	I/O_3

NC 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 NC
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3
2864A
E2PROM
290103-2

NOTE:
Intel "Universal Site" Compatible E²PROM Pin Configurations are shown in the adjacent blocks.

Figure 2. Pin Configurations


256K
2864A
2817A
A7
A12
A14
DU
VCC
WE
A13
NC
NC
NC
R/B
NC
4
3
2
1
32
31
30
A6
A5
A4
A3
A2
A1
A0
NC
I/O0
5
6
7
8
9
10
11
12
13
29
28
27
26
25
24
23
22
21
A8
A9
NC
A11
NC
OE
A10
CE
I/O7
I/O6
32 LEAD PLCC
0.450" x 0.550"
(11.430 x 13.970)
(MILLIMETERS)
TOP VIEW
14
15
16
17
18
19
20
I/O1
I/O2
GND
DU
I/O3
I/O4
I/O5

290103-10

Figure 3. PLCC(N) Lead Configuration

The 2864A has four basic modes of operation which are detailed in Table 1. All modes are designed to enhance the 2864A's functionality to the user and provide total E^2PROM Microprocessor compatibility.

Table 1. Mode Selection Table

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	$I/O_0-I/O_7$ (11–13, 15–19)
STANDBY	V_{IH}	X	X	High Z
READ	V_{IL}	V_{IL}	V_{IH}	DATA Out
WRITE	V_{IL}	V_{IH}	V_{IL}	DATA In
$\overline{\text{DATA}}$ POLLING	V_{IL}	V_{IL}	V_{IH}	$\overline{\text{DATA}}$ Out

NOTE:
1. X can be V_{IH} or V_{IL}

THE STANDBY MODE

The 2864A has a standby mode which reduces the maximum active current from 140 mA to 60 mA. The 2864A is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

READ MODE

The 2864A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate the data from the output pins, independent of device selection. Assuming that addresses are stable, the address access (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

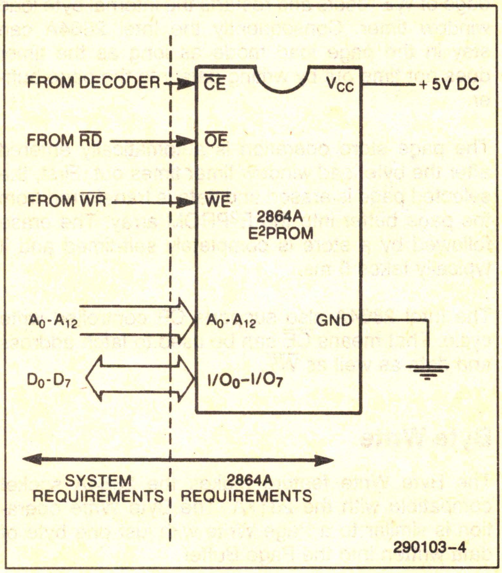


Figure 3. Simple 2864A Interface Requirements

WRITE MODE

The Intel 2864A has a new enhanced write mode which allows the user to write from 1 to 16 bytes of data in a single write cycle. The write mode is a 2 step operation. In the first step, data is written into a static RAM page buffer in a random fashion by the host system which is similar to a static RAM write operation. The second step is user transparent and initiated automatically 20 μs after the last byte has been written into the page buffer. In the following text, all references to "Page Load" imply a system write into the page buffer. "Page Store" implies transfer of data from the page buffer into the E^{2}PROM array. "Write cycle" refers to the entire page load and page store operations.

Page Write

The 2864A employs a Page Buffer consisting of 16 bytes of storage (SRAM). The E^{2}PROM array is organized into 512 pages with 16 bytes per page. Address lines A_0–A_3 select one of 16 bytes within the page buffer, while address lines A_4–A_{12} select one of 512 pages in the array.

During a write cycle, the addresses are latched on the falling edge and the data is latched on the rising edge of $\overline{WE}$. Data can be randomly written into the page buffer as long as the byte load window timer does not time out. It should be noted that the falling edge of $\overline{WE}$ resets and restarts the internal byte load window timer. Consequently the Intel 2864A can stay in the page load mode as long as the timer does not time out by writing data into the page buffer.

The page store operation is automatically entered after the byte load window timer times out. First, the selected page is erased and data is transferred from the page buffer into the E^{2}PROM array. The erase followed by a store is completely self-timed and it typically takes 5 ms.

The Intel 2864A also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

Byte Write

The Byte Write feature makes the 2864A socket compatible with the 2817A. The Byte Write operation is similar to a Page Write with just one byte of data written into the Page Buffer.

$\overline{\text{DATA}}$ POLLING MODE

$\overline{\text{DATA}}$ POLLING is a software technique to detect the completion of a Write Cycle.

During a Write Cycle, the most significant bit of the last byte written into the Page Buffer is inverted and available at I/O_7 if a Read command is issued. The device will not release true data until the Write Cycle is complete. To detect the end of a Write Cycle, the CPU can thus compare for true data on I/O_7 at the exact address (A_0–A_{12}) last written. If the data is false, the 2864A has not completed the Write Cycle. If the data is true, the 2864A has completed the Write Cycle and is now ready for another Write Cycle.

DATA PROTECTION

A write operation in the 2864A is accomplished with input signals $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, and $\overline{WE} = V_{IL}$. During a system power up or power down, this condition may occur as V_{CC} ramps up to or down from its steady state value of 5 volts. To ensure the data integrity during this power transition period, the following mechanisms are designed into Intel 2864A:

Device Lock-Out

An on-chip sensing circuit monitors the V_{CC} voltage level and disables the internal programming circuit whenever the V_{CC} level is below 3.0 volts, typically.

Write Inhibit Protection

Another form of data protection also incorporated into the 2864A is the internal write inhibit mode. The internal programming circuit will be inhibited if $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IL}$ or $\overline{WE} = V_{IH}$. These modes provide a maximum system protection solution.

SYSTEM IMPLEMENTATION

The control signals for the 2864A have been designed for ease of interfacing to today's microprocessors and microcontrollers. The $\overline{OE}$ and $\overline{WE}$ inputs of the 2864A can be connected directly to $\overline{RD}$ and $\overline{WR}$ signals of most microprocessor/microcontroller system bus control signals. The $\overline{CE}$ input is normally connected to the output of the system address decoder. The use of a separate Chip Enable and Output Enable provide a two-line control method which eliminates data bus contention in a system environment.

Figure 4 shows how the 2864A can be designed into an iAPX-188 system. In multiple E^{2}PROM configurations, the 2864A has been designed so that through proper use of two-line control, a second 2864A device may have a Write Cycle initiated after the first device has entered the Store operation. During the Store Operation, it will ignore all Write inputs and will complete the Store Operation itself. Note that the device does not enter the power standby mode until completion of the Store Operation even if the $\overline{CE}$ is no longer active.

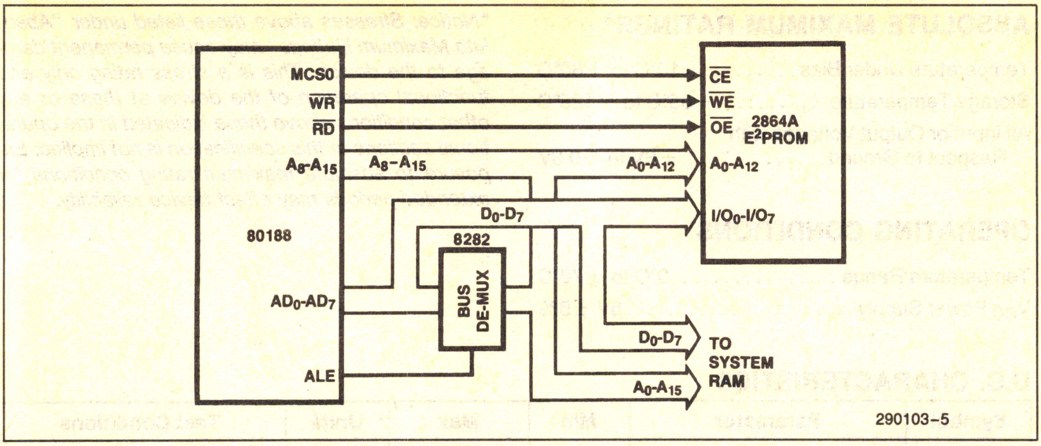


Figure 4. 2864A in an iAPX 188 System

$\overline{\text{DATA}}$ Polling mode is used to determine when the write operation has been completed. The CPU could be performing other tasks while periodically coming back to poll the 2864A.

APPLICATIONS

The Intel 2864A is ideal for non-volatile memory for program storage or data table applications, such as calibration constants, user defined functions, configuration parameters, and accumulated totals. Soft key configurations in a character oriented or graphics terminal is an example where user defined functions, such as protocol, color, screen attributes, and character fonts can be keyed in by the user. Calibration constants can be stored in the 2864A with a smart interface for a robot's axis of movement. Movement constants, compensation algorithms, and learned axis characteristics would be included. In programmable controllers and data loggers, configuration parameters for polling time, sequence, and location can be stored in the 2864A. Additional applications include accumulated totals for dollars, energy consumption, volume, and even the logging of service performed on computer boards or systems for documentation purposes.

The 2864A will also open up new applications in program storage, or in environments where flexible parameters (data storage) could not be implemented before. Applications with board space constraints are ideal for the 2864A due to the higher density and on-chip integration of all functions required.

The application note AP-158 provides a comprehensive discussion of four major applications for E^{2}PROMs:

1) Remote firmware downloading
2) System reconfiguration
3) Maintenance logging
4) Electronic mail

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . −10°C to +80°C

Storage Temperature . . . . −65°C to +125°C

All Input or Output Voltages with
Respect to Ground . . . . +6V to −0.3V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

OPERATING CONDITIONS

Temperature Range . . . . 0°C to +70°C

V_{CC} Power Supply . . . . 5V ±5%

D.C. CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max
I_{CCA}	V_{CC} Current (Read)		140	mA	$\overline{OE}, \overline{CE} = V_{IL}, \overline{WE} = V_{IH}$
I_{CCW}	V_{CC} Current (Write)		140	mA	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$ $\overline{WE} = V_{IL}$
I_{CCS}	V_{CC} Current (Standby)		60	mA	$\overline{CE} = V_{IH}$
V_{IL}	Input Low Voltage	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA

CAPACITANCE

Symbol	Parameter	Max	Units	Test Conditions
C_{IN}(1)	Input Capacitance	10	pF	$V_{IN} = 0V$ 25°C, f = 1 MHz
C_{OUT}(1)	Output Capacitance	6	pF	$\overline{OE}, \overline{CE} = V_{IH}$ 25°C, f = 1 MHz

A.C. TEST CONDITIONS

Output Load . . . . 1 TTL gate + C_L = 100 pF

Input Rise and Fall Times (10% to 90%) . . . . . . 10 ns

Input Pulse Levels . . . . 0V to 3.0V

Input Timing Reference Level 1.5V

Output Timing Reference Level 1.5V

NOTE:
1. This parameter only sampled and not 100% tested.

A.C. CHARACTERISTICS—READ CYCLE

Symbol	Parameter	2864A-25		2864A-30		2864A-35		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	250		300		350		ns
t_{ACC}	Address to Output Delay		250		300		350	ns
t_{CE}	$\overline{CE}$ to Output Delay		250		300		350	ns
t_{OE}	$\overline{OE}$ to Output Delay		150		150		150	ns
t_{DF}(1)	$\overline{OE}$ or $\overline{CE}$ HIGH to Output not Driven	10	60	10	80	10	80	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$	20		20		20		ns

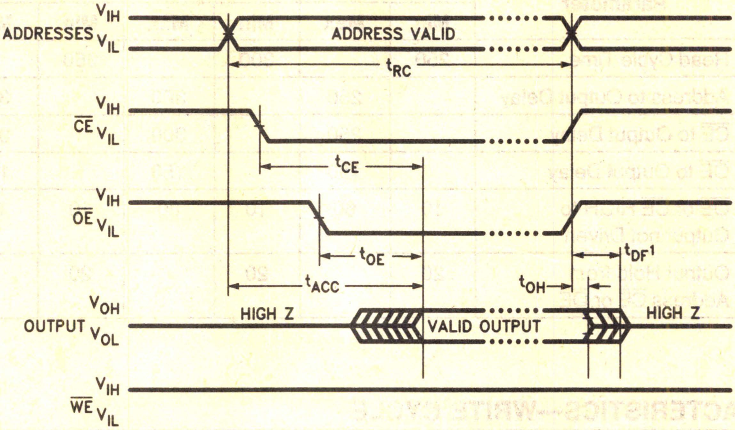
A.C. CHARACTERISTICS—WRITE CYCLE

Symbol	Parameter	2864A-25		2864A-30		2864A-35		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	250		300		350		ns
t_{AS}	Address Set Up Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Set Up Time	0		0		0		ns
t_{WP}	Write Pulse Width	150		150		150		ns
t_{AH}	Address Hold Time	200		200		200		ns
t_{DS}	Data Set Up Time	100		100		100		ns
t_{DH}	Data Hold Time	20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WPH}	Write Pulse Width High	50		50		50		ns
t_{ST}	Store Time		10		10		10	ms
t_{BLW}	Byte Load Window	3	20	3	20	3	20	μs
t_{DV}	Data Valid		300		300		300	ns

NOTE:

1. This parameter only sampled and not 100% tested.

A.C. WAVEFORMS FOR READ CYCLE

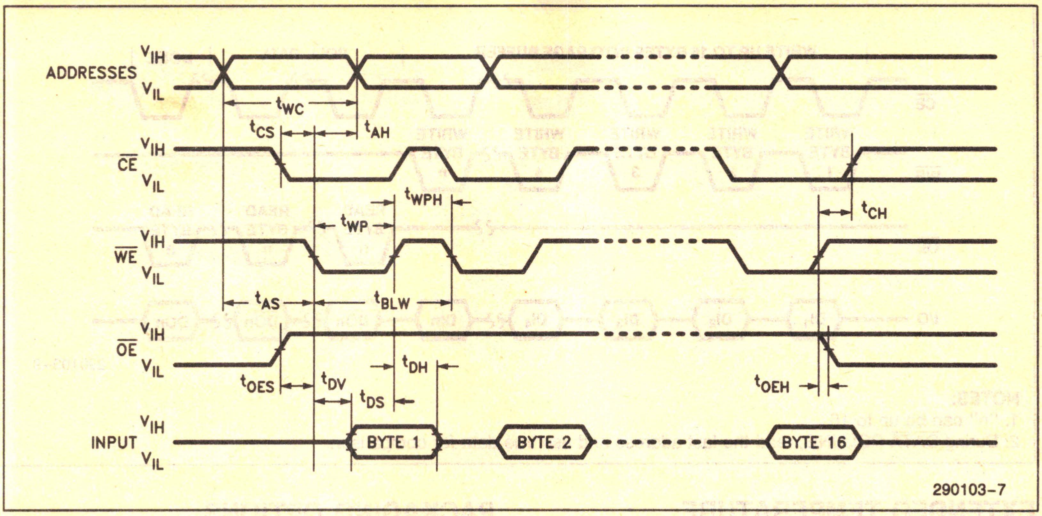

ADDRESSES
V_{IH}
V_{IL}
ADDRESS VALID
t_{RC}
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}^1
t_{ACC}
t_{OH}
OUTPUT
V_{OH}
V_{OL}
HIGH Z
VALID OUTPUT
HIGH Z
$\overline{WE}$

290103-6

NOTE:

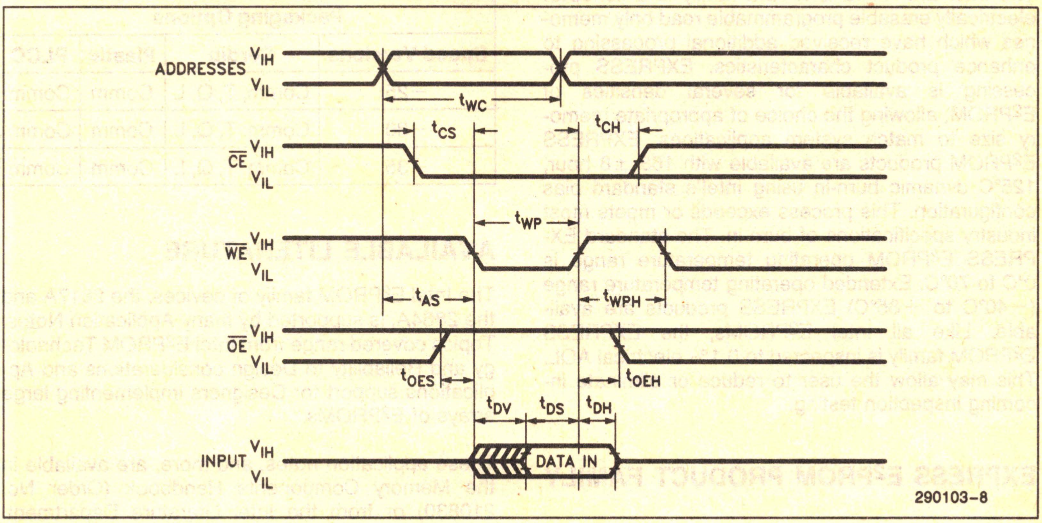
1. t_{DF} is measured from the point when $\overline{CE}$ or $\overline{OE}$ returns high (whichever occurs first) to the time when the outputs are no longer driven. This parameter is not 100% tested.

A.C. WAVEFORMS FOR PAGE WRITE CYCLE


ADDRESSES
V_IH
V_IL
t_WC
t_CS
t_AH
CE
t_WPH
t_CH
t_WP
WE
t_AS
t_BLW
OE
t_OES
t_DV
t_DH
t_DS
t_OEH
INPUT
BYTE 1
BYTE 2
BYTE 16

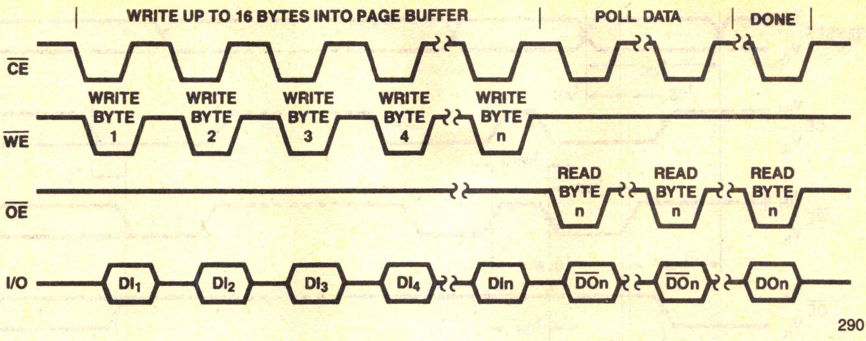
290103-7

A.C. WAVEFORMS FOR BYTE WRITE CYCLE


ADDRESSES
V_IH
V_IL
t_WC
t_CS
t_CH
CE
t_WP
WE
t_AS
t_WPH
OE
t_OES
t_OEH
t_DV
t_DS
t_DH
INPUT
DATA IN

290103-8

A.C. WAVEFORM FOR $\overline{\text{DATA}}$ POLLING


WRITE UP TO 16 BYTES INTO PAGE BUFFER
POLL DATA
DONE
$\overline{CE}$
$\overline{WE}$
$\overline{OE}$
I/O
WRITE BYTE 1
WRITE BYTE 2
WRITE BYTE 3
WRITE BYTE 4
WRITE BYTE n
READ BYTE n
READ BYTE n
READ BYTE n
DI_1
DI_2
DI_3
DI_4
DIn
$\overline{DO}$n
$\overline{DO}$n
DOn
290103-9

NOTES:
1. "n" can be up to 16
2. During $\overline{\text{DATA}}$ POLLING, read the last address and use true data for comparison.

EXTENDED TEMPERATURE (EXPRESS) E²PROMs

The Intel EXPRESS E²PROM family is a series of electrically erasable programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of E²PROM, allowing the choice of appropriate memory size to match system applications. EXPRESS E²PROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS E²PROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel E²PROMs, the EXPRESS E²PROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS E²PROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125° (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

PACKAGING OPTIONS

2864A Versions

	Packaging Options		
Speed Versions	**Cerdip**	**Plastic**	**PLCC**
−25	Comm, T, Q, L	Comm	Comm
−30	Comm, T, Q, L	Comm	Comm
−35	Comm, T, Q, L	Comm	Comm

AVAILABLE LITERATURE

The Intel E²PROM family of devices, the 2817A and the 2864A, is supported by many Application Notes. Topics covered range from Intel E²PROM Technology and Reliability to Design considerations and Applications support for Designers implementing large arrays of E²PROMs.

These application notes, and more, are available in the Memory Components Handbook (Order No. 210830) or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051. To obtain this book please contact your local Field Sales office. Your Field Applications Engineer is available to discuss all aspects of the Intel E² product line with you.

November 1986

Designing with the System Friendly 2817A 5V-Only E^{2}PROM

JUSTIN ORION
APPLICATIONS ENGINEER
INTEL CORPORATION

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Order Number: 230714-002

INTRODUCTION

Valuable New System Capabilities Now Possible with E^2PROMs

E^2PROMs provide the designer with non-volatile in-circuit writable memory for any size microprocessor based system at a cost and space requirement equivalent to that of the microprocessor chip itself. Application areas range from small stand-alone systems such as the 8088 based PC board shown in this Applications Note to large systems that require highly reliable solid state non-volatile memory operating in harsh environments.

This Application Note shows how the 2817A intelligent E^2PROM can be used in four major application areas:

1. Remote Firmware Downloading
2. System Reconfiguration
3. Maintenance Logging
4. Electronic Message Storage

A small, stand-alone 2817A/8088 system that demonstrates these applications is described in detail. Listings of the software used to run the 2817A/8088 PC board are included. A number of key hardware and software interface options are also discussed in detail.

Evolution of the E^2PROM

The 2816 represents the first E^2PROM generation. The 2816 required external address and data latches, erase and write pulse timing, Vpp waveshaping, a 21V supply, and a power up/down write protection circuit. (see Figure 1). The next generation E^2PROM was the 2817 which had all of the above interface circuit requirements, except for the last two, built into the device. The 2817 also had a RDY/$\overline{\text{BUSY}}$ output to indicate when a write operation is completed. Regarded as an "intelligent" E^2PROM, the 2817 was a radical improvement because it could be directly connected to any system bus without slowing the bus down. The 2817 required only a standard system write pulse to perform a write operation. The present generation of the E^2PROM is the 2817A. This device is exactly like the 2817 except that the 21V supply and the write protection circuit is on the chip as shown in Figure 1.

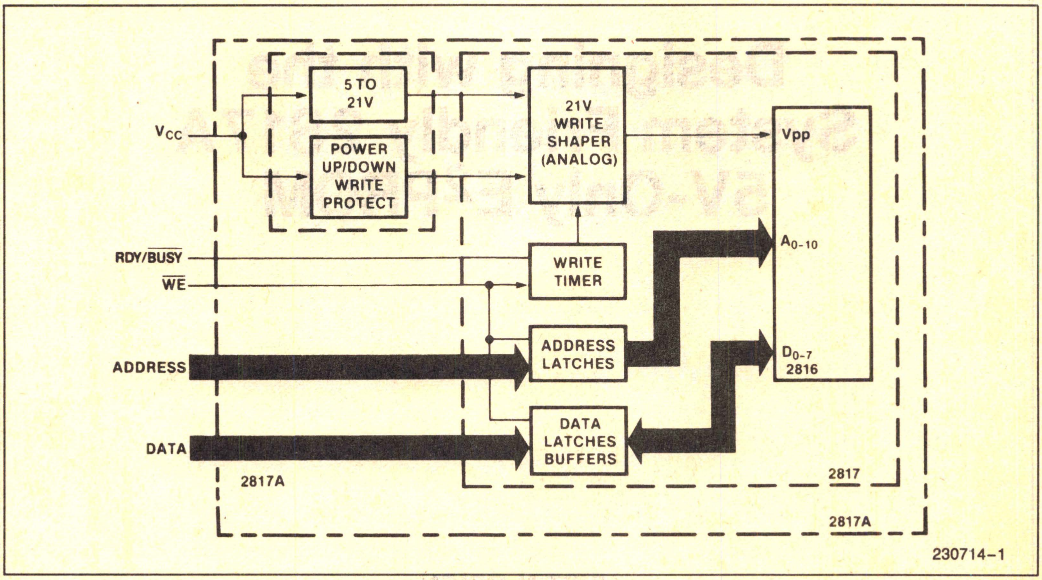


Figure 1. E^2PROM Evolution: Increasing Intelligence On-Chip

Advantages of an Intelligent E^2PROM

The 2817A has on-chip latches and timing which allow it to connect directly to the microprocessor data bus. Writing a byte to the 2817A is accomplished by sending a write pulse to the part. The timing for this pulse is the same as the timing for a static RAM write cycle. Upon receiving this write pulse the 2817A starts a write operation. During a write operation the 2817A's data lines go to a high impedance state, allowing normal processing to continue on the microprocessor data bus. After the write operation has been completed, the system CPU is notified via the 2817A's RDY/$\overline{\text{BUSY}}$ output. The RDY/$\overline{\text{BUSY}}$ signal frees the designer from having to time the E^2PROM write operation by either hardware timing logic or software time-out loops.

Note that while performing a write operation the 2817A will not respond to read or write requests. The 2817A's data bus will remain in a high impedance state, regardless of the input control signals, until the write operation has been completed.

APPLICATIONS FOR E^2PROMS

Application Area # 1: Firmware Remote Downloading

Remote downloading is important in any system that uses firmware to store program code. Storing software in ultraviolet erasable EPROMs has the advantages of being non-volatile and allowing zero wait-state execution with high-speed processors such as the 8 MHz 8086-2. A limitation of this method of firmware storage is that system software usually has bugs in the first year or so and is frequently improved or upgraded. To make a firmware change in a system with UV EPROMs a serviceperson must go to each customers site, partially disassemble each system, replace the EPROMs, and reassemble the system. Now, by storing some or all of the system software code in E^2PROMs, software changes can be made by telephone, without sending a serviceperson to the customer site. To make software changes in E^2PROMs, the serviceperson calls the customer site, connects the system to the service center computer via telephone, and transfers the new code to the customer's system. In less than a minute the system can be up and running with the new software at a minimal cost to the manufacturer or customer.

Firmware stored in E^2PROM can be changed/upgraded remotely over any type of communications link.

All E^2PROM or a Combination of EPROM/E^2PROM?

System firmware can be completely stored in E^2PROM to allow remote alterability of all code, or a combination of E^2PROM and UV PROM can be used.

If the firmware is completely stored in E^2PROM, any or all of the firmware can be replaced electrically. This type of system is shown in Figure 2. When the system is prepared for shipping, the operating system software is downloaded directly into the E^2PROM memory after the E^2PROMs have been installed in the system. When the software is changed, upgraded, or expanded the entire new software package can be loaded remotely over the telephone.

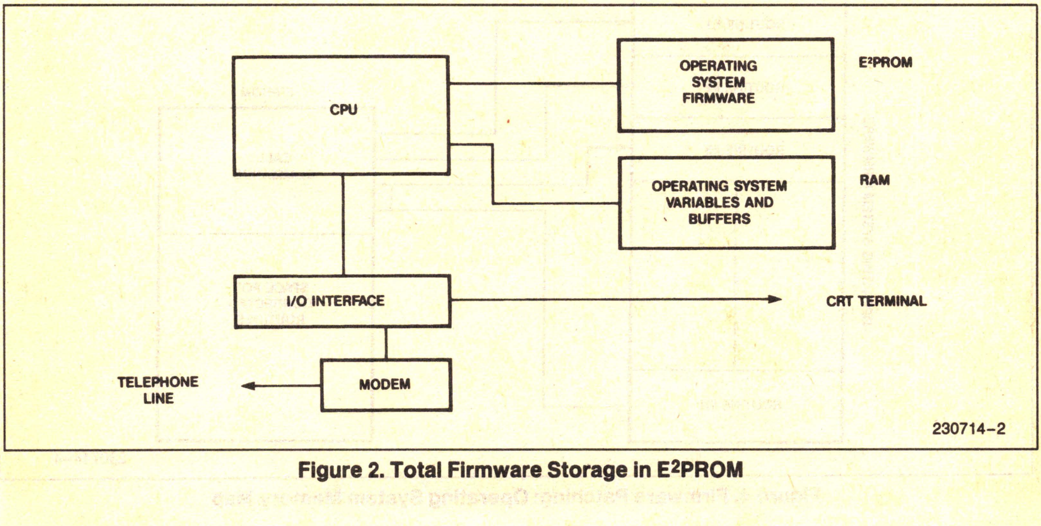


Figure 2. Total Firmware Storage in E^2PROM

In a system with a large amount of program code, it may be desirable to use EPROM for storing most of the firmware and use E²PROM for the corrected portions of the code (see Figure 3). This method, sometimes called "firmware patching," allows a system to use high density EPROM to store a firmware package that is segmented into a number of sections or routines. A small part of the system's E²PROM is used to store a short program that calls each routine as it is needed (see Figure 4). When an error is found in one of the firmware routines, a corrected version is loaded into the extra E²PROM space. The new corrected routine is then called instead of the erroneous routine by changing the calling program (see Figure 5). The corrected routine and new call command can be sent directly from a service center to the system at the customer site over any telephone line.

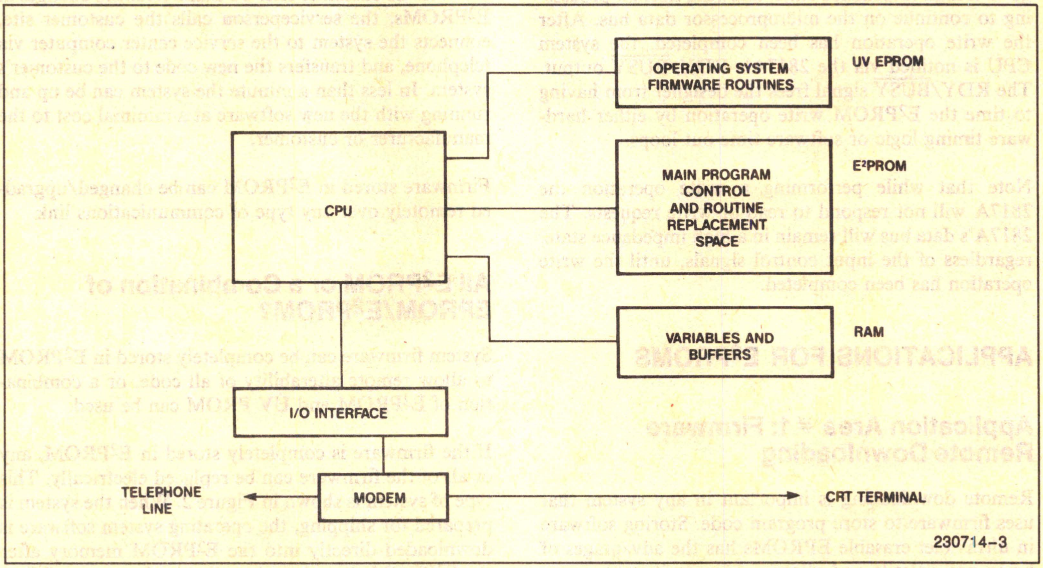

OPERATING SYSTEM FIRMWARE ROUTINES
UV EPROM
MAIN PROGRAM CONTROL AND ROUTINE REPLACEMENT SPACE
E²PROM
CPU
VARIABLES AND BUFFERS
RAM
I/O INTERFACE
TELEPHONE LINE
MODEM
CRT TERMINAL
230714-3

Figure 3. Partial Firmware Storage in E²PROM

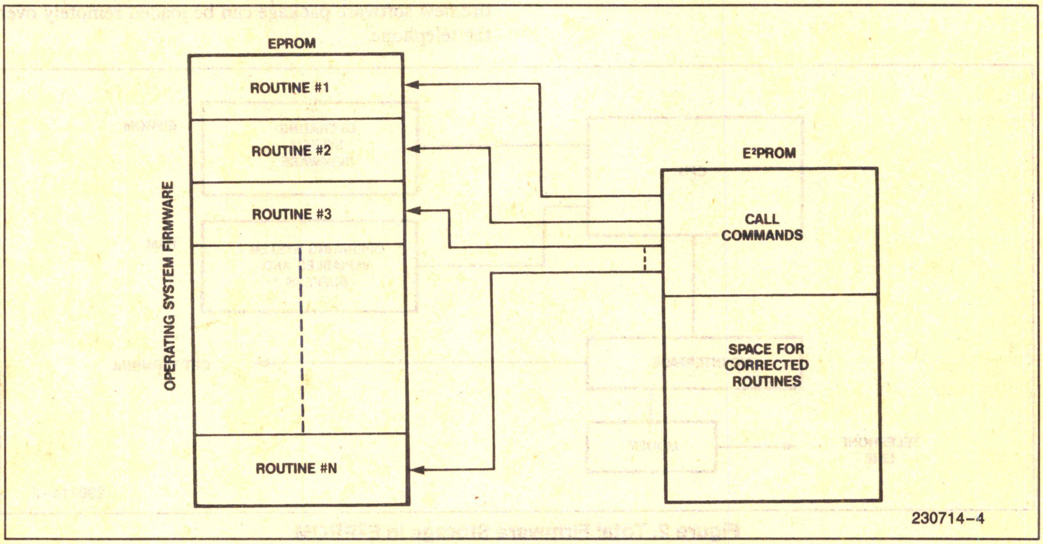

EPROM
ROUTINE #1
ROUTINE #2
ROUTINE #3
ROUTINE #N
OPERATING SYSTEM FIRMWARE
E²PROM
CALL COMMANDS
SPACE FOR CORRECTED ROUTINES
230714-4

Figure 4. Firmware Patching: Operating System Memory Map

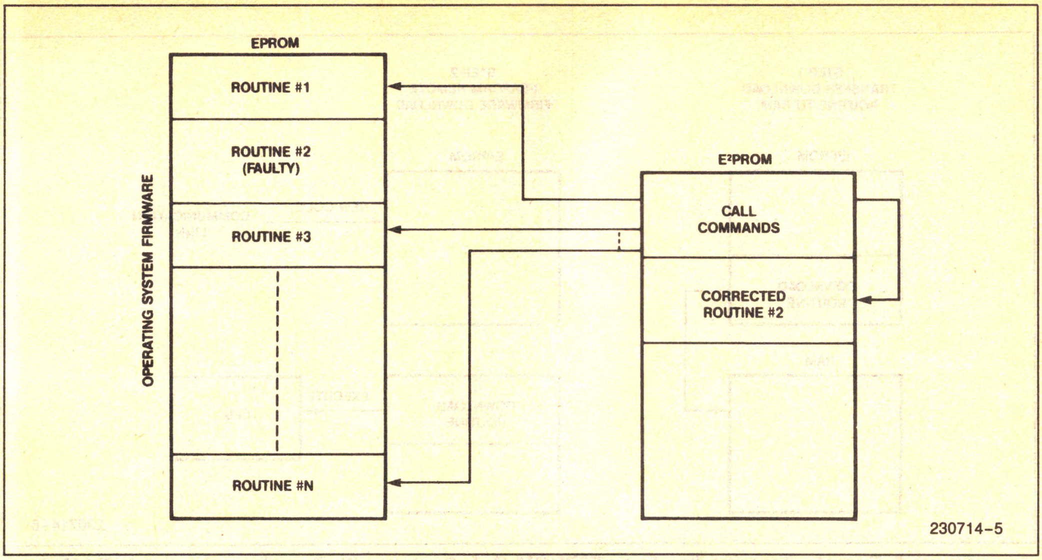


Figure 5. Firmware Patching Example: Replacement of Fault Routine with Corrected Routine in E^{2}PROM

Easy Software Upgrades

Software corrections, upgrades, or the addition of software options are easily done in a system using E^{2}PROMs for complete or partial firmware storage. The following is a typical example.

The OEM's service center calls the customer on the telephone and tells him that the center wishes to upgrade the customer's system firmware. The center instructs the system operator to set a "download" switch on the system, connect the phone to the system, and depress the system RESET switch. The new software is transferred from the center to the customer system, where it is stored in E^{2}PROM. The new software package then tests itself and the system. The system's CRT display keeps the operator informed of each step in the process. When the system test is done, the CRT display instructs the operator to disconnect the phone, turn off the "download" switch, and reset the system. The system is now up and running with the new software after only 40 seconds of down time (see Figure 29).

Hardware Implementation of Remote Downloading

As the new code is being received over the phone from the service center it is loaded into RAM. The code is sent in blocks and a checksum is sent with each block. If a data error occurs due to a poor phone connection the block is re-transmitted. Once the entire program has been correctly received, it is transferred to E^{2}PROM.

In a system using both EPROM/ROM and E^{2}PROM the downloading software routine is executed out of the EPROM/ROM. In a system with only E^{2}PROM, the downloading routine can be executed either out of the system RAM or out of E^{2}PROM. With the first method the downloading routine is transferred from E^{2}PROM to RAM (see Figure 6). The routine is then executed out of RAM and the new code is loaded remotely over a communications link into E^{2}PROM. A copy of the downloading routine is included in the new code in the E^{2}PROM for future remote upgrades. At the end of the transfer operation, control is passed back to the new program in E^{2}PROM.

In systems where there are two or more E^{2}PROMs the downloading routine can be initially executed out of the first E^{2}PROM (see Figure 7). After the new program code has been loaded into the rest of the E^{2}PROMS in the system, execution control is passed to a copy of the download routine in E^{2}PROM #2, as shown in Figure 7. The remaining new code is then loaded into E^{2}PROM #1.

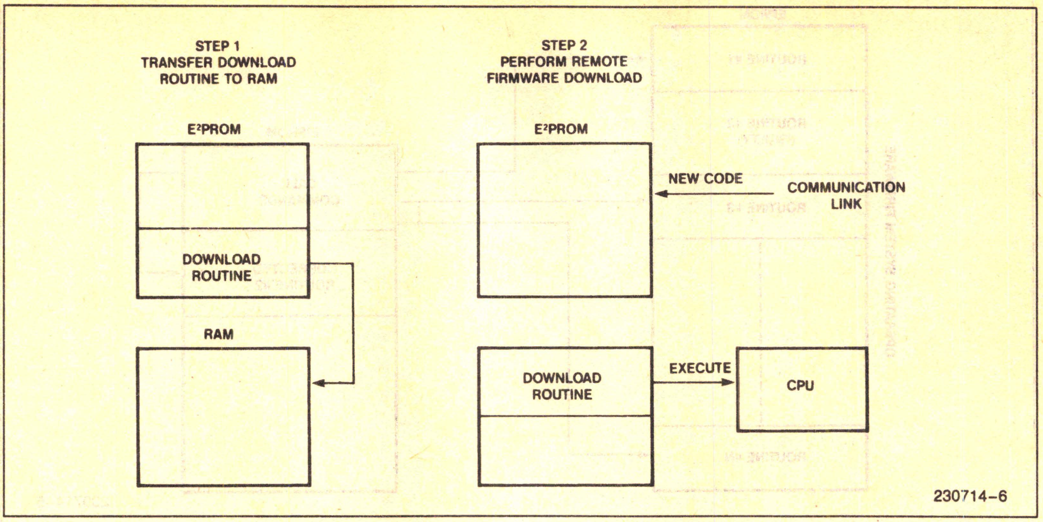

STEP 1
TRANSFER DOWNLOAD
ROUTINE TO RAM
E²PROM
DOWNLOAD
ROUTINE
RAM
STEP 2
PERFORM REMOTE
FIRMWARE DOWNLOAD
E²PROM
NEW CODE
COMMUNICATION
LINK
DOWNLOAD
ROUTINE
EXECUTE
CPU
230714-6

Figure 6. Remote Downloading to an E²PROM-Only System with Download Routine in RAM

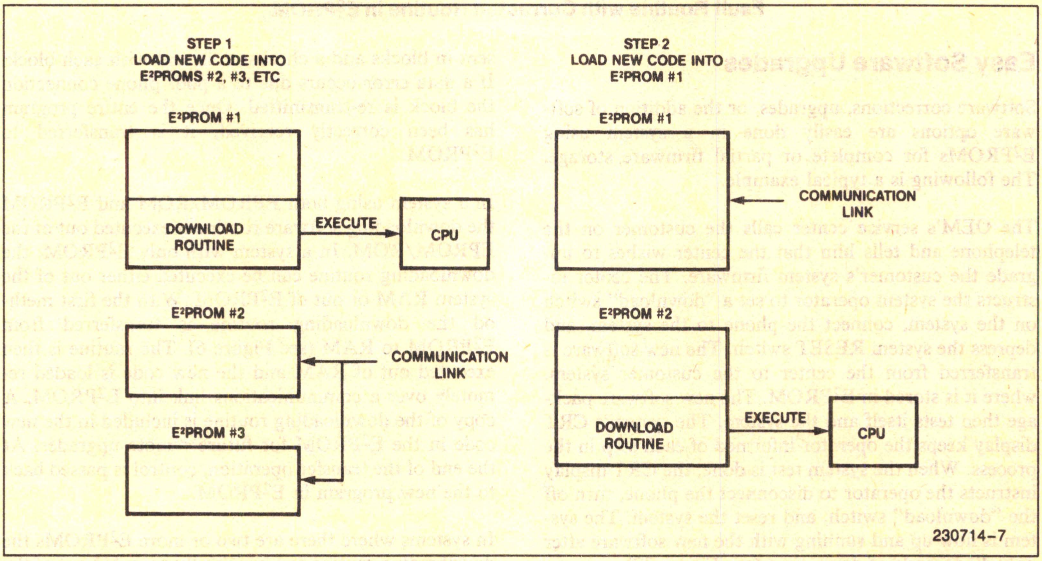

STEP 1
LOAD NEW CODE INTO
E²PROMS #2, #3, ETC
E²PROM #1
DOWNLOAD
ROUTINE
EXECUTE
CPU
E²PROM #2
COMMUNICATION
LINK
E²PROM #3
STEP 2
LOAD NEW CODE INTO
E²PROM #1
E²PROM #1
COMMUNICATION
LINK
E²PROM #2
DOWNLOAD
ROUTINE
EXECUTE
CPU
230714-7

Figure 7. Remote Downloading to an E²PROM-Only System with Downloading Routine in E²PROM

Demo Circuit

The 2817A/8088 stand-alone system design shown in this applications note can send data over a serial RS232 cable, as shown in the block diagram in Figure 8. This design can also send over any telephone line using an acoustic coupler. The hookup for transmission over a phone line is shown in Figure 9. The software on the applications demo board is set up to send text messages between boards when they are connected as shown in Figure 8 or 9. The messages are then stored in E^2PROM memory where they remain unchanged until it is desired to delete a message or clear the message array. It can be seen that program code rather than text messages can just as easily be transferred between the two systems and stored in E^2PROM memory. The downloading routine would be transferred to and executed from the system RAM. The new program code would then be executed directly out of E^2PROM.

The "modified serial cable" shown in Figure 8 is an RS232 serial cable with the send and receive lines switched as shown in Figure 10.

The 8088 software for performing a data block transfer between systems is shown in Appendix A. Figures 11 and 12 show the flow charts for the data transfer software routines.

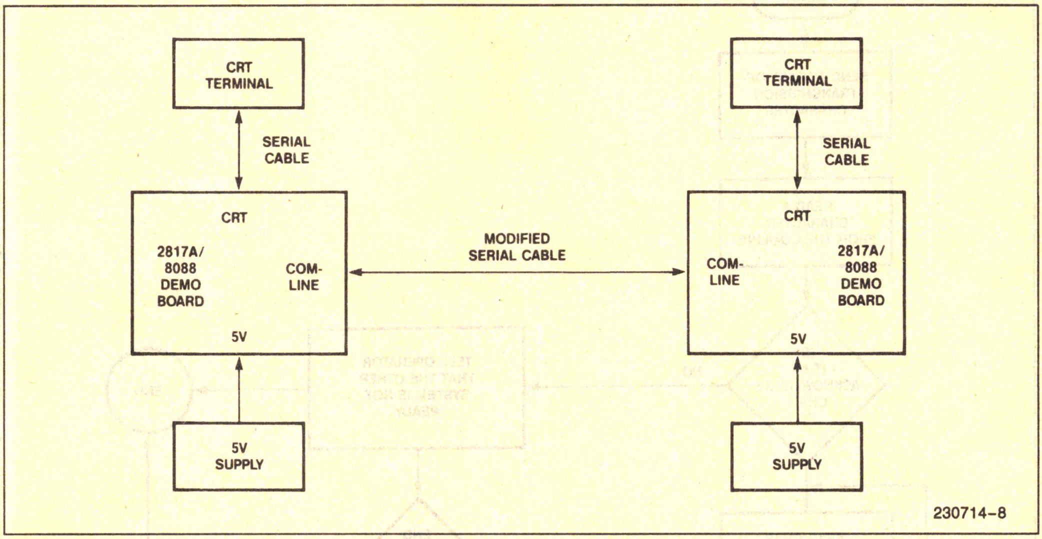

CRT TERMINAL
SERIAL CABLE
CRT
2817A/ 8088 DEMO BOARD
COM-LINE
5V
5V SUPPLY
MODIFIED SERIAL CABLE
CRT TERMINAL
SERIAL CABLE
CRT
COM-LINE
2817A/ 8088 DEMO BOARD
5V
5V SUPPLY
230714-8

Figure 8. Remote Download Demo Hookup

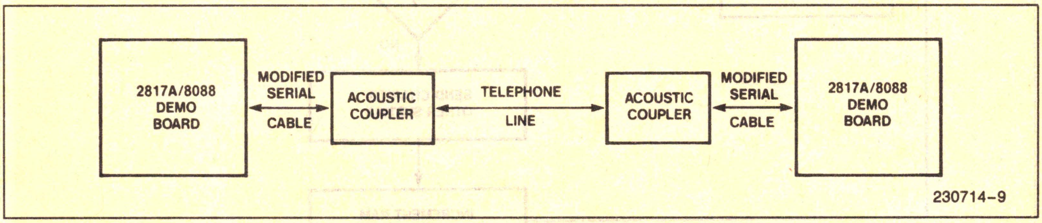

2817A/8088 DEMO BOARD
MODIFIED SERIAL CABLE
ACOUSTIC COUPLER
TELEPHONE LINE
ACOUSTIC COUPLER
MODIFIED SERIAL CABLE
2817A/8088 DEMO BOARD
230714-9

Figure 9. Remote Downloading over a Telephone Line Using the 2817A/8088 Demo Board

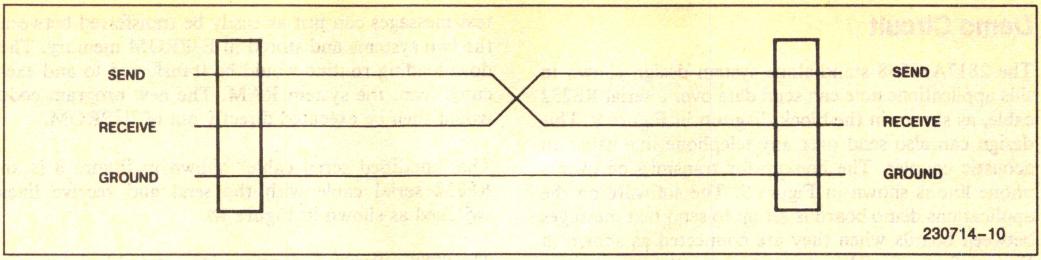

SEND
RECEIVE
GROUND
SEND
RECEIVE
GROUND
230714-10

Figure 10. Modified RS232 Serial Cable

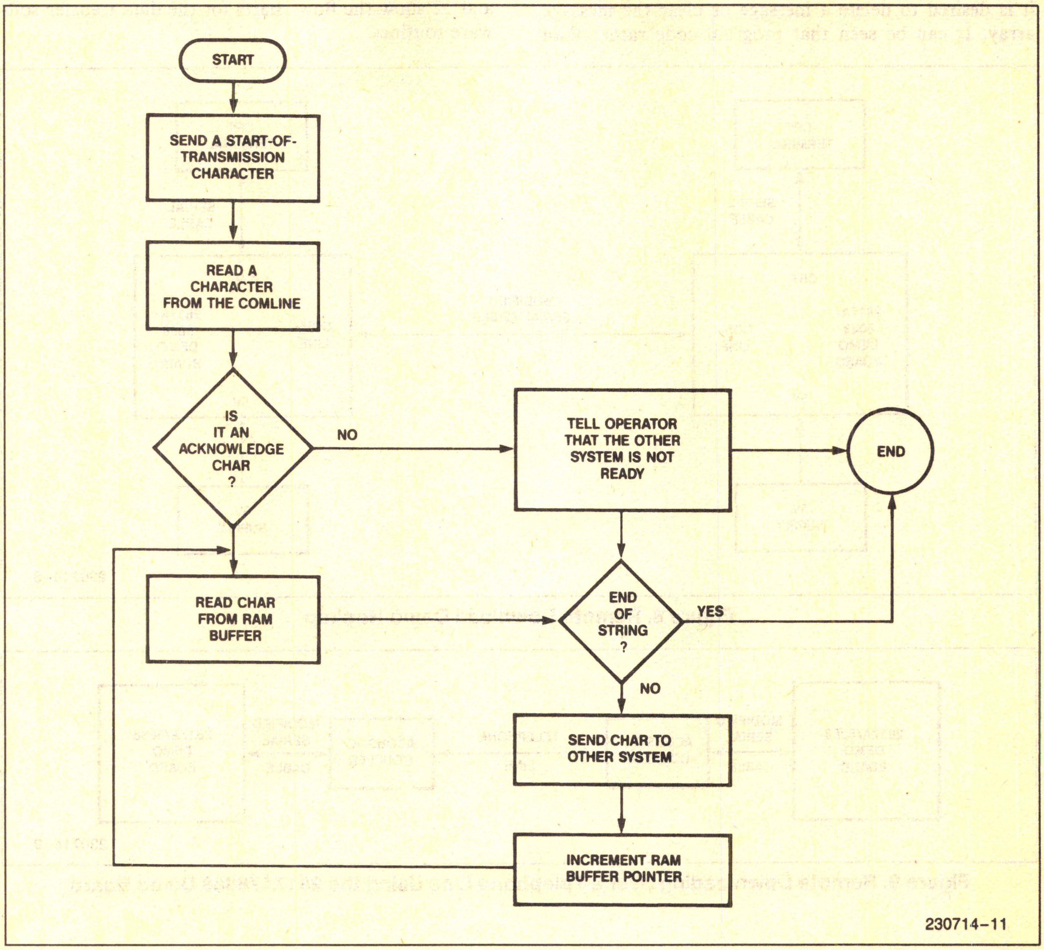

START
SEND A START-OF-TRANSMISSION CHARACTER
READ A CHARACTER FROM THE COMLINE
IS IT AN ACKNOWLEDGE CHAR ?
NO
TELL OPERATOR THAT THE OTHER SYSTEM IS NOT READY
END
READ CHAR FROM RAM BUFFER
END OF STRING ?
YES
NO
SEND CHAR TO OTHER SYSTEM
INCREMENT RAM BUFFER POINTER
230714-11

Figure 11. Data Transfer Software: Transmitting System

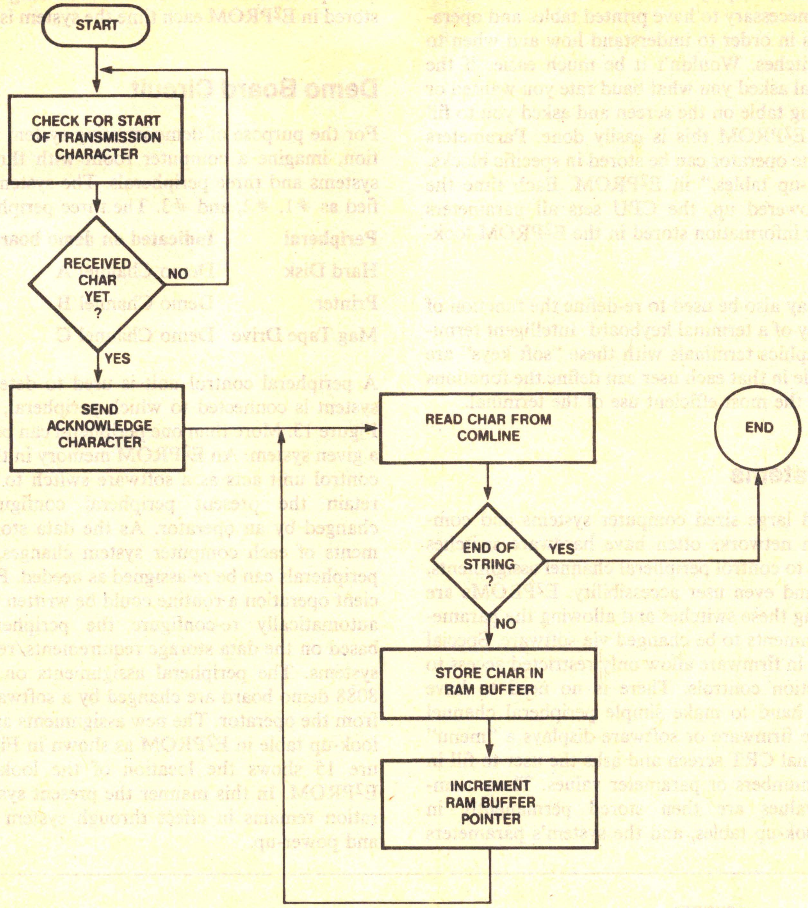

START
CHECK FOR START OF TRANSMISSION CHARACTER
RECEIVED CHAR YET ?
NO
YES
SEND ACKNOWLEDGE CHARACTER
READ CHAR FROM COMLINE
END OF STRING ?
YES
NO
END
STORE CHAR IN RAM BUFFER
INCREMENT RAM BUFFER POINTER
230714–12

Figure 12. Data Transfer Software: Receiving System

Since serial channel drivers in this design do not provide full spec RS232 levels, the serial cables should be kept under 10 feet in length. The drivers are less than full spec to reduce the complexity of this system for demonstration purposes. These drivers require only a 5V supply to operate rather than the +12V and −12V required for standard RS232 interfaces. The circuit description for the RS232 serial channel drivers under the section, "2817A/8088 Applications Demo Board Circuit Operation" gives more information on the circuitry and also shows a design example for a full spec RS232 interface.

Application Area #2: System Reconfiguration

Small Systems—User Friendly Operation

In small systems such as modems, point of sale terminals, and data terminals, hardware switches have been used to set operation parameters such as baud rates, synchronous/asynchronous selection, and data constants (tax rates, display attributes, and many others). It is usually necessary to have printed tables and operation manuals in order to understand how and when to set these switches. Wouldn't it be much easier if the CRT terminal asked you what baud rate you wanted or drew a pricing table on the screen and asked you to fill it in? With E^{2}PROM this is easily done. Parameters entered by the operator can be stored in specific blocks, called "look-up tables," in E^{2}PROM. Each time the system is powered up, the CPU sets all parameters based on the information stored in the E^{2}PROM look-up table.

E^{2}PROM may also be used to re-define the function of any given key of a terminal keyboard. Intelligent terminals and graphics terminals with these "soft keys" are highly flexible in that each user can define the functions he needs for the most efficient use of the terminal.

Large Systems

Medium and large sized computer systems and computer system networks often have hardware switches and jumpers to control peripheral channel assignments, data rates, and even user accessibility. E^{2}PROMs are now replacing these switches and allowing the parameters or assignments to be changed via software. Special access codes in firmware allow only restricted access to critical function controls. There is no need to have manuals on hand to make simple peripheral channel changes. The firmware or software displays a "menu" on the terminal CRT screen and asks the user to fill in the desired numbers or parameter values. These numbers and values are then stored permanently in E^{2}PROM look-up tables, and the system's parameters and operational modes are set according to the values stored in E^{2}PROM each time the system is powered up.

Demo Board Circuit

For the purpose of demonstrating system re-configuration, imagine a computer room with three computer systems and three peripherals. The systems are identified as #1, #2, and #3. The three peripherals are:

Peripheral	Indicated on demo board as:
Hard Disk	Demo Channel A
Printer	Demo Channel B
Mag Tape Drive	Demo Channel C

A peripheral control unit is used to determine which system is connected to which peripheral, as shown in Figure 13. More than one peripheral can be allocated to a given system. An E^{2}PROM memory in the peripheral control unit acts as a software switch to permanently retain the present peripheral configuration until changed by an operator. As the data storage requirements of each computer system changes, the various peripherals can be re-assigned as needed. For more efficient operation a routine could be written which would automatically re-configure the peripheral channels based on the data storage requirements/requests of the systems. The peripheral assignments on the 2817A/8088 demo board are changed by a software command from the operator. The new assignments are stored in a look-up table in E^{2}PROM as shown in Figure 14. Figure 15 shows the location of the look-up table in E^{2}PROM. In this manner the present system configuration remains in effect through system power-down and power-up.

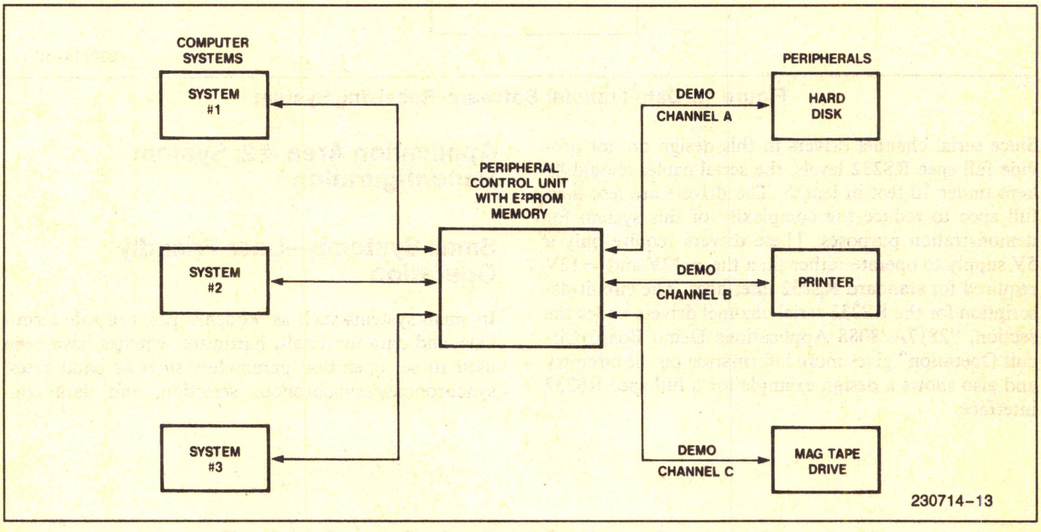


Figure 13. System Re-Configuration Demo: Computer Room

		PERIPHERAL
BYTE #1	SYSTEM #	(DEMO CHANNEL A) HARD DISK
BYTE #2	SYSTEM #	(DEMO CHANNEL B) PRINTER
BYTE #3	SYSTEM #	(DEMO CHANNEL C) MAG TAPE DRIVE

The value "System #" Determines Which System has access to the Peripheral.

Figure 14. System Re-Configuration Look-Up Table

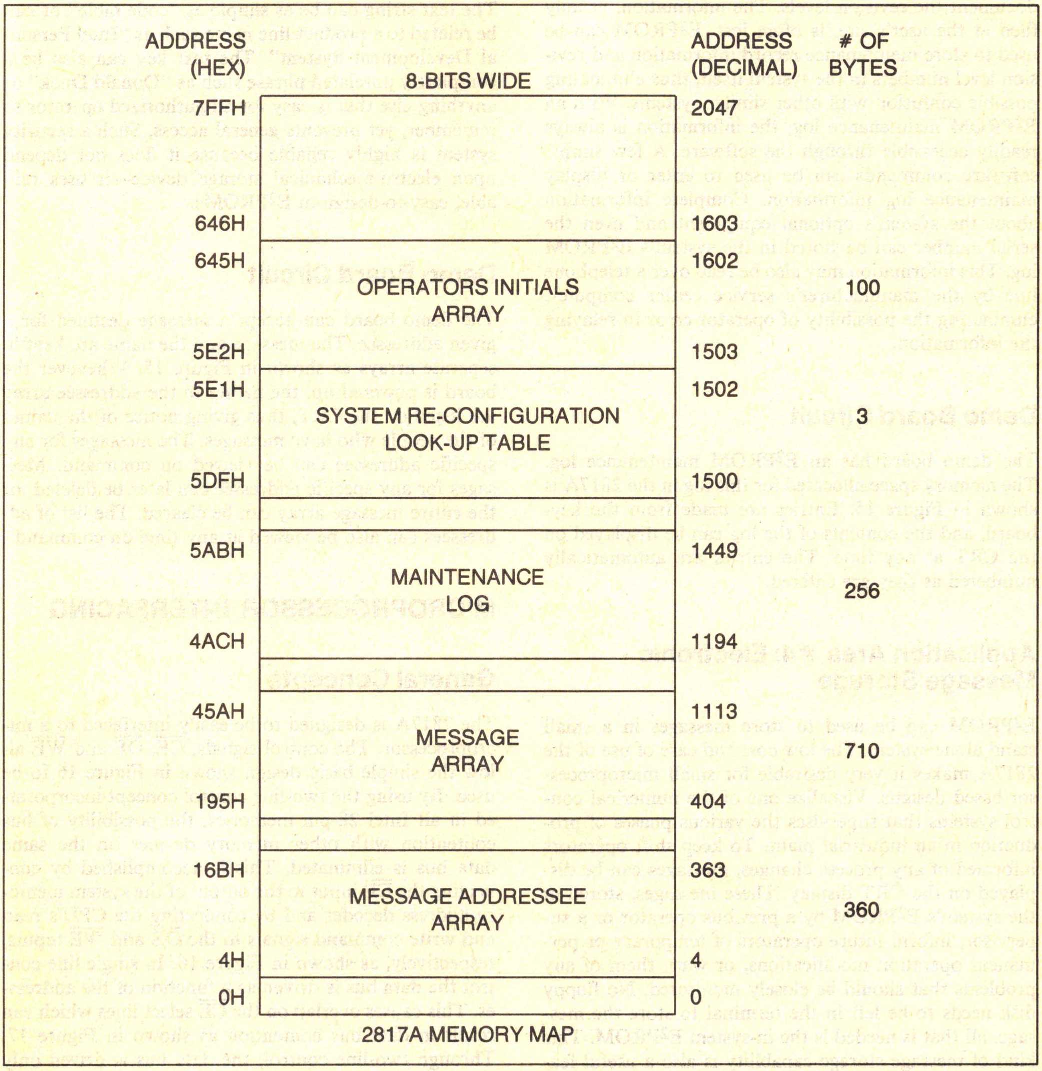

ADDRESS (HEX)
8-BITS WIDE
ADDRESS (DECIMAL)
# OF BYTES
7FFH
2047
646H
1603
645H
1602
OPERATORS INITIALS ARRAY
100
5E2H
1503
5E1H
1502
SYSTEM RE-CONFIGURATION LOOK-UP TABLE
3
5DFH
1500
5ABH
1449
MAINTENANCE LOG
256
4ACH
1194
45AH
1113
MESSAGE ARRAY
710
195H
404
16BH
363
MESSAGE ADDRESSEE ARRAY
360
4H
4
0H
0
2817A MEMORY MAP

Figure 15. 2817A/8088 Applications Demo

Further detailed information on the hardware operation of the System Reconfiguration Demo is given in the section "2817A/8088 Applications Demo Board Circuit Operation" under "Demo Channel Display LED Ports."

Application Area #3: Maintenance Log

When equipment is repaired or upgraded it is important to record the nature of each repair problem and to document the revision levels. The information, usually filed at the user's site, is often lost. E^{2}PROM can be used to store maintenance record information and revision level numbers in the system itself, thus eliminating possible confusion with other similar systems. With an E^{2}PROM maintenance log, the information is always readily accessible through the software. A few simple software commands can be used to enter or display maintenance log information. Complete information about the system's optional equipment and even the serial number can be stored in the system's E^{2}PROM log. This information may also be read over a telephone line by the manufacturer's service center computer, eliminating the possibility of operator error in relaying the information.

Demo Board Circuit

The demo board has an E^{2}PROM maintenance log. The memory space allocated for this log in the 2817A is shown in Figure 15. Entries are made from the keyboard, and the contents of the log can be displayed on the CRT at any time. The entries are automatically numbered as they are entered.

Application Area #4: Electronic Message Storage

E^{2}PROM can be used to store messages in a small stand-alone system. The low cost and ease of use of the 2817A makes it very desirable for small microprocessor-based designs. Visualize one of the numerical control systems that supervises the various phases of production in an industrial plant. To keep shift operators informed of any process changes, messages can be displayed on the CRT display. These messages, stored in the system's E^{2}PROM by a previous operator or a supervisor, inform future operators of temporary or permanent operation modifications, or warn them of any problems that should be closely monitored. No floppy disk needs to be left in the terminal to store the message: all that is needed is the in-system E^{2}PROM. This kind of message storage capability is also a useful feature on personal computers, personal development systems, and intelligent modems.

Another application for E^{2}PROM message storage is re-programmable restricted access keys to computer systems. In a system using E^{2}PROM for security control, access to critical data can be restricted based on specific text strings, or "keys", that are entered by the operator. In this type of system the "keys" are stored in E^{2}PROM and are changed as needed by an authorized company officer. For example, a data processing system using this technique allows access to sensitive product cost tables only upon receipt of a specific text string that is determined by an authorized company officer. The text string can be as simple as "code table" or can be related to a product line name such as "Intel Personal Development System". The text key can also be a completely unrelated phrase such as "Donald Duck" or anything else that is easy for an authorized operator to remember, yet prevents general access. Such a security system is highly reliable because it does not depend upon electro-mechanical storage device—it uses reliable, easy-to-design-in E^{2}PROMs.

Demo Board Circuit

The demo board can accept a message destined for a given addressee. The message and the name are kept in separate arrays as shown in Figure 15. Whenever the board is powered up, the names in the addressee array are listed on the CRT, thus giving notice of the names of the people who have messages. The messages for any specific addressee can be viewed on command. Messages for any specific addressee can later be deleted, or the entire message array can be cleared. The list of addressees can also be viewed at any time on command.

MICROPROCESSOR INTERFACING

General Concepts

The 2817A is designed to be easily interfaced to a microprocessor. The control signals, $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ allow the simple basic design shown in Figure 16 to be used. By using the two-line control concept incorporated in all Intel 28-pin memories, the possibility of bus contention with other memory devices on the same data bus is eliminated. This is accomplished by connecting the $\overline{CE}$ input to the output of the system memory address decoder and by connecting the CPU's read and write command signals to the $\overline{OE}$ and $\overline{WE}$ inputs, respectively, as shown in Figure 16. In single line control the data bus is driven as a function of the addresses. This causes overlap on the $\overline{CE}$ select lines which can result in data bus contention as shown in Figure 17. Through two-line control, the data bus is driven only when both the address select ($\overline{CE}$) and the memory command ($\overline{RD}$) are active (see Figure 18).

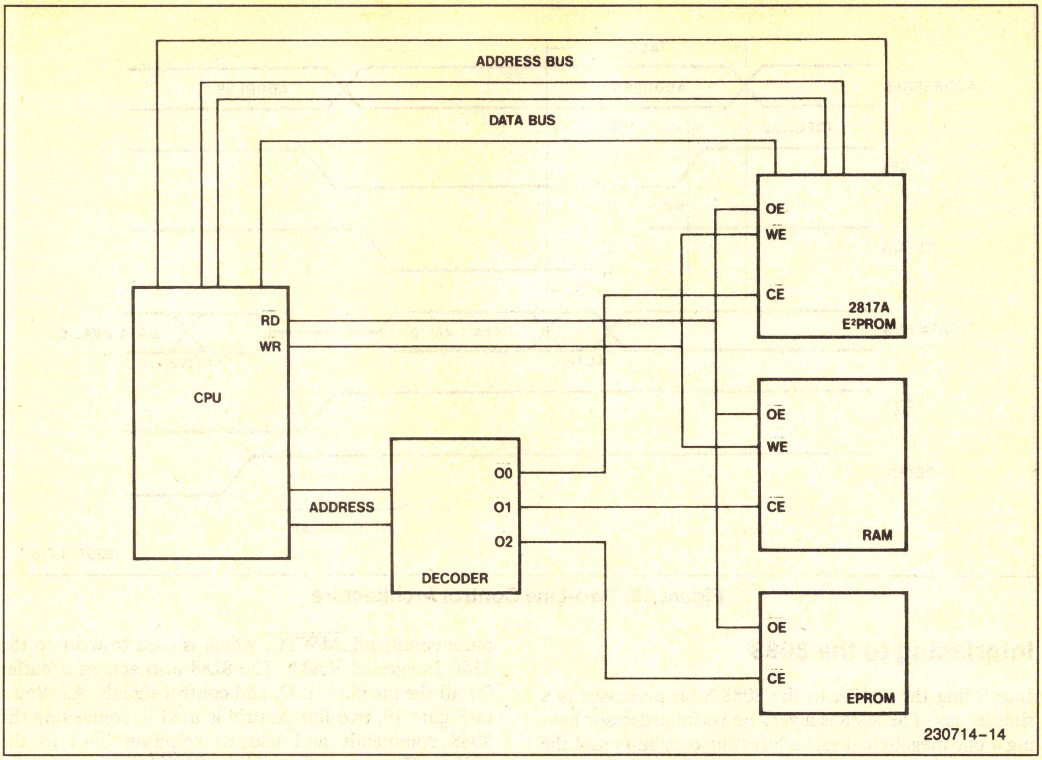

ADDRESS BUS
DATA BUS
CPU
RD
WR
ADDRESS
DECODER
O0
O1
O2
OE
WE
CE
2817A
E²PROM
OE
WE
CE
RAM
OE
CE
EPROM
230714-14

Figure 16. Basic Microprocessor Interface

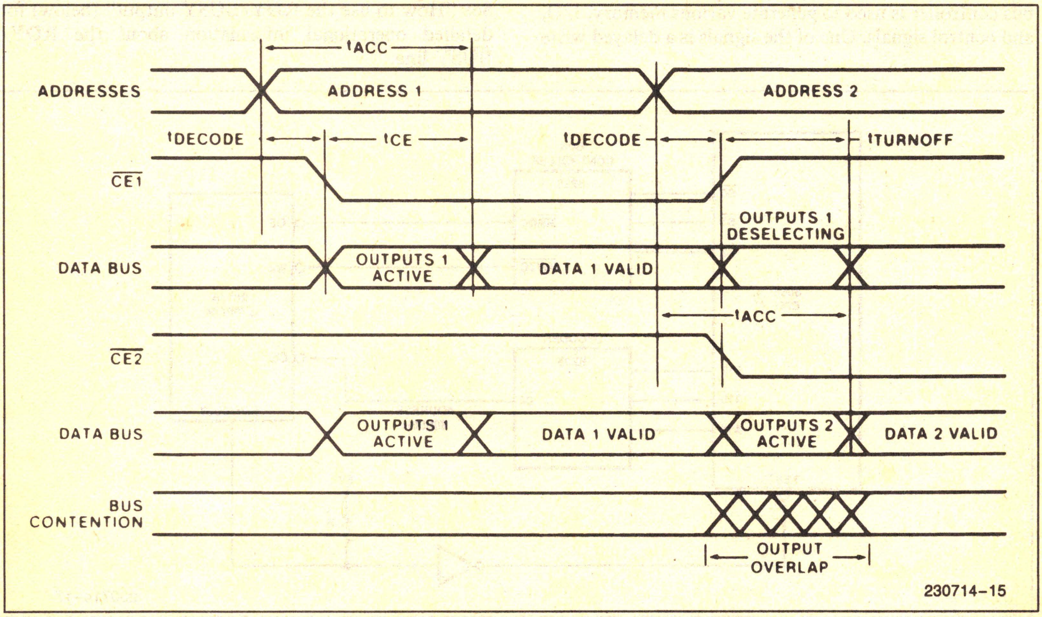

tACC
ADDRESSES
ADDRESS 1
ADDRESS 2
tDECODE
tCE
tDECODE
tTURNOFF
CE1
OUTPUTS 1 DESELECTING
DATA BUS
OUTPUTS 1 ACTIVE
DATA 1 VALID
tACC
CE2
DATA BUS
OUTPUTS 1 ACTIVE
DATA 1 VALID
OUTPUTS 2 ACTIVE
DATA 2 VALID
BUS CONTENTION
OUTPUT OVERLAP
230714-15

Figure 17. Single-Line Control and Bus Contention

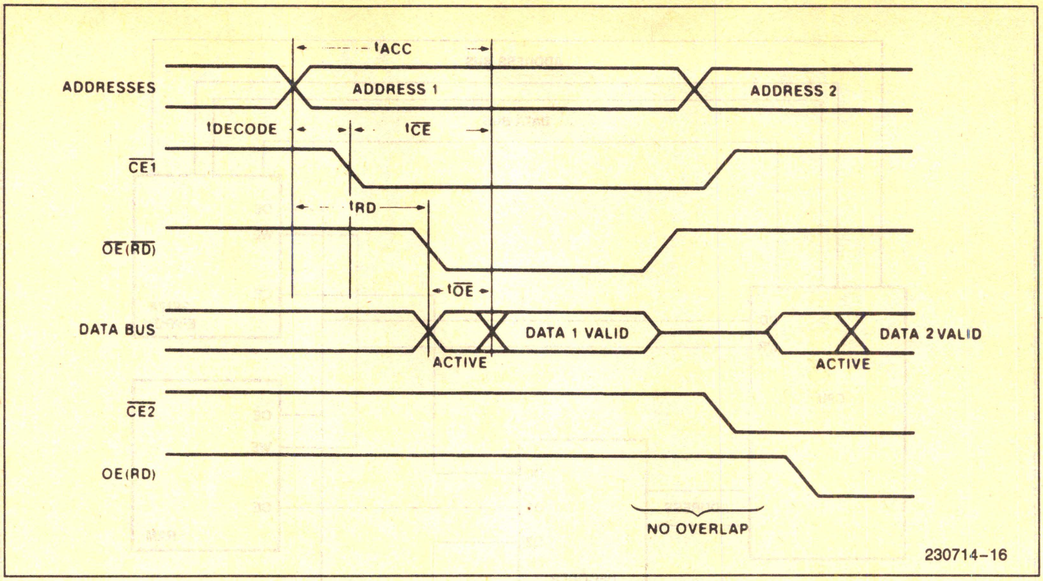

tACC
ADDRESSES
ADDRESS 1
ADDRESS 2
tDECODE
tCE
CE1
tRD
OE(RD)
tOE
DATA BUS
DATA 1 VALID
DATA 2 VALID
ACTIVE
ACTIVE
CE2
OE(RD)
NO OVERLAP
230714–16

Figure 18. Two-Line Control Architecture

Interfacing to the 8088

Interfacing the 2817A to the 8088 8-bit processor is a simple task. The 8088 is a very powerful processor having a one megabyte direct addressing capability and the 8086 instruction set. Figure 19 shows the interface used on the 2817A/8088 applications demo board. The 8288 bus controller is used to generate various memory, I/O, and control signals. One of the signals is a delayed write pulse command, $\overline{\text{MWTC}}$, which is used to write to the 2186 Integrated RAM. The 8288 also acts as a buffer for all the memory, I/O, and control signals. As shown in Figure 19, two-line control is used in connecting the 8088 commands and address selection lines to the 2817A. The status of the RDY/$\overline{\text{BUSY}}$ line is polled via the 8088's $\overline{\text{TEST}}$ input by using the WAIT instruction. See "How to use the RDY/$\overline{\text{BUSY}}$ output" (below) for detailed operational information about the RDY/$\overline{\text{BUSY}}$ line.

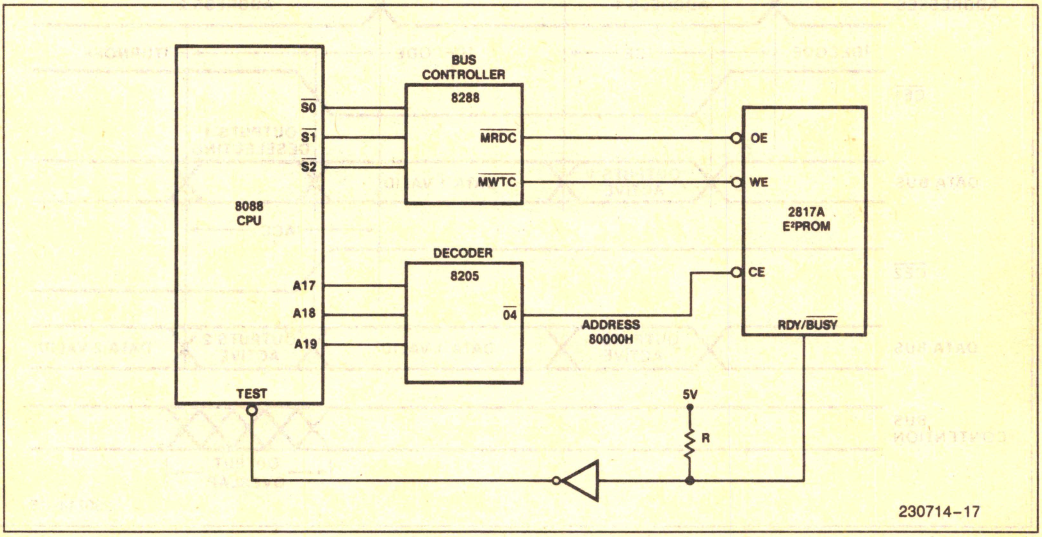

BUS CONTROLLER
8288
S0
S1
S2
MRDC
MWTC
8088 CPU
OE
WE
2817A E²PROM
DECODER
8205
A17
A18
A19
04
ADDRESS 80000H
CE
RDY/BUSY
TEST
5V
R
230714–17

Figure 19. 2817A Interface to the 8088

DESIGN CONSIDERATIONS

How to Use the RDY/$\overline{\text{BUSY}}$ Output

The 2817A has a RDY/$\overline{\text{BUSY}}$ output that indicates when a write operation is in progress and when the 2817A is ready for access. The RDY/$\overline{\text{BUSY}}$ line goes low when a write operation starts and goes back high when the operation is completed. The system CPU can poll this output to determine when another byte can be written, or can use the output as an interrupt to notify the CPU when the current write operation has been completed.

Polled mode is usually the easiest interface to design. It is a good choice as long as the CPU can afford to wait while a byte is being written into the 2817A. In systems where the CPU must continue processing during the 20 milliseconds it takes to complete a byte write operation, an interrupt mode should be used.

Polled Methods

A polled mode can be used whenever it is not necessary for the CPU to be constantly processing while an E^{2}PROM byte write operation is taking place. An example is the remote upgrade of a system's software over the telephone. The service center calls a customer and informs him that a new software package is available for the customer's system and is ready for transmission over the telephone. The customer connects the system to the phone line, either via an acoustic coupler or a direct connection, and waits about 40 seconds (see section on Fast Array Programming) while the new software package is being sent. During this time the only task the CPU is likely to have is the supervision of the downloading operation, so it can afford to wait while data is being written into E^{2}PROM. The user's system now has the latest firmware package, received quickly and inexpensively over the phone, and good for another year or so until the next upgrade.

Polled mode is usually done by connecting the RDY/$\overline{\text{BUSY}}$ output to the CPU data bus via a three-state buffer as shown in Figure 20. (If desired, the rising edge of the RDY/$\overline{\text{BUSY}}$ signal could be used to set a positive edge-triggered flip-flop.) By polling the E2 RDY port the CPU can determine when the 2817A is ready for a read cycle or another write cycle. If any of the Intel I/O port devices (8155, 8255, 8355, or 8755A) are being used in the system, the RDY/$\overline{\text{BUSY}}$ output can be connected to one of the input ports of one of these devices.

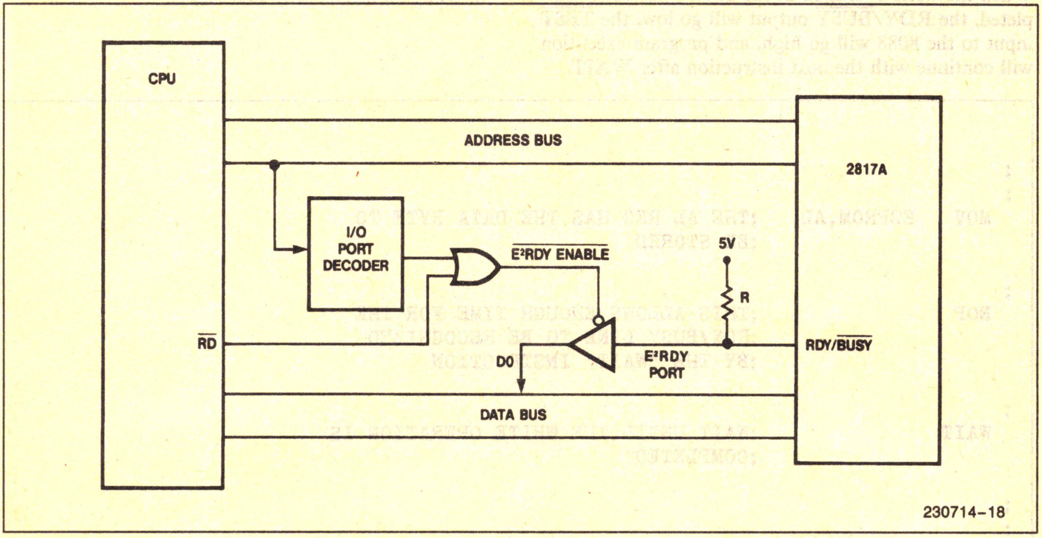


Figure 20. Polled Mode: Using an I/O Input Port to Poll the RDY/$\overline{\text{BUSY}}$ Output

Polled mode for the 8086/8088 microprocesor family is particularly easy using the TEST input and the WAIT instruction. This method is used on the 2817A/8088 demo board. The mardware hookup is shown in Figure 19.

In the 2817A/8088 demo board design a polled method was chosen for its hardware and software simplicity. The hardware consists of an inverter between the RDY/BUSY output and the TEST input of the 8088. In the software, writing to the 2817A simply requires a MOV instruction, and a NOP and a WAIT instruction, as below:

The MOV instruction writes the data byte contained in the AL register to the 2817A. The 2817A latches the byte's address on the falling edge of the WE signal and latches the data on the rising edge of WE. Inside the 2817A the write operation begins, while externally the RDY/BUSY output goes low. The inverted value to the 8088 TEST input is a "high". When the 8088 starts to execute the WAIT instruction the CPU will poll the TEST input. The short delay caused by the NOP instruction insures that the TEST input will be high when the wait instruction is executed. Otherwise, the TEST input would be sampled immediately after the write command (MWTC) goes inactive high. As long as the TEST input is high the 8088 will remain in wait state. When the write operation in the 2817A has been completed, the RDY/BUSY output will go low, the TEST input to the 8088 will go high, and program execution will continue with the next instruction after WAIT.

Interrupt Methods

Interrupt mode is desirable when data or parameters need to be stored at irregular and relatively frequent intervals, and the CPU must be constantly processing. ("Relatively" meaning not so frequent as to exceed the write endurance of the E^{2}PROM). With interrupt mode, as implemented in this application note, not only is the CPU's processing time not significantly affected by the E^{2}PROM write cycles, but the user's main program does not have to worry about checking on the E^{2}PROM to see if a given write cycle is done, nor do any status flags have to be monitored. The user program need only write the data to be stored in E^{2}PROM to a RAM buffer table. The status and interrupt subroutines do the rest.

For the 8088, and 8259A Programmable Interrupt Controller is used to handle interrupt signals. The 8259A can itself handle up to 8 interrupt lines: each line is separately maskable and priority handling is dynamically programmable. The 2817A's RDY/BUSY output can be directly connected to any one of the 8259A's interrupt inputs. The edge-triggered mode is used to trigger the interrupt input to the 8259A when the RDY/BUSY output returns high upon completion of the write operation. The schematic diagrams in Figure 21 and Appendix B show the electrical connections for using an 8259A with 8088 CPU.

```
;
;
  MOV    E2PROM,AL     ;THE AL REG HAS THE DATA BYTE TO
                       ;BE STORED

;
  NOP                  ;THIS ALLOWS ENOUGH TIME FOR THE
                       ;RDY/BUSY LINE TO BE RECOGNIZED
                       ;BY THE "WAIT" INSTRUCTION

;
  WAIT                 ;WAIT UNTIL THE WRITE OPERATION IS
                       ;COMPLETED

;
;
```

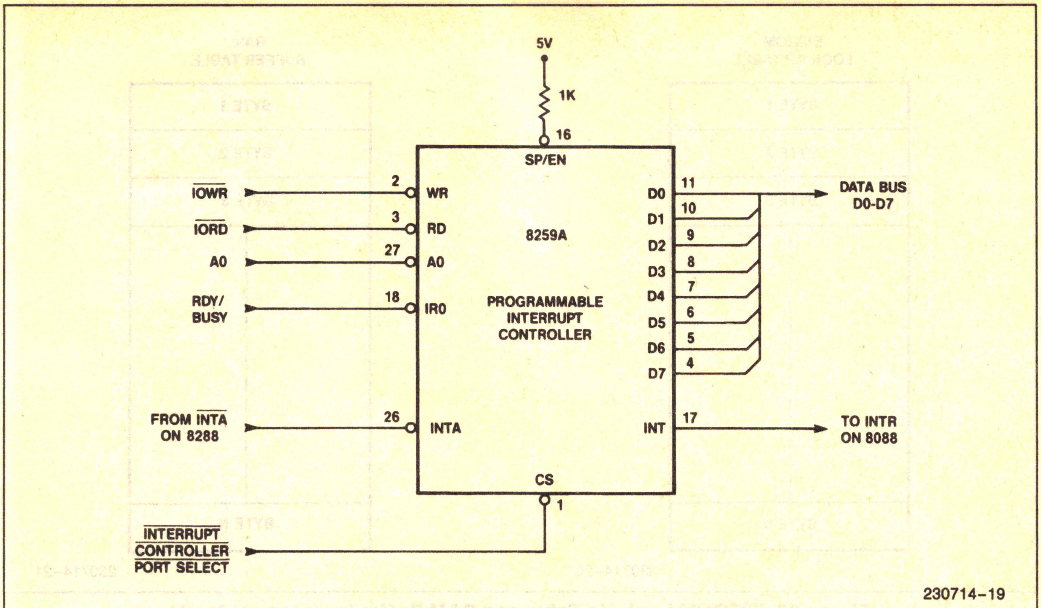

5V
1K
16
SP/EN
IOWR
2
WR
IORD
3
RD
A0
27
A0
RDY/
BUSY
18
IR0
8259A
PROGRAMMABLE
INTERRUPT
CONTROLLER
D0
D1
D2
D3
D4
D5
D6
D7
11
10
9
8
7
6
5
4
DATA BUS
D0-D7
FROM INTA
ON 8288
26
INTA
INT
17
TO INTR
ON 8088
CS
1
INTERRUPT
CONTROLLER
PORT SELECT
230714-19

Figure 21. Interrupt Mode: 8259A in an 8088 System

Interrupt Subroutine

The following is an example of how to implement an interrupt-driven system in software.

A section of the system RAM is organized exactly like the look-up table in the 2817A E^{2}PROM. In this example the table consists of ten bytes (see Figure 22).

Each time the user program receives or produces data to be stored in E^{2}PROM, all the user program has to do is write the desired data into the corresponding locations in the RAM buffer table, then call a short status subroutine. The transfer of data to the E^{2}PROM and the monitoring of the write operation are done by the status and interrupt subroutines.

The status subroutine checks if an E^{2}PROM write operation is in progress, which would mean that the interrupt subroutine is already in the process of transferring data from RAM to E^{2}PROM. If so, then nothing else needs to be done. If no transfer is in process, then the status routine will start an E^{2}PROM write operation by looking for the first byte of data in the RAM buffer table that is not equal to its corresponding byte of data in the E^{2}PROM table. When that write operation is complete, the interrupt subroutine is called, which checks for any more data to be written to E^{2}PROM. The interrupt subroutine is called after each write operation is completed until all the new data in the RAM buffer table has been transferred to E^{2}PROM.

The flowcharts for these subroutines are shown in Figures 23 and 24, and the software implementation for the 2817A/8088 demo board is shown in Appendix A. The code to initialize the 8259A Programmable Interrupt Controller is also given in Appendix A.

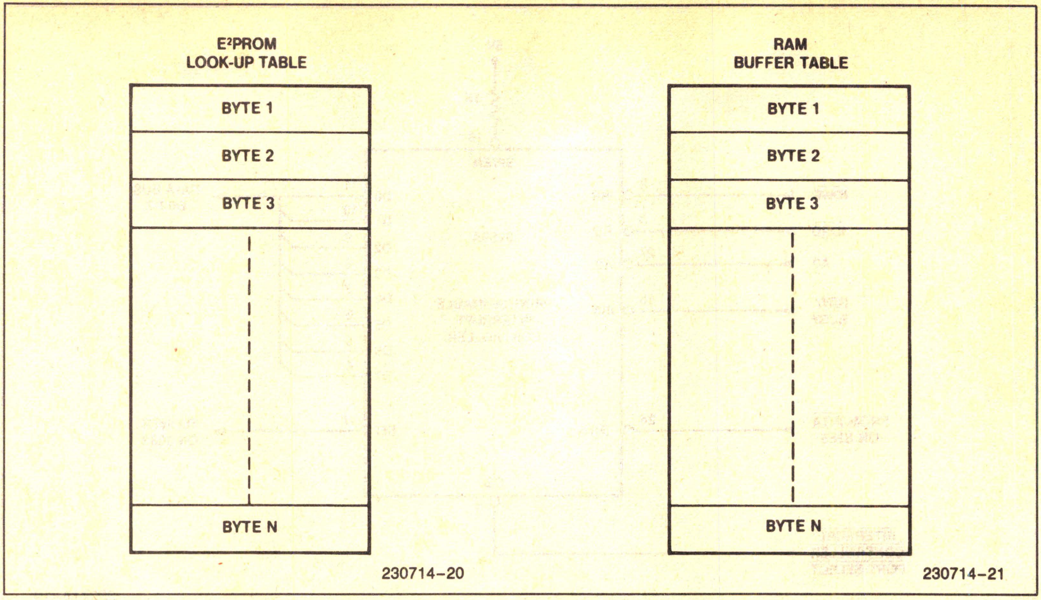

E²PROM
LOOK-UP TABLE
BYTE 1
BYTE 2
BYTE 3
BYTE N
230714-20
RAM
BUFFER TABLE
BYTE 1
BYTE 2
BYTE 3
BYTE N
230714-21

Figure 22. E²PROM Look-Up Table and RAM Buffer for Interrupt Mode

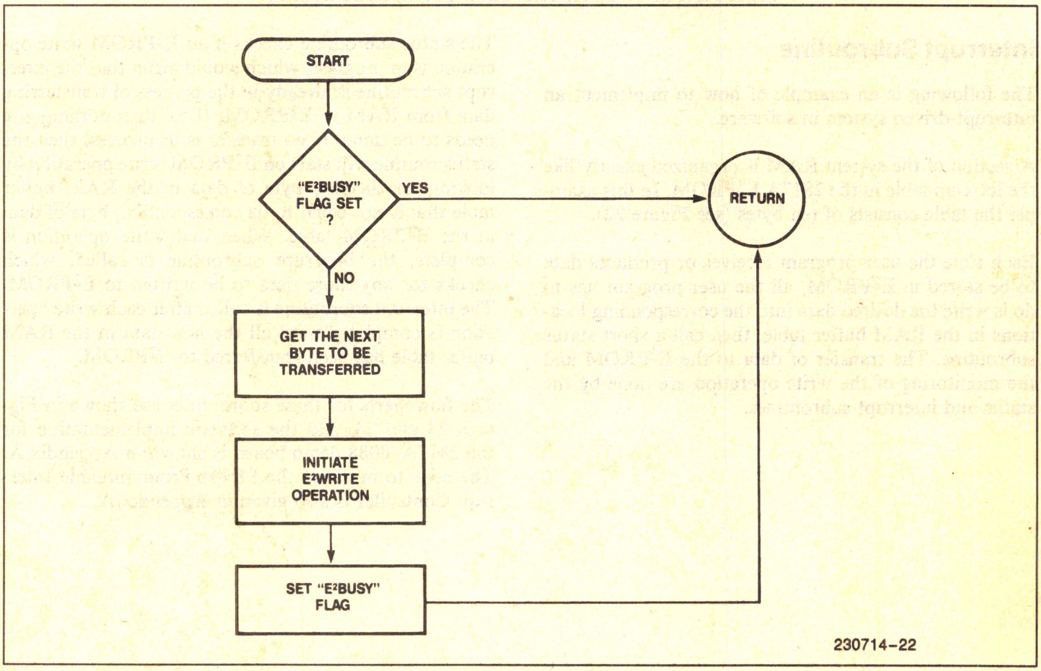

START
"E²BUSY"
FLAG SET
?
YES
NO
RETURN
GET THE NEXT
BYTE TO BE
TRANSFERRED
INITIATE
E²WRITE
OPERATION
SET "E²BUSY"
FLAG
230714-22

Figure 23. Status Subroutine

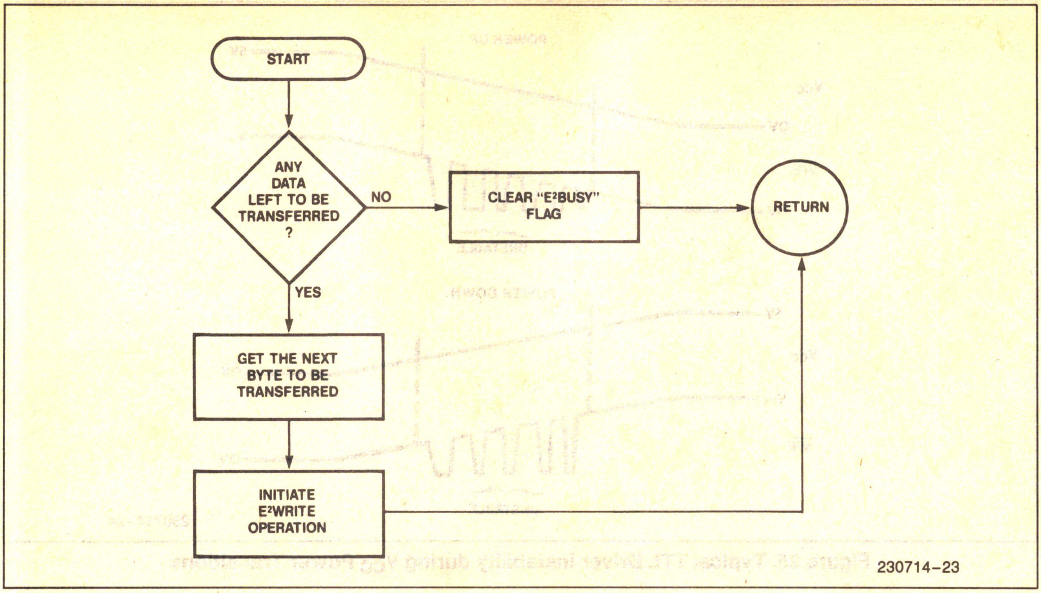

START
ANY DATA LEFT TO BE TRANSFERRED ?
NO
YES
CLEAR "E²BUSY" FLAG
RETURN
GET THE NEXT BYTE TO BE TRANSFERRED
INITIATE E²WRITE OPERATION
230714-23

Figure 24. Interrupt Subroutine

When first initializing this look-up table, each byte in the E^2PROM table is set equal to its corresponding byte in the RAM buffer table. Any subsequent changes to the RAM buffer table are easily detected by the status and interrupt subroutines by comparing each pair of corresponding locations in the two tables.

Combining Multiple RDY/$\overline{\text{BUSY}}$ Outputs in a 2817A Array

The 2817A's RDY/$\overline{\text{BUSY}}$ pin is an open-drain output, so multiple RDY/$\overline{\text{BUSY}}$ outputs can be or-tied together. The value of the pull-up resistor for the RDY/$\overline{\text{BUSY}}$ output can be calculated by the following formula:

$$R(\text{pullup}) = \frac{4.6\text{V}}{2.1\text{ mA} - I_{IL}}$$

where I_{IL} (or I_{LI}) is the total V_{IL} input current of all device inputs connected to RDY/$\overline{\text{BUSY}}$.

There is no limit to the number of RDY/$\overline{\text{BUSY}}$ outputs that can be or-tied together.

Write Protection during Power Transitions

The 2817A has an on-chip write protection circuit that prevents a write operation from occurring when V_{CC} is below 3.5V.

All E^2PROMs need inadvertent write protection, either internally or externally, when system power is being turned on or off. Since an E^2PROM can be programmed in-circuit, the possibility exists that it can be programmed accidentally when system power is removed. This is because the same control signals, $\overline{\text{CE}}$ and $\overline{\text{WE}}$, that can normally initiate a write operation could also trigger the write mode as system power is failing. As the 5V supply to the system falls, the system components will become unpredictable, and $\overline{\text{CE}}$ and $\overline{\text{WE}}$ may be spuriously driven active low as shown in Figure 25. To prevent a write operation from accidentally occurring when system power is dropping, an on-chip write protection circuit is needed to hold inactive at least one of the control signals. The same protection is needed when V_{CC} is rising from 0V to 5V as shown in Figure 25.

Alternate RDY/$\overline{\text{BUSY}}$ Interfacing Methods

There are many ways to interface the 2817A to a microprocessor using the RDY/$\overline{\text{BUSY}}$ output. The polled and interrupt-driven modes discussed in this application note are the easiest and most commonly used methods. These methods are compatible with the con-

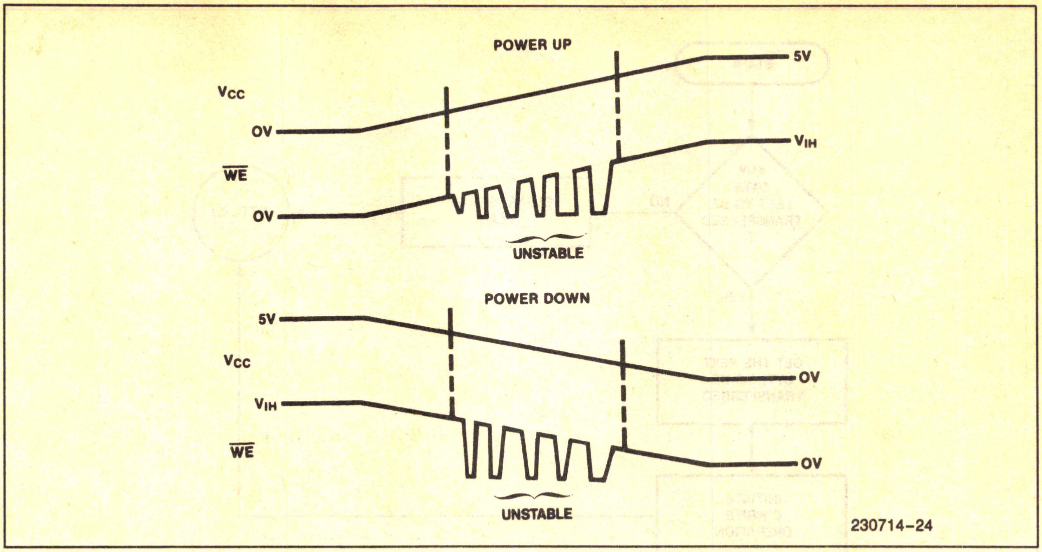


Figure 25. Typical TTL Driver Instability during V_{CC} Power Transitions

cept of an "intelligent" E^{2}PROM which allows write operations to be done without holding up the microprocessor.

When first looking at the 2817A it might seem as if the RDY/$\overline{\text{BUSY}}$ line should be connected directly to a microprocessor's "ready" input since the signals have similar names. There are certain timing and operational considerations, however, that make this method more difficult to design into a system than the interrupt or polled modes described earlier. These considerations are discussed below.

It is possible to use the RDY/$\overline{\text{BUSY}}$ output to hold up the microprocessor until the write operation is completed. This involves the insertion of wait states into the microprocessor's instruction cycle. For the 8085A and the 8088/8086, wait states occur when the READY input is brought inactive low. This type of interface would be implemented by connecting the 2817A's RDY/$\overline{\text{BUSY}}$ output to the microprocessor's READY input. At first this method might seem even simpler than polled mode, but a closer examination shows that this is not true.

The first consideration is the discrepancy between the timing of the 2817A's RDY/$\overline{\text{BUSY}}$ signal and the "ready" input of a microprocessor. Taking the 8088 as an example, the READY input is required to be low (if wait states are desired) about the same time that the 8088's write signal goes low. The top three signals in Figure 26 show this requirement. (The READY input shown is that of the 8284A clock generator. The output of the 8284A is then normally connected to the READY pin on the 8088. The $\overline{\text{AMWC}}$ write signal is the output of the 8288 bus controller which is used with the 8088 in MAX mode.) As shown by the bottom signal in Figure 26, the 2817A's RDY/$\overline{\text{BUSY}}$ output does not go low until after the $\overline{\text{WE}}$ input signal goes back high.

Although this timing discrepancy is not critical, the implications for any given system (and the microprocessor used) must be examined carefully before this method of interfacing is used.

Another consideration that must be taken into account is the possibility of two or more sequential write cycles being done by the microprocessor. An 8088 string operation, for example, would allow the CPU to do one bus write cycle after another without any other intervening cycles. The 2817A would be able to respond successfully to the first write cycle, but not the second. The following would happen:

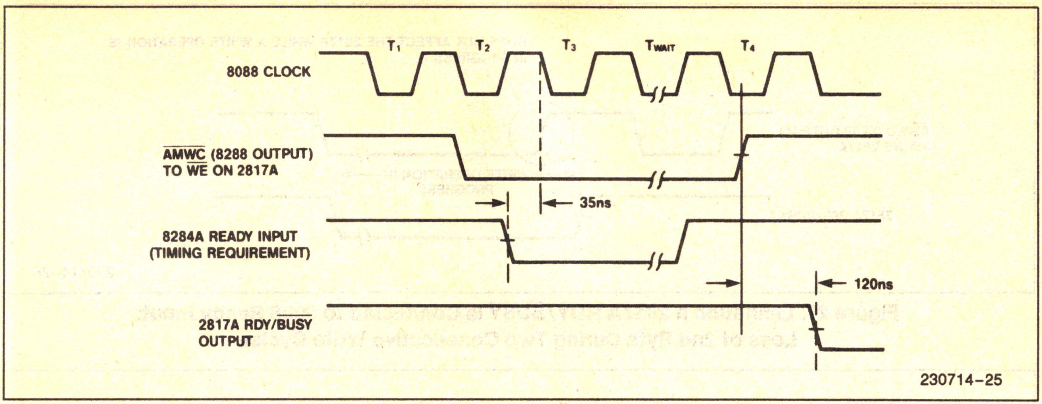

T₁
T₂
T₃
TWAIT
T₄
8088 CLOCK
$\overline{\text{AMWC}}$ (8288 OUTPUT) TO $\overline{\text{WE}}$ ON 2817A
35ns
8284A READY INPUT (TIMING REQUIREMENT)
120ns
2817A RDY/$\overline{\text{BUSY}}$ OUTPUT
230714-25

Figure 26. 8088 Ready Input Timing Requirement

Upon seeing the rising and falling edges of the write pulse during the first write cycle, the 2817A would start an E²PROM write operation. The RDY/$\overline{\text{BUSY}}$ output would go low 75 ns after the rising edge of the write pulse as shown in Figure 27. The RDY/$\overline{\text{BUSY}}$ signal would not hold up the CPU until the following write cycle. While the first byte write operation is in progress the 2817A is not affected by any of the input signals and the data bus is in a high impedance state. When this write operation is completed and the RDY/$\overline{\text{BUSY}}$ signal returns high, the CPU will complete its second write cycle. The 2817A will not have recognized the second write cycle, however, because it did not see the $\overline{\text{WE}}$ signal fall.

The direct connection of the 2817A's RDY/$\overline{\text{BUSY}}$ to the 8088's (or any other microprocessor's) READY input would thus require that no software be written that might cause two or more consecutive write cycles to occur.

The design of the 2817A's on-chip intelligence gives the 2817A maximum flexibility in interfacing to microprocessor-based systems. While the interrupt-driven and polled interface modes are two relatively simple (and widely used) approaches, many other methods are possible. In each case the timing specifications should be studied to insure that the timing requirements of all devices involved are met.

E²PROM Mapping Techniques

Inherent in the design of all E²PROM's is a 10,000 write cycle per bye limitation. As an example of the allowable write cycle frequency, all 2048 bytes in one 2817A could be written three times each day, 365 days a year, for 10 years before exceeding guaranteed limits.

The E²PROM is not designed to be written to as often as RAM memory. Mapping techniques such as the ones shown here, however, allow higher write cycle frequencies than normal to be used.

Electronic Message Storage Applications

A memory usage mapping technique such as the one used in the Electronic Message Storage Demo described in this applications note can more evenly distribute the number of write cycles to each byte in the E²PROM array, thus stretching the usable life of the E²PROM. In message storage, if a pointer is used to indicate the location of the next empty message block, that pointer has to be re-written into an E²PROM memory location each time a message is stored in the E²PROM memory. That particular pointer storage location could reliably be used 10,000 times and still be guaranteed to remain within specification. If a system using this method had one 2817A for message storage, it could store 3 messages per day, 365 days a year for 10 years.

In the Electronic Message Storage Demo, no pointer is stored each time a message is stored. Instead, the 2817A is partitioned into a number of fixed-length message block spaces. Empty blocks have the byte "FF" in the lst location, as shown in Figure 28. Thus, whenever a message is to be stored, the 2817A is searched for a block with an "FF" in the 1st location. Using this method, if the 2817A in a message storage system is divided into 20 100-byte blocks (2817A = 2K bytes), up to 60 messages can be stored each day, 365 days a year, for 10 years. In this example, for every additional 2817A in the system, 60 more messages of this size could be stored each day.

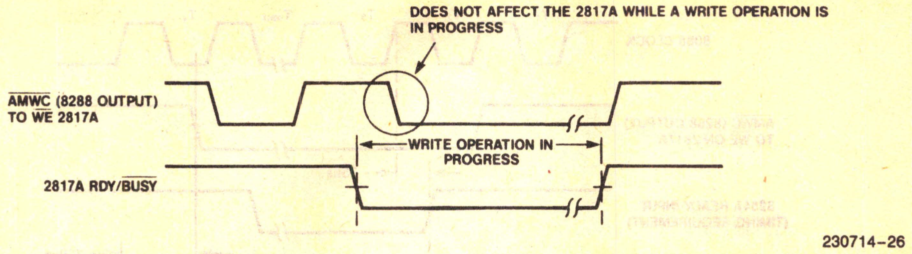
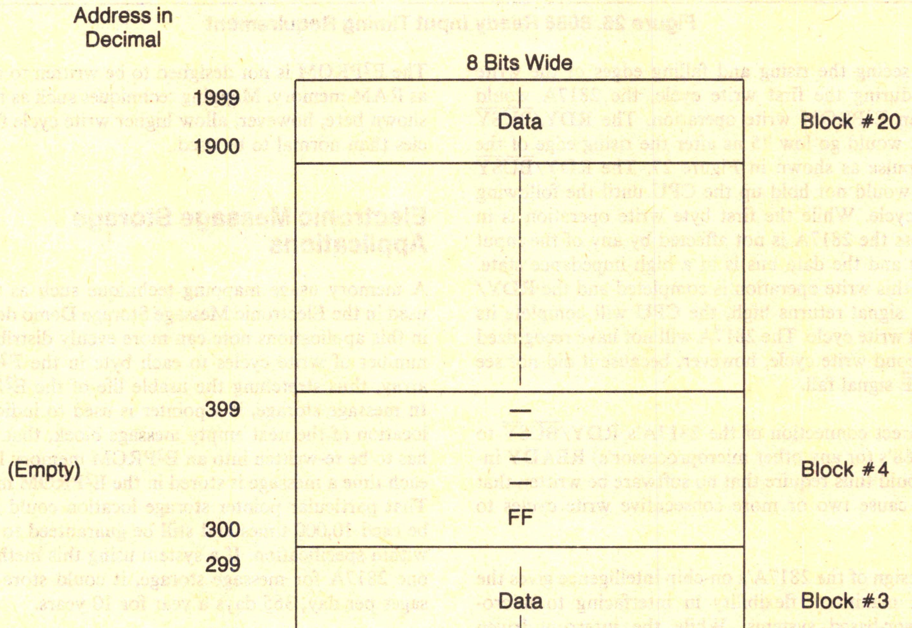
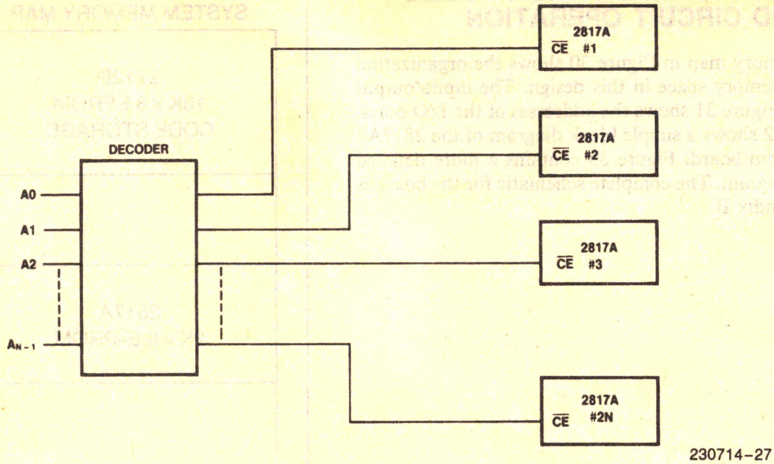

DOES NOT AFFECT THE 2817A WHILE A WRITE OPERATION IS IN PROGRESS
$\overline{\text{AMWC}}$ (8288 OUTPUT) TO $\overline{\text{WE}}$ 2817A
WRITE OPERATION IN PROGRESS
2817A RDY/$\overline{\text{BUSY}}$
230714-26

Figure 27. Limitation if 2817A RDY/$\overline{\text{BUSY}}$ is Connected to 8088 Ready Input: Loss of 2nd Byte During Two Consecutive Write Cycles


Address in Decimal
8 Bits Wide
1999
Data
Block #20
1900
399
(Empty)
Block #4
FF
300
299
Data
Block #3
200
199
Data
Block #2
100
99
(Empty)
Block #1
FF
0
2817A Memory Map

In this example, Blocks 1 and 4 are empty while blocks 2, 3, and 20 have messages.

Figure 28. Message Storage Technique Example



NOTES:

1. Addresses A_0-A_{N-1} are connected to decoder for an array of 2^N devices.
2. All RDY/$\overline{\text{BUSY}}$ outputs are tied together.
3. 2817A address inputs A0–A10 are connected to system addresses A_N-A_{N+10}.

Figure 29. Fast Array Programming

Fast Array Programming

In large memory storage applications where fast write times are important, fast array programming can provide a solution. The total write time of any block of data to the array is reduced by a factor equal to the number of 2817As in the array. For example, an 8K byte block of data can be stored in an array of sixteen 2817As (32K x 8 of E^2PROM memory) in $1/16$ the normal time, that is, 8192×10 milliseconds $\times 1/16 =$ 5.12 seconds. This is particularly useful in designs that require a large amount of non-volatile memory to be used in harsh environments. No additional hardware or software is required: the memory address decoder is simply connected according to the schematic diagram in Figure 29. The result is a decoding of the least significant address lines rather than the most significant address lines.

To transfer data to the E^2PROM memory, a series of high-speed, system write cycles are performed, one immediately after the other, to the E^2PROM memory array. Each 2817A will internally perform a write operation using one of the successive bytes. For example, if the array in Figure 29 had 64 2817As, then 64 bytes would be written in each burst of high-speed write cycles. The total programming time for each 64-byte block would be the same as for one 2817A: 10 milliseconds.

Effectively, the total time needed to write a block of data into the array shown in Figure 29 is equal to:

$$\text{Total Write Time} = \frac{\text{write time (10 ms)} \times \text{\# of bytes to be stored}}{\text{\# of 2817A devices in the array}}$$

The more 2817As there are in the array, the shorter the write time for a given block of data. For example, writing a block of 16K bytes to an array of 32 2817As (64K bytes of E^2PROM) would take 5.12 seconds (25.6K bits per second). A more significant application would be a $1/4$ megabyte E^2PROM array (128 2817As). Writing 128K bytes to such an array would take only 10.2 seconds, which is 103K bits/second.

2817A/8088 APPLICATIONS DEMO BOARD CIRCUIT OPERATION

The memory map in Figure 30 shows the organization of the memory space in this design. The input/output map in Figure 31 shows the addresses of the I/O ports. Figure 32 shows a simple block diagram of the 2817A/8088 demo board. Figure 33 contains a more detailed block diagram. The complete schematic for the board is in Appendix B.

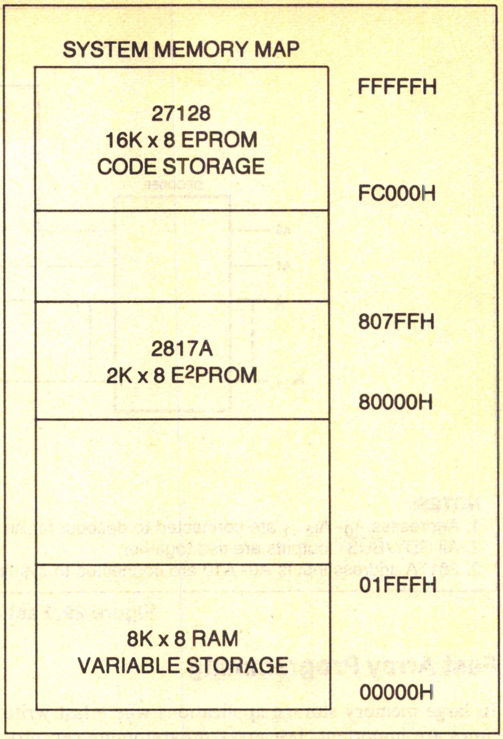
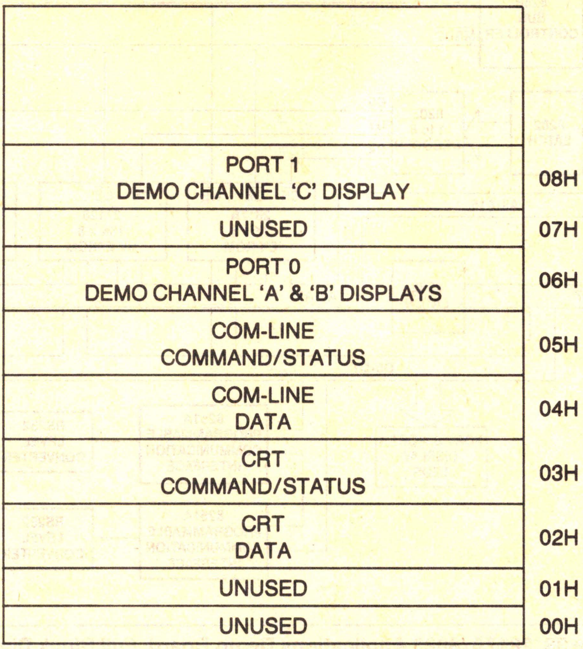

SYSTEM MEMORY MAP
27128
16K x 8 EPROM
CODE STORAGE
FFFFFH
FC000H
2817A
2K x 8 E2PROM
807FFH
80000H
01FFFH
8K x 8 RAM
VARIABLE STORAGE
00000H

Figure 30. 2817A/8088 Applications Demo Board

INPUT/OUTPUT PORT MAP



PORT 1 DEMO CHANNEL 'C' DISPLAY	08H
UNUSED	07H
PORT 0 DEMO CHANNEL 'A' & 'B' DISPLAYS	06H
COM-LINE COMMAND/STATUS	05H
COM-LINE DATA	04H
CRT COMMAND/STATUS	03H
CRT DATA	02H
UNUSED	01H
UNUSED	00H

Figure 31. 2817A/8088 Applications Demo Board

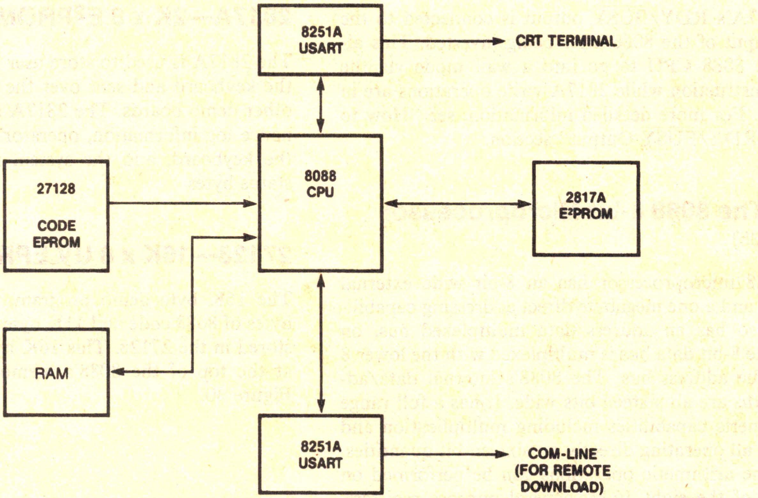

8251A
USART
CRT TERMINAL
27128
CODE
EPROM
8088
CPU
2817A
E²PROM
RAM
8251A
USART
COM-LINE
(FOR REMOTE
DOWNLOAD)

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Figure 32. 2817A/8088 Applications Demo Board Simplified Block Diagram

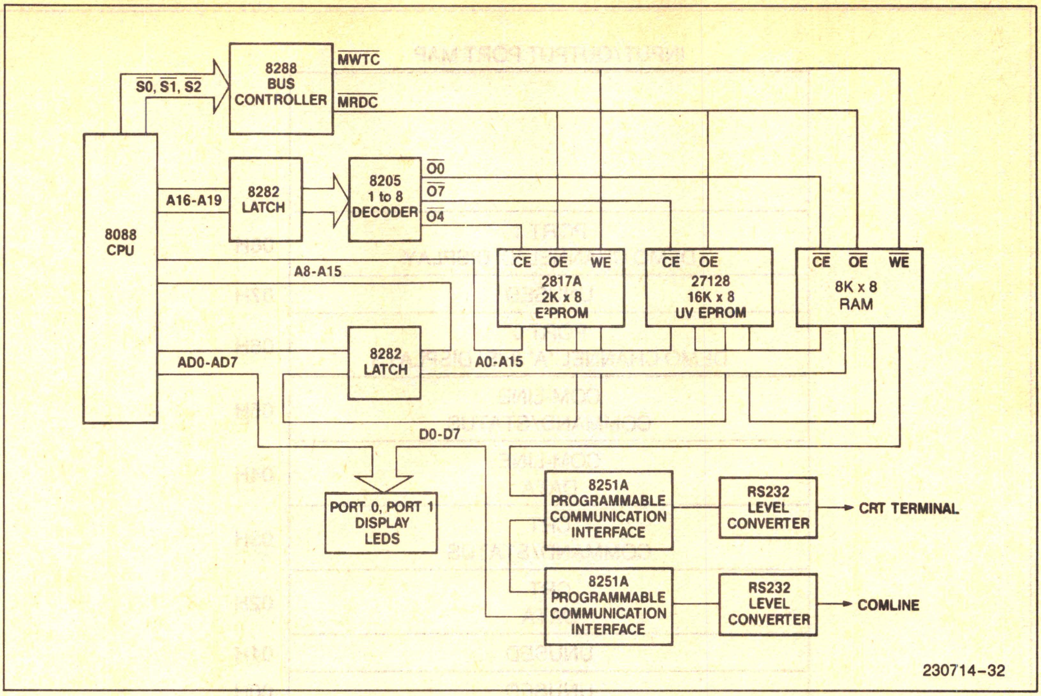
$\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{S2}}$
8288
BUS
CONTROLLER
$\overline{\text{MWTC}}$
$\overline{\text{MRDC}}$
8088
CPU
A16-A19
8282
LATCH
8205
1 to 8
DECODER
$\overline{\text{O0}}$
$\overline{\text{O7}}$
$\overline{\text{O4}}$
A8-A15
$\overline{\text{CE}}$ $\overline{\text{OE}}$ $\overline{\text{WE}}$
2817A
2K x 8
E^{2}PROM
$\overline{\text{CE}}$ $\overline{\text{OE}}$
27128
16K x 8
UV EPROM
$\overline{\text{CE}}$ $\overline{\text{OE}}$ $\overline{\text{WE}}$
8K x 8
RAM
AD0-AD7
8282
LATCH
A0-A15
D0-D7
PORT 0, PORT 1
DISPLAY
LEDS
8251A
PROGRAMMABLE
COMMUNICATION
INTERFACE
RS232
LEVEL
CONVERTER
CRT TERMINAL
8251A
PROGRAMMABLE
COMMUNICATION
INTERFACE
RS232
LEVEL
CONVERTER
COMLINE
230714-32

Figure 33. 2817A/8088 Applications Demo Board: Full Block Diagram

2817A Interface Circuitry: The RDY/$\overline{\text{BUSY}}$ Output (Figures 35 and 36)

The 2817A's RDY/$\overline{\text{BUSY}}$ output is connected to the $\overline{\text{TEST}}$ input of the 8088 after being inverted. This allows the 8088 CPU to go into a wait mode via the WAIT instruction while 2817A write operations are in progress. For more detailed information, see "How to Use the RDY/$\overline{\text{BUSY}}$ Output" section.

CPU: The 8088 8-bit Microprocessor (Figure 35)

The 8088 microprocessor has an 8-bit wide external data bus and a one megabyte direct addressing capability. It also has an address/data multiplexed bus, on which the 8-bit data bus is multiplexed with the lower 8 bits of the address bus. The 8088's internal data/address paths are all sixteen bits wide. It has a full range of arithmetic capabilities including multiplication and division, all operating directly on sixteen-bit quantities. All of the arithmetic operations can be performed on any one of the eight 16-bit general purpose registers. The 8088 also has string operation commands which allow high-speed processing of large data blocks.

MEMORY

2817A—2K x 8 E^{2}PROM (Figure 36)

The 2817A is used to store user messages entered from the keyboard and sent over the comline channel from other demo boards. The 2817A also stores the maintenance log information, operator's initials entered from the keyboard, and the system re-configuration demo status bytes.

27128—16K x 8 UV EPROM (Figure 38)

The 16K byte demo program, which consists of 5K bytes of 8088 code and 11K bytes of ASCII text data, is stored in the 27128. This 16K byte EPROM is located at the top of the 8088's memory space as shown in Figure 30.

Demo Channel Display LED Ports
(Figure 40)

Two 74LS374 8-bit D flip-flop devices are used to store the system re-configuration demo status bits for display with LEDs. Output ports 0 and 1 are used to control nine light-emitting diodes. The output states of these bits are determined by the system re-configuration look-up table in E^{2}PROM (see Figure 14). When the demo board is powered up, the firmware reads the look-up table to determine what states the port bits should be in. These port bits could easily control peripheral channeling between systems and peripheral devices in a computer room. The port bits could also control system parameters such as communications modes, baud rates, display formats, and "soft key" definitions.

8251A Programmable Communications Interface

Hardware (Figure 39)

Baud Rate

The first counter in the 74LS393 is used to generate the 4800 baud rate for the CRT terminal comm(communications)-interface. The baud rate is produced by dividing the PCLK 2.5 MHz clock by 8 to obtain a 312.5 KHz clock. The 2nd 4-bit counter in the 74LS393 is used to generate the 300 baud rate for the Comline comm-interface. This is done by dividing the 312.5 KHz clock by 16 down to 19.5 KHz.

RS232 Level Interface Circuit

A standard RS232 serial line driver and receiver circuit requires ± 12V power supplies to generate the required ± 12V signal levels. To reduce the complexity of operating this demo the RS232 level shifting circuits were designed so that they need only a +5V power supply. These circuits allow the demo board to communicate with any system that has standard RS232 level inputs and outputs. The level shifter circuit shown with the CRT interface, however, will not actively assert a valid logic "0" level when connected to another level shifter exactly like it. To allow two demo boards to communicate with each other the level shifter circuit at the top of Figure 39 has to be modified. For this reason the Comline level shifter at the bottom of Figure 39 is slightly different than the CRT interface level shifter at the top of the figure. This allows the Comline channels of two boards to be connected together so that data can be transferred between demo boards to be ultimately stored in E^{2}PROM.

An example of a circuit that will provide the full RS232 spec + and −12V signal levels is shown in Figure 34.

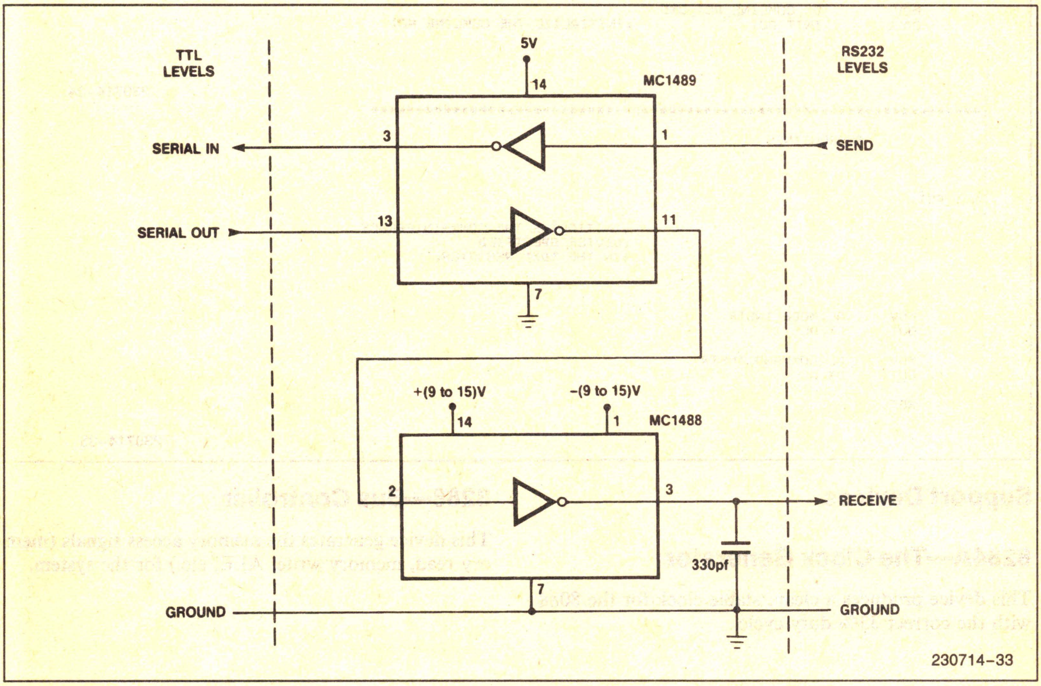

Figure 34. Full Spec TTL to RS232 Level Converter Circuit

8251A Software Initialization

The following software listing shows the procedure used on the 2817A/8088 applications demo to initialize the 8251A Programmable Communication Interface devices.

```
;
;
;
:
:           EQUATES
;
;
MODE_INSTR          EQU         11001111B           ;ASYNCHRONOUS MODE
                                                    ;64X BAUD RATE
                                                    ;8-BIT CHARACTER LENGTH
                                                    ;PARITY DISABLED
                                                    ;2 STOP BITS
;
COMMAND_INSTR       EQU         00100101B           ;TRANSMIT ON
                                                    ;DTR/ = 1
                                                    ;RECEIVE ENABLE


                                                    :NORMAL OP - NO BREAK CHAR
                                                    ;NO ERROR RESET
                                                    ;RTS/ = 0



;
CRT_PCI_CMD                 EQU      03H       ;COMMAND MODE I/O PORT FOR
                                               ;THE CRT TERMINAL PROG'BLE COMM
                                               ;INTERFACE
;
COMLINE_PCI_CMD             EQU      05H       ;COMMAND MODE I/O PORT FOR
                                               ;THE COMLINE USART
;
;


;
;       CODE TO INITIALIZE THE 8251A'S
;
;
        MOV         DX,CRT_PCI_CMD
        CALL        INIT_PCI                   ;INITIALIZE THE CRT COMM-INTERFACE
;
        MOV         DX,COMLINE_PCI_CMD
        CALL        INIT_PCI                   ;INITIALIZE THE COMLINE PCI
;
;
;
;
;************************************************************************
:
:           SUBROUTINES
;
;
:
INIT_PCI:
:
                                               ;INITIALIZE THE COMM-INTERFACE
                                               ;DEVICE SPECIFIED
                                               ;IN THE 'DX' REGISTER.


:
;
        MOV      AL,MODE_INSTR
        OUT      DX,AL
:
        MOV      AL,COMMAND_INSTR
        OUT      DX,AL
;
        RET
;
:
```

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230714-35

Support Devices

8284A—The Clock Generator

This device produces a clean, stable clock for the 8088 with the correct 33% duty cycle.

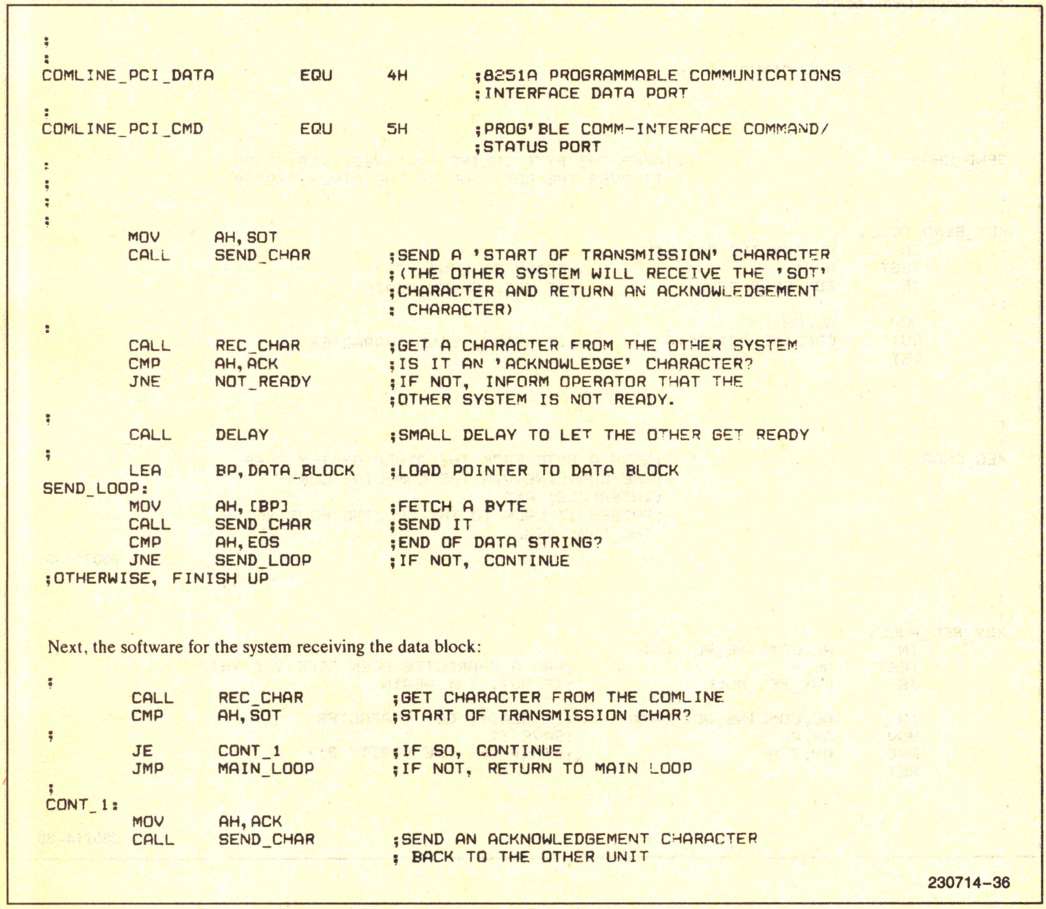
8288—Bus Controller

This device generates the memory access signals (memory read, memory write, ALE, etc.) for the system.

APPENDIX A
SOFTWARE LISTINGS

Routines for Data Transfer Between 2817A/8088 Demo Boards over the 'COMLINE' Communications Interface Channel

This is the routine for the system sending the data block.



```
;
:
COMLINE_PCI_DATA        EQU     4H      ;8251A PROGRAMMABLE COMMUNICATIONS
                                        :INTERFACE DATA PORT
:
COMLINE_PCI_CMD         EQU     5H      ;PROG'BLE COMM-INTERFACE COMMAND/
                                        ;STATUS PORT
:
;
:
:
        MOV     AH,SOT
        CALL    SEND_CHAR       ;SEND A 'START OF TRANSMISSION' CHARACTER
                                ;(THE OTHER SYSTEM WILL RECEIVE THE 'SOT'
                                ;CHARACTER AND RETURN AN ACKNOWLEDGEMENT
                                : CHARACTER)
:
        CALL    REC_CHAR        ;GET A CHARACTER FROM THE OTHER SYSTEM
        CMP     AH,ACK          ;IS IT AN 'ACKNOWLEDGE' CHARACTER?
        JNE     NOT_READY       ;IF NOT, INFORM OPERATOR THAT THE
                                ;OTHER SYSTEM IS NOT READY.
;
        CALL    DELAY           ;SMALL DELAY TO LET THE OTHER GET READY
;
        LEA     BP,DATA_BLOCK   ;LOAD POINTER TO DATA BLOCK
SEND_LOOP:
        MOV     AH,[BP]         ;FETCH A BYTE
        CALL    SEND_CHAR       ;SEND IT
        CMP     AH,EOS          ;END OF DATA STRING?
        JNE     SEND_LOOP       ;IF NOT, CONTINUE
;OTHERWISE, FINISH UP
```

Next, the software for the system receiving the data block:

```
;
        CALL    REC_CHAR        ;GET CHARACTER FROM THE COMLINE
        CMP     AH,SOT          ;START OF TRANSMISSION CHAR?
;
        JE      CONT_1          ;IF SO, CONTINUE
        JMP     MAIN_LOOP       ;IF NOT, RETURN TO MAIN LOOP
;
CONT_1:
        MOV     AH,ACK
        CALL    SEND_CHAR       ;SEND AN ACKNOWLEDGEMENT CHARACTER
                                ; BACK TO THE OTHER UNIT
```

230714-36

```
;
        LEA     BP,DATA_BLK_BUFFER          ;SET POINTER TO DATA BLOCK
                                            ;BUFFER
;
REC_BLK_LOOP:
        CALL    REC_CHAR            ;GET BYTE FROM THE COMLINE
        CMP     AH,EOS              ;END OF DATA BLOCK?
        JE      FINISH_UP           ;IF SO, FINISH UP
        MOV     [BP],AH             ;IF NOT, STORE BYTE AND GET ANOTHER
        JMP     REC_BLK_LOOP
;
FINISH_UP:
;
```

The following are the subroutines used for the software for data transfer between 2817A/8088 Demo boards.

```
;
;               SUBROUTINES
;
;
;
;
SEND_CHAR:                          ;TAKES THE BYTE IN THE 'AH' REG. AND SENDS
                                    ; IT OVER THE COM-LINE TO THE OTHER SYSTEM.
;
;
RDY_SEND_POLL:
        IN      AL,COMLINE_PCI_CMD
        TEST    AL,1                        ;READY TO SEND YET?
        JE      RDY_SEND_POLL               ;IF NOT, CHECK AGAIN
;
        MOV     AL,AH
        OUT     COMLINE_PCI_DATA            ;IF READY, SEND CHARACTER
        RET
;
;
;
;
REC_CHAR:                             ;GETS A BYTE FROM THE OTHER SYSTEM OVER
                                      ;THE COM-LINE(VIA THE COM-LINE COMM-
                                      ;INTERFACE) AND
                                      ;PASSES IT BACK TO THE CALLING ROUTINE IN
                                      ;THE 'AH' REG.
```

230714-37

```
;
;
RDY_REC_POLL:
        IN      AL,COMLINE_PCI_CMD
        TEST    AL,2                        ;HAS A CHARACTER BEEN RECEIVED YET?
        JE      RDY_REC_POLL                ;IF NOT, TRY AGAIN
;
        IN      AL,COMLINE_PCI_DATA         ;IF READY, GET CHARACTER
        MOV     AH,AL                       ;SAVE IT
        AND     AH,7FH                      ;STRIP OFF THE PARITY BIT
        RET
;
;
```

230714-38

Interrupt Mode Software

Status Subroutine

```
;
;
XFER_STATUS_SUBR:                       ;DETERMINES IF AN E2PROM TRANSFER IS
                                        ;ALREADY IN PROGRESS.  IF NOT, THE
                                        ;NEXT BYTE TO BE TRANSFERRED IS
                                        ;WRITTEN TO E2PROM.
;
;
        CMP     E2_BUSY,1               ;E2 WRITE IN PROGRESS?
        JNE     DO_TRANSFER             ;IF NOT, PROCEED
        RET                             ;IF SO, RETURN, SINCE THE NEW DATA
                                        ;IN THE RAM BUFFER TABLE WILL BE
                                        ;DETECTED BY THE INTERRUPT SUBROUTINE
                                        ;AND EVENTUALLY TRANSFERRED TO
                                        ;E2PROM.
;
DO_TRANSFER:
        CALLWRITE_E2_DATA            ;FIND NEXT BYTE TO BE TRANSFERRED AND
                                        ;WRITE IT TO THE E2PROM.
;
;
        RET
;
;
```

230714-39

```
    Interrupt subroutine
;
;
E2_INTERRUPT_SUBROUTINE:                ;EACH TIME AN E2PROM WRITE OPERATION
                                        ;ENDS, CHECK IF THERE ARE ANY MORE
                                        ;BYTES TO BE TRANSFERRED.  IF SO,
                                        ;FETCH THE BYTE AND WRITE IT TO
                                        ;THE E2PROM.
;
        PUSH    DX
        PUSH    AX
        MOV     AL,OCW2
        MOV     DX,PIC_A0_LOW           ;INFORM THE PROGRAMMABLE
        OUT     DX,AL                   ;INTERRUPT CONTROLLER THAT THE
        POP     AX                      ;INTERRUPT HAS BEEN SERVICED
        POP     DX
;
        CALL    WRITE_E2_DATA
        IRET
;
```

230714-40

This subroutine determines if there is any data left to be transferred from the RAM Buffer table to the E^{2}PROM table, and if there is, transfers the next byte.

```
;
;
WRITE_E2_DATA:                           ;CHECK FOR ANY MORE DATA TO BE
                                         ;TRANSFERRED.  IF NONE, CLEAR THE
                                         ;"E2_BUSY" FLAG.  IF ANOTHER BYTE
                                         ;IS TRANSFERRED, SET THE "E2_BUSY"
                                         ;FLAG.
;
;
         PUSH    SI
         PUSH    DI
;
         LEA     SI,RAM_BUFFER_TABLE     ;POINT THE SI REG. TO THE RAM
                                         ;BUFFER TABLE
;
         LEA     DI,E2PROM_TABLE         ;POINT THE DI REG. TO THE E2PROM
                                         ;LOOK-UP TABLE
;
         MOV     CX,10                   ;DEFAULT COUNT = SIZE OF LOOK-UP
                                         ;TABLE
;
REPE     CMPSB                           ;SEARCH FOR ANY NEW DATA BYTES
                                         ;IN THE RAM BUFFER TABLE.
;
         JZ      NO_NEW_DATA             ;IF NO NEW DATA, FINISH UP
;
         ;OTHERWISE, WRITE THE NEW DATA BYTE TO E2PROM
         DEC     SI
         DEC     DI                      ;BACK UP TO THE NEW, UNEQUAL BYTE
;
         MOVSB                           ;WRITE THE NEW BYTE TO THE 2817A
                                         ; (THE 2817A WILL NOW START A WRITE
                                         ;  OPERATION, INTERNALLY)
```

230714-41

```
                  ;
                          MOV     E2_BUSY,1               ;SET THE FLAG
                  ;
                          JMP     E2_XFER_FINISH


                  NO_NEW_DATA:
                          MOV     E2_BUSY,0               ;CLEAR THE FLAG
                  E2_XFER_FINISH:
                          POP     DI
                          POP     SI
                          RET
                  ;
                  ;
```

230714-42

This is how a section of the stack segment is allocated for the RAM Buffer table.

```
;
:
STACK      SEGMENT
:
;
;
RAM_BUFFER_TABLE     DB      ?        ;BYTE 1
                     DB      ?        ;BYTE 2
                     DB      ?        ;BYTE 3
                     DB      ?        ;BYTE 4
                     DB      ?        ;BYTE 5
                     DB      ?        ;BYTE 6
                     DB      ?        ;BYTE 7
                     DB      ?        ;BYTE 8
                     DB      ?        ;BYTE 9
                     DB      ?        ;BYTE 10
```

230714-43

This is the space allocation for the actual E^{2}PROM Look-up table in the 2817A.

```
;
:
E2PROM        SEGMENT
:
;
E2PROM_TABLE        DB      ?        ;BYTE 1
                    DB      ?        ;BYTE 2
                    DB      ?        ;BYTE 3
                    DB      ?        ;BYTE 4
                    DB      ?        ;BYTE 5
                    DB      ?        ;BYTE 6
                    DB      ?        ;BYTE 7
                    DB      ?        ;BYTE 8
                    DB      ?        ;BYTE 9
                    DB      ?        ;BYTE 10
```

230714-44

The 'DI' register is used in the "WRITE-E2-DATA" subroutine above to reference the E^{2}PROM. The following ASSUME directive and MOV instructions would be needed to assign the proper addresses to the segment registers:

```
;
     ASSUME       ES:E2PROM, SS:STACK
;
       MOV      AX,0
       MOV      SS,AX
       MOV      AX,8000H
       MOV      ES,AX
;
;
```

230714-45

8259A Initialization

The following is the code to initialize the 8259A Programmable Interrupt Controller for use in the 2817A/8088 Demo board.

```
;                      EQUATES
;
;
;
;
INT_CNTRLR_A0_LOW       EQU      0H
INT_CNTRLR_A0_HIGH      EQU      1H
;
ICW1          EQU        00010111B          ;EDGE TRIGGERED MODE
                                            ;ADDR INTERVAL OF 4
                                            ;SINGLE MODE
                                            ;ICW4 NEEDED
```

230714-46

```
;
ICW2          EQU        00100000B          ;TYPE 20H, (VECTOR OF 20H
                                            ;WILL COME FROM 8259A: IT'S
                                            ;VALUE IS MULTIPLIED BY 4,
                                            ;SO THAT AN INTERRUPT 0 TO
                                            ;THE 8259A WILL RESULT IN THE
                                            ;VECTOR BEING FETCHED FROM
                                            ;LOCATION 80H)
;
ICW4          EQU        00000001B          ;NOT SPECIAL FULLY NESTED
                                            ;MODE
                                            ;NON-BUFFERED MODE
                                            ;NORMAL EOI
                                            ;8086 MODE
;
OCW1          EQU        11111110B          ;MASK OUT ALL BUT INTERRUPT 0
;
OCW2          EQU        00100000B          ;END OF INTERRUPT COMMAND
                                            ;NON-SPECIFIC EOI COMMAND
;
;
;
;                 RAM MEMORY SPACE
;
;
;
STACK              SEGMENT AT 0                   ;RAM AREA LOCATED FROM 0 TO 1FFFH
                   DB       128 DUP(?)            ;RESERVED LOC'S


;
INTR_VECT          DW       ?                     ;E2PROM READY INTERRUPT SERVICE
                                                  ;SUBROUTINE VECTOR - OFFSET.
;
                   DW       ?                     ;SEGMENT VALUE
;
;
E2_BUSY            DB       ?                     ;SOFTWARE FLAG TO INDICATE THAT
                                                  ;AN E2PROM BLOCK TRANSFER IS IN
                                                  ;PROGRESS
;
;
                ORG         1FFFH
TOP_OF_STACK    DW          ?
;
STACK           ENDS
;
;
;
;
```

230714-47

```
;
;          CODE TO INITIALIZE THE 8259A
;
;
;
      OUT      INT_CNTRLR_A0_LOW,ICW1        ;1ST INITIALIZATION
                                             ;CONTROL WORD
;
      OUT      INT_CNTRLR_A0_HIGH,ICW2       ;2ND INITIALIZATION CONTROL
                                             ;WORD
;
      OUT      INT_CNTRLR_A0_HIGH,ICW4       ;LAST INIT. CONTROL WORD


      OUT      INT_CNTRLR_A0_HIGH,0CW1       ;MASK OUT UNUSED INTR LINES
;
      MOV      AX,OFFSET INTR_SERV_ROUT
      MOV      INTR_VECT,AX                  ;LOAD THE OFFSET VALUE OF THE
                                             ;INTERRUPT SERVICE ROUTINE INTO
                                             ;THE 1ST TWO BYTES OF THE
                                             ;INTERRUPT VECTOR DOUBLEWORD
;
      MOV      AX,CS
      MOV      INTR_VECT+2,AX                ;LOAD THE SEGMENT VALUE INTO THE
                                             ;2ND TWO BYTES OF THE INTERRUPT
                                             ;VECTOR DOUBLEWORD
```

230714-48

APPENDIX B
2817A/8088 APPLICATIONS DEMO

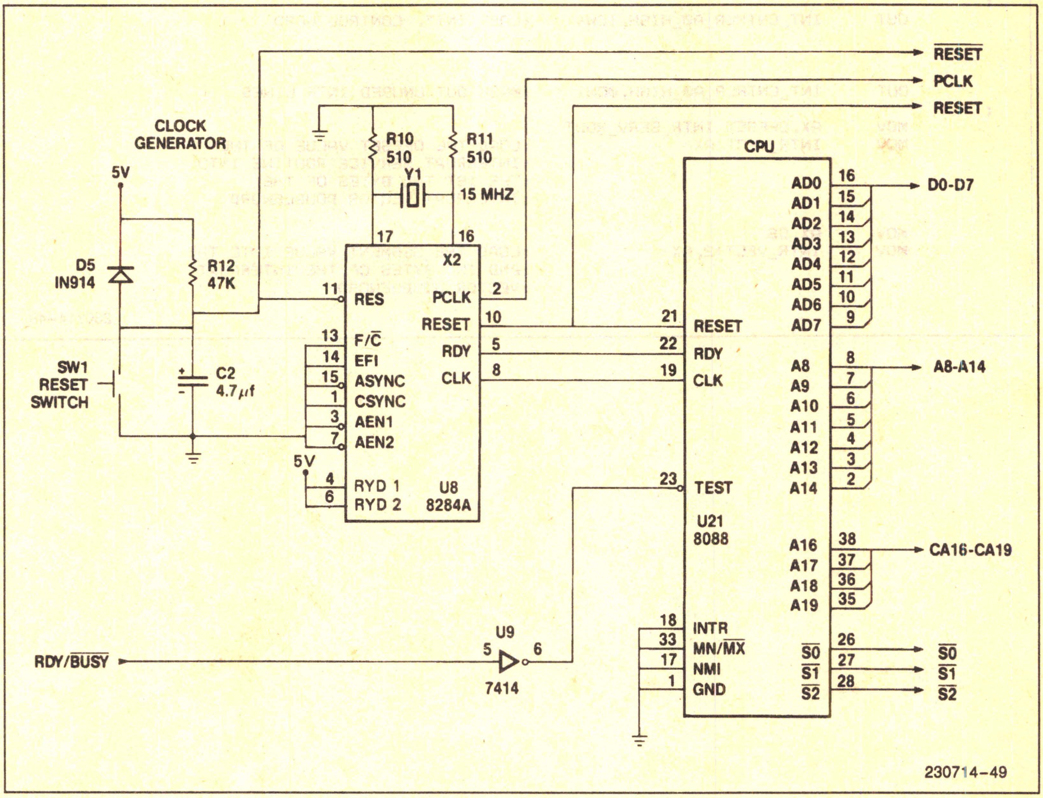

RESET
PCLK
RESET
CLOCK GENERATOR
5V
D5
IN914
R12
47K
SW1
RESET
SWITCH
C2
4.7μf
R10
510
R11
510
Y1
15 MHZ
17
16
X2
11
RES
PCLK
2
RESET
10
13
F/C
14
EFI
RDY
5
15
ASYNC
CLK
8
1
CSYNC
3
AEN1
7
AEN2
5V
4
RYD 1
6
RYD 2
U8
8284A
CPU
21
RESET
22
RDY
19
CLK
23
TEST
U21
8088
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
16
15
14
13
12
11
10
9
D0-D7
A8
A9
A10
A11
A12
A13
A14
8
7
6
5
4
3
2
A8-A14
A16
A17
A18
A19
38
37
36
35
CA16-CA19
18
INTR
33
MN/MX
17
NMI
1
GND
S0
S1
S2
26
27
28
S0
S1
S2
RDY/BUSY
U9
5
6
7414
230714-49

Figure 35. 2817A/8088 Applications Demo

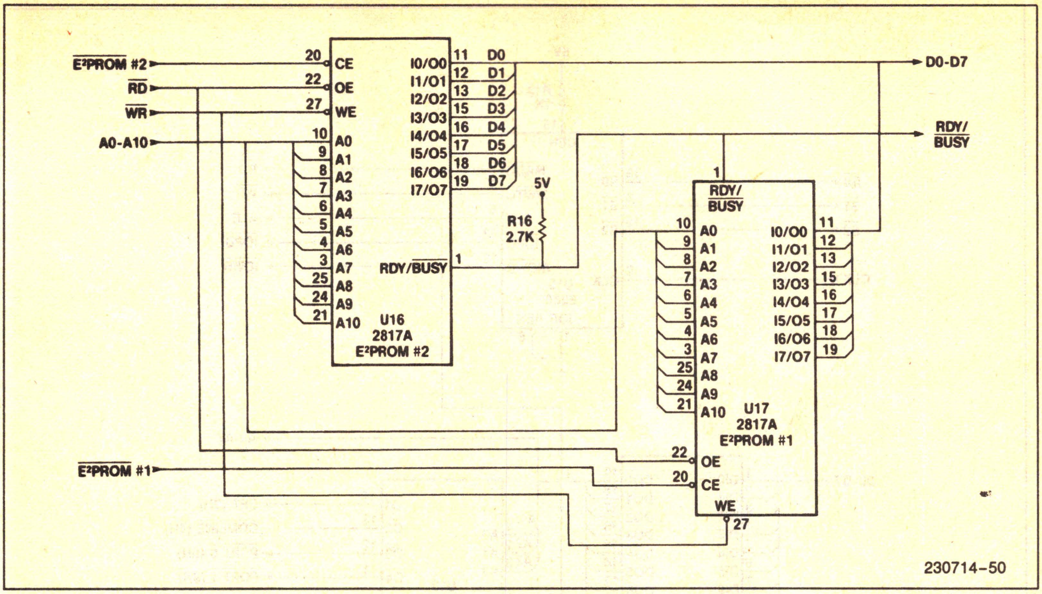

E²PROM #2
RD
WR
A0-A10
E²PROM #1
20
CE
22
OE
27
WE
10
A0
9
A1
8
A2
7
A3
6
A4
5
A5
4
A6
3
A7
25
A8
24
A9
21
A10
U16
2817A
E²PROM #2
I0/O0
I1/O1
I2/O2
I3/O3
I4/O4
I5/O5
I6/O6
I7/O7
11
12
13
15
16
17
18
19
D0
D1
D2
D3
D4
D5
D6
D7
RDY/BUSY
1
5V
R16
2.7K
D0-D7
RDY/
BUSY
1
RDY/
BUSY
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
U17
2817A
E²PROM #1
22
OE
20
CE
WE
27
I0/O0
I1/O1
I2/O2
I3/O3
I4/O4
I5/O5
I6/O6
I7/O7
230714-50

Figure 36. 2817A E²PROM Sockets

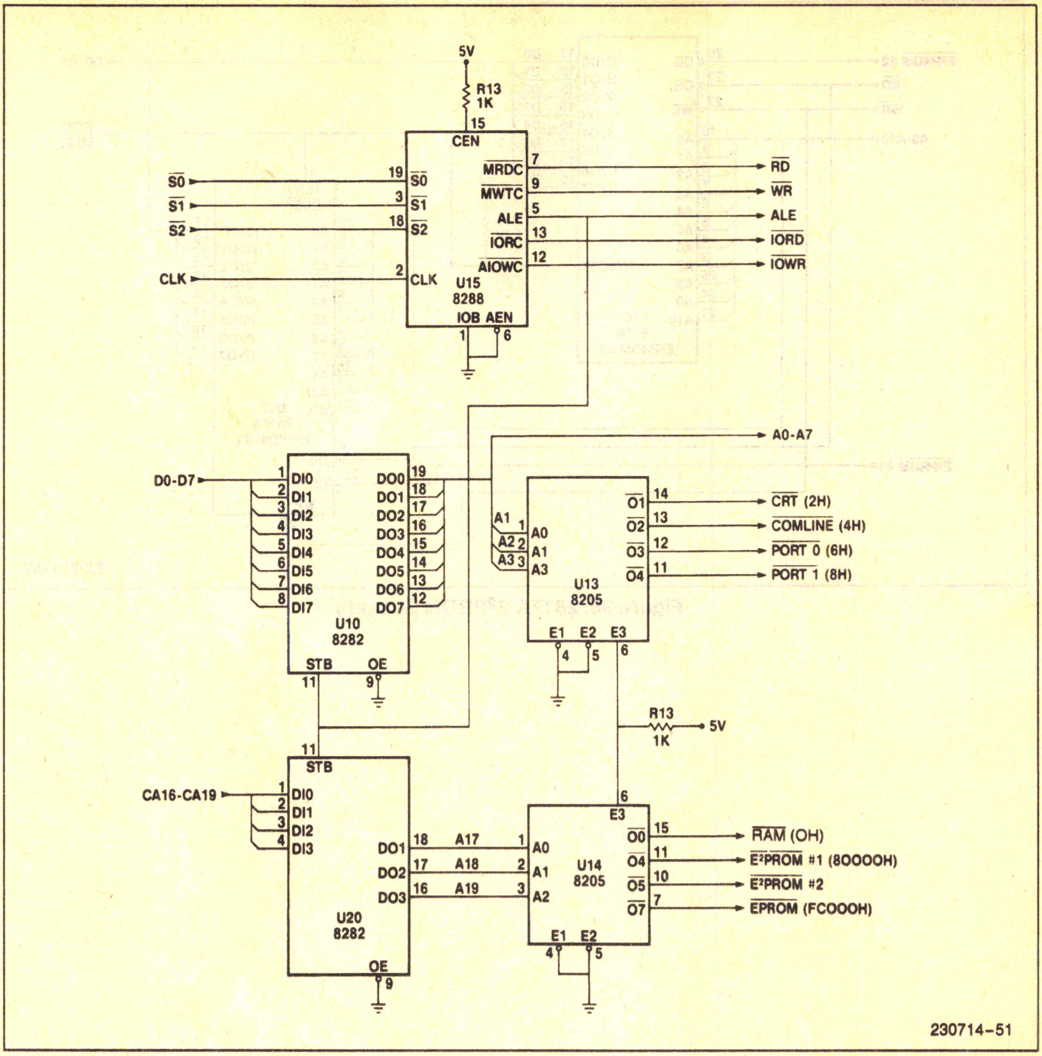

5V
R13
1K
15
CEN
S̄0
S̄1
S̄2
CLK
19
3
18
2
MRDC
MWTC
ALE
IORC
AIOWC
7
9
5
13
12
RD
WR
ALE
IORD
IOWR
U15
8288
IOB AEN
1
6
A0-A7
D0-D7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
U10
8282
STB
OE
11
9
A1
A2
A3
A0
A1
A3
O1
O2
O3
O4
14
13
12
11
CRT (2H)
COMLINE (4H)
PORT 0 (6H)
PORT 1 (8H)
U13
8205
E1
E2
E3
4
5
6
R13
1K
5V
CA16-CA19
STB
DI0
DI1
DI2
DI3
DO1
DO2
DO3
18
17
16
A17
A18
A19
U20
8282
OE
9
A0
A1
A2
E3
U14
8205
O0
O4
O5
O7
15
11
10
7
RAM (OH)
E²PROM #1 (80000H)
E²PROM #2
EPROM (FC000H)
E1
E2
4
5
230714-51

Figure 37. 2817A/8088 Applications Demo

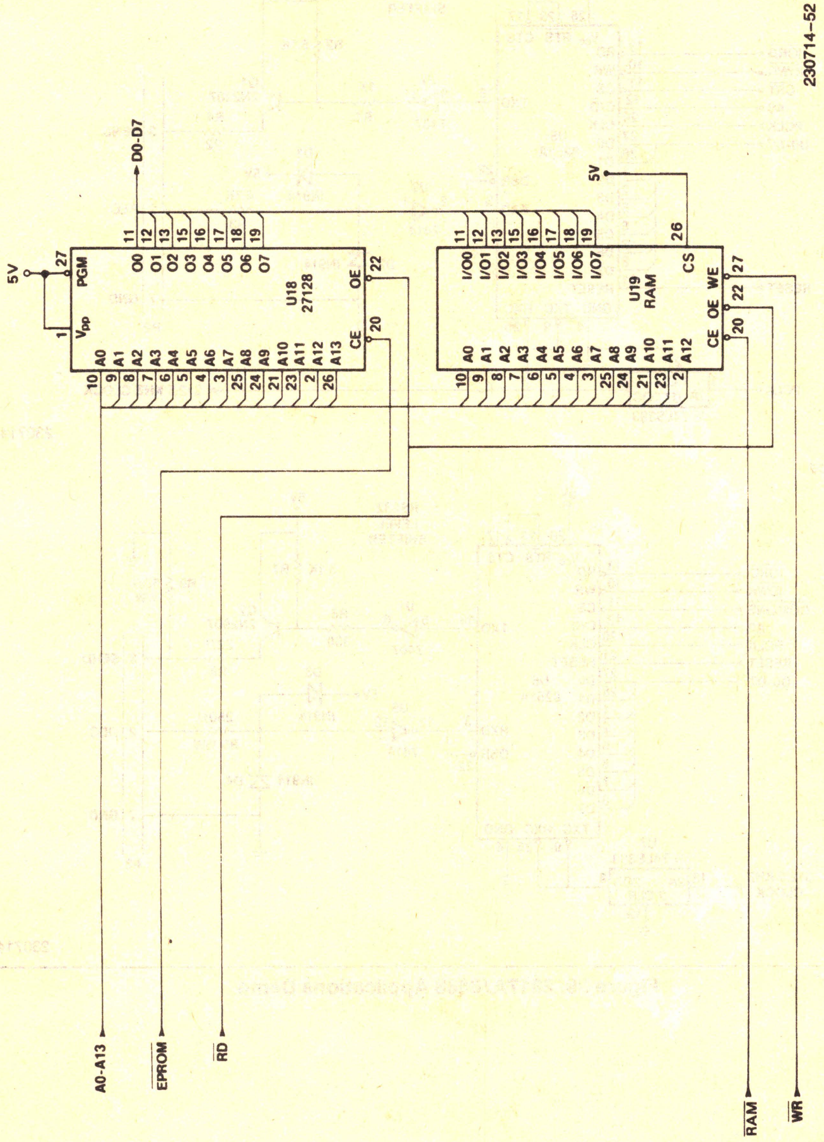
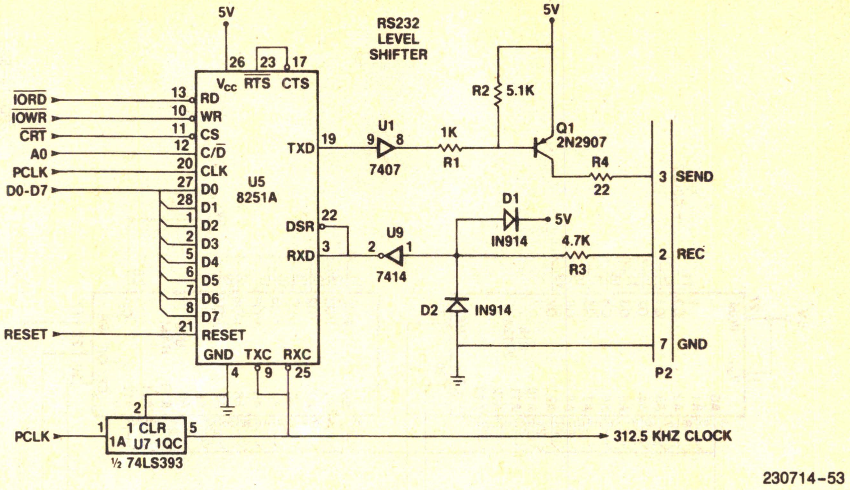

5V
1
27
Vpp
PGM
A0-A13
EPROM
RD
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
10
9
8
7
6
5
4
3
25
24
21
23
2
26
O0
O1
O2
O3
O4
O5
O6
O7
11
12
13
15
16
17
18
19
D0-D7
U18
27128
CE
OE
20
22
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
U19
RAM
5V
26
CS
CE
OE
WE
20
22
27
RAM
WR
230714-52

Figure 38. 2817A/8088 Applications Demo

CRT Interface


5V
26
23
17
Vcc RTS CTS
IORD
IOWR
CRT
A0
PCLK
D0-D7
13 RD
10 WR
11 CS
12 C/D
20 CLK
27 D0
28 D1
1 D2
2 D3
5 D4
6 D5
7 D6
8 D7
21 RESET
RESET
U5
8251A
TXD 19
DSR 22
RXD 3
GND TXC RXC
4 9 25
RS232
LEVEL
SHIFTER
U1
9 8
7407
U9
2 1
7414
1K
R1
5V
R2 5.1K
Q1
2N2907
R4
22
D1
IN914
5V
4.7K
R3
D2 IN914
3 SEND
2 REC
7 GND
P2
PCLK
1
2
1 CLR
1A U7 1QC
5
½ 74LS393
312.5 KHZ CLOCK
230714-53

COMLINE Interface

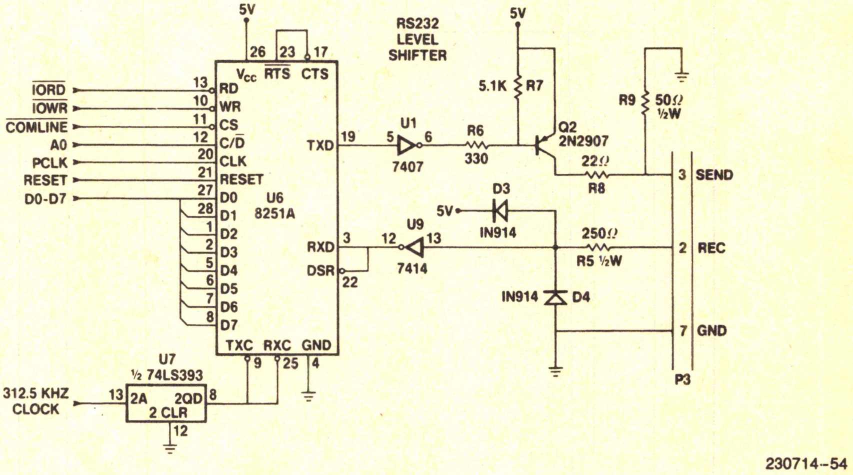

5V
26
23
17
Vcc RTS CTS
IORD
IOWR
COMLINE
A0
PCLK
RESET
D0-D7
13 RD
10 WR
11 CS
12 C/D
20 CLK
21 RESET
27 D0
28 D1
1 D2
2 D3
5 D4
6 D5
7 D6
8 D7
U6
8251A
TXD 19
RXD 3
DSR 22
TXC RXC GND
9 25 4
RS232
LEVEL
SHIFTER
U1
5 6
7407
R6
330
5V
5.1K R7
Q2
2N2907
22Ω
R8
R9 50Ω ½W
D3
5V
IN914
U9
12 13
7414
250Ω
R5 ½W
IN914 D4
3 SEND
2 REC
7 GND
P3
U7
½ 74LS393
312.5 KHZ CLOCK
13 2A 2QD 8
2 CLR
12
230714-54

Figure 39. 2817A/8088 Applications Demo

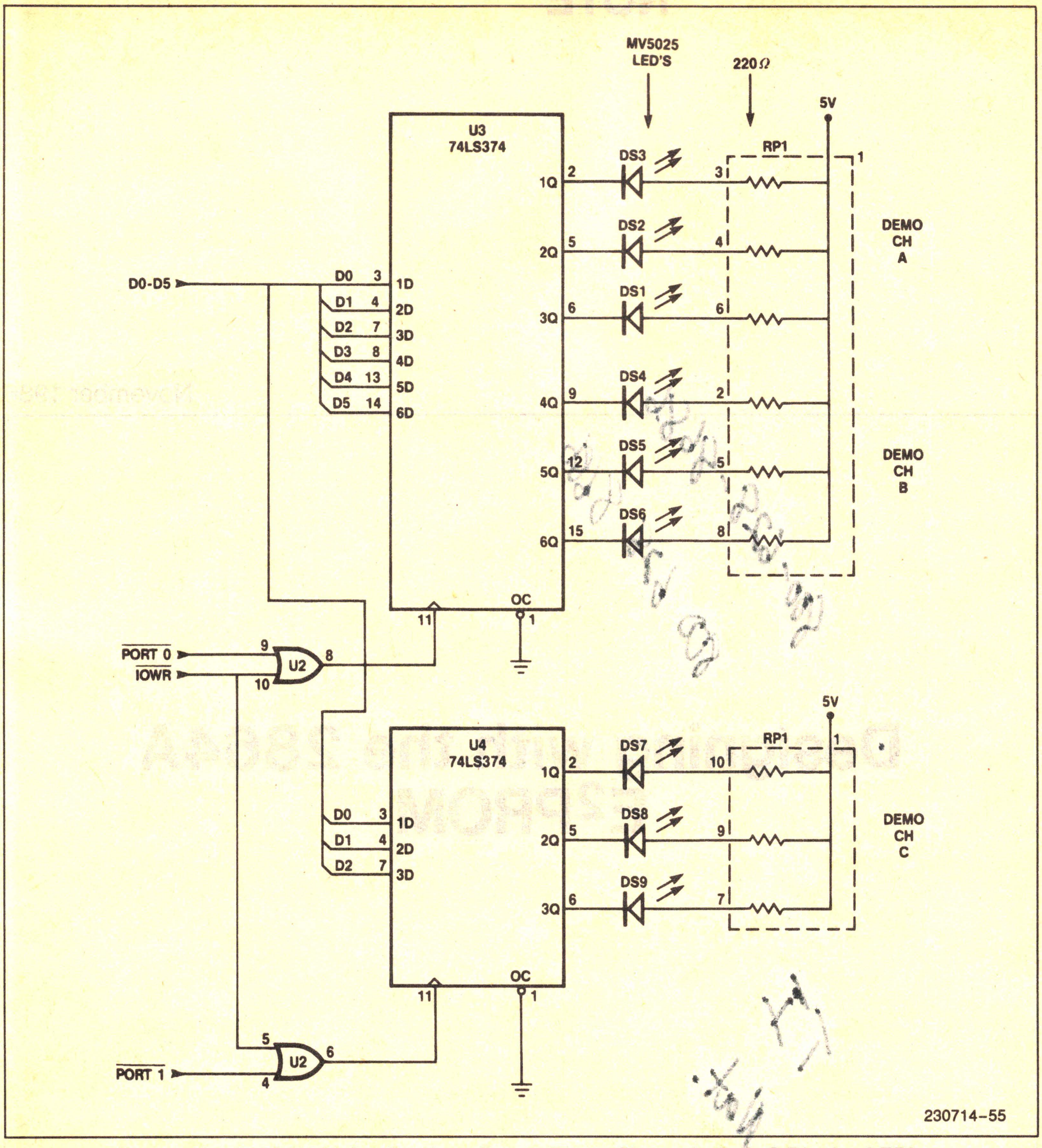

MV5025
LED'S
220Ω
5V
U3
74LS374
RP1
DS3
DS2
DS1
DS4
DS5
DS6
1Q
2Q
3Q
4Q
5Q
6Q
1D
2D
3D
4D
5D
6D
D0-D5
D0 3
D1 4
D2 7
D3 8
D4 13
D5 14
OC
11
1
DEMO CH A
DEMO CH B
PORT 0
IOWR
U2
9
10
8
U4
74LS374
DS7
DS8
DS9
D0 3
D1 4
D2 7
DEMO CH C
PORT 1
5
4
6
230714-55

Figure 40. 2817A/8088 Applications Demo, Demo Channels A, B, C Display LED's

intel®

APPLICATION
NOTE

AP-260

November 1986

800-628-8686

800 628 8688

Designing with the 2864A E^{2}PROM

TI

Nat.

DUC NGO
APPLICATIONS ENGINEER
INTEL CORPORATION

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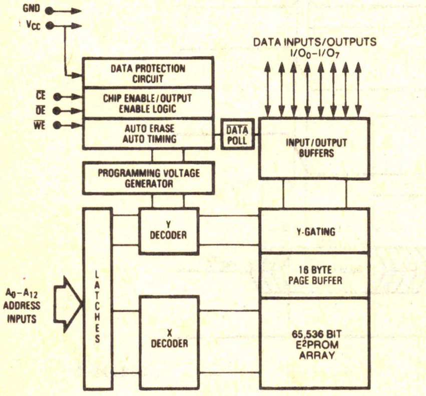
1.0 INTRODUCTION

Beginning with the introduction of the world first Electrically Erasable PROM in 1980, Intel has continued to drive the evolution of E^{2}PROM technology. As semiconductor process technologies are being pushed to new limits, it has become possible to integrate all the support circuitries onto silicon to make the E^{2}PROM a "user friendly" device. Figure 1.1 summarizes the Intel E^{2}PROM product family and the features of each product.

The Intel 2864A is a 5 volt only 8K × 8 E^{2}PROM. A high degree of integrated functionality includes a 16 byte Page Buffer, $\overline{\text{DATA}}$ Polling for end-of-write detection, on-chip data protection and on-chip latches. These additional features promote low hardware and software overhead, and ease of use for the designer. Figures 1.2, 1.3, 1.4 show the 2864A block diagram, pin out, and simple interface requirements.

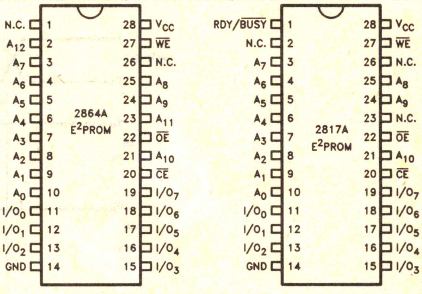
	2816A	2817A	2864A
Organization	2K × 8	2K × 8	8K × 8
Auto Erase	no	yes	yes
Internal Latches	no	yes	yes
5 Volt Only	yes	yes	yes
Data Protection	yes	yes	yes
$\overline{\text{DATA}}$ Polling End-of-Write	no	no	yes
Fast Read Access Time (ns)	200	200	200
Write Time (ms)	10	10	10
Chip Clear	yes	yes	yes
Endurance	10K	10K	10K
Data Retention (years)	10	10	10
Number of Pins	24	28	28

Figure 1.1. Intel E^{2}PROM Family


GND
VCC
CE
OE
WE
DATA PROTECTION CIRCUIT
CHIP ENABLE/OUTPUT ENABLE LOGIC
AUTO ERASE AUTO TIMING
DATA POLL
PROGRAMMING VOLTAGE GENERATOR
DATA INPUTS/OUTPUTS I/O0–I/O7
INPUT/OUTPUT BUFFERS
Y DECODER
Y-GATING
16 BYTE PAGE BUFFER
A0–A12 ADDRESS INPUTS
LATCHES
X DECODER
65,536 BIT E2PROM ARRAY

292004-1

Figure 1.2. 2864A Functional Block Diagram


N.C. 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 N.C.
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3
2864A E2PROM
RDY/BUSY 1
N.C. 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 N.C.
25 A8
24 A9
23 N.C.
22 OE
21 A10
20 CE
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3
2817A E2PROM

292004-2 292004-3

Figure 1.3. Pin Configurations

Pin Names

A_0–A_{12}	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
O_0–O_7	Data Outputs
I_0–I_7	Data Inputs
NC	No Connect
$\overline{\text{WE}}$	Write Enable

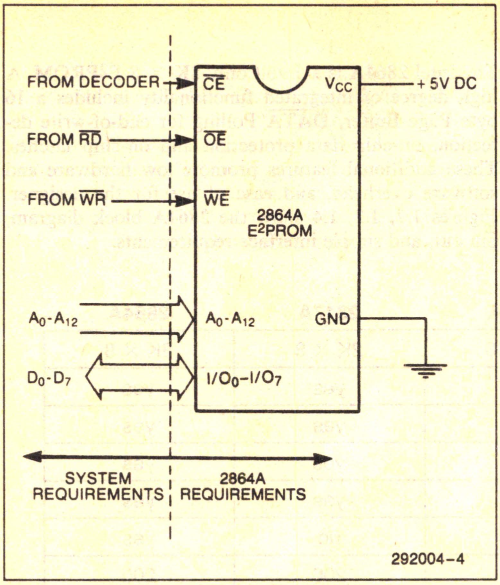

FROM DECODER
$\overline{CE}$
V_{CC}
+ 5V DC
FROM $\overline{RD}$
$\overline{OE}$
FROM $\overline{WR}$
$\overline{WE}$
2864A
E²PROM
A_0-A_{12}
A_0-A_{12}
GND
D_0-D_7
I/O_0-I/O_7
SYSTEM REQUIREMENTS
2864A REQUIREMENTS
292004-4

Figure 1.4. Simple 2864A Interface Requirements

2.0 DEVICE OPERATION

The 2864A has 5 modes of operation which are detailed in Figure 2.1. These modes enhance the 2864A's functionality to users and provide total E²PROM/microprocessor-microcontroller compatibility.

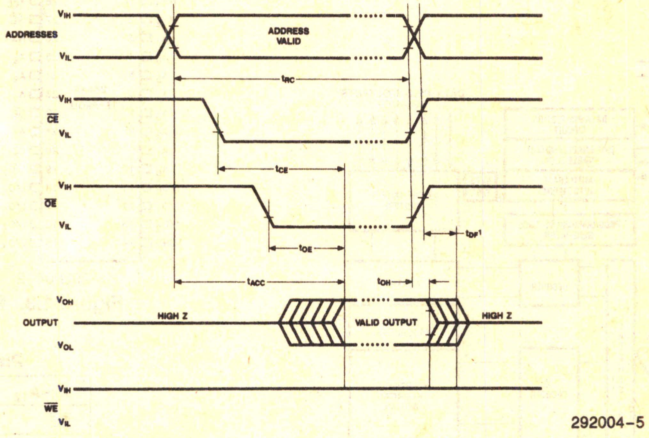
2.1 Read Mode

Reading a 2864A is similar to reading EPROMs and SRAMs. The read timing diagram and its characteristics are shown in Figures 2.2 and 2.3. The 2864A has two control functions, both of which must be logically active in order to obtain data at the outputs. $\overline{CE}$ controls power to the chip and should be used for device selection. The 2864A should be selected by connecting the output of the system address decoder to $\overline{CE}$. $\overline{OE}$ is the output control and it should be used to gate the data from the output pins, independent of device selection. $\overline{OE}$ is usually connected to the $\overline{RD}$ from the processor. Assuming that address inputs are stable, the address access (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O_0-I/O_7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby and Write Inhibit	V_{IH}	X	X	Hi Z
Write Inhibit	X	V_{IL}	X	—
Write Inhibit	X	X	V_{IH}	—

Figure 2.1. Mode Selection Table

NOTE:
1. X can be V_{IH} or V_{IL}


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
t_{RC}
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF}¹
t_{OE}
t_{ACC}
t_{OH}
V_{OH}
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
V_{OL}
V_{IH}
$\overline{WE}$
V_{IL}
292004-5

NOTE:
1. t_{DF} is measured from the point when $\overline{CE}$ or $\overline{OE}$ returns high (whichever occurs first) to the time when the outputs are no longer driven. This parameter is not 100% tested.

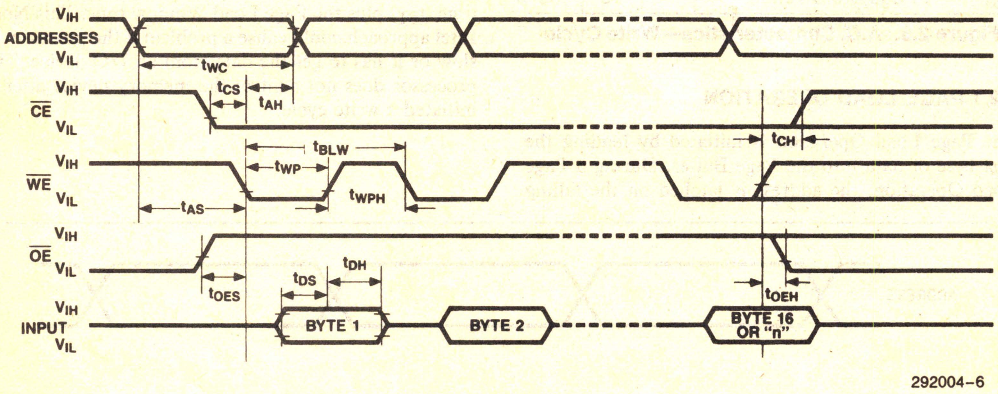
Figure 2.2. A.C. Waveforms for Read Cycle

Symbol	Parameter	2864A-20		Units
		Min	Max	
t_{RC}	Read Cycle Time	200		ns
t_{ACC}	Address to Output Delay		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		150	ns
t_{DF}(1)	$\overline{OE}$ or $\overline{CE}$ HIGH to Output not Driven	10	60	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$	10		ns

Figure 2.3. A.C. Characteristics—Read Cycle

2.2 Write Mode

The 2864A enhanced write mode allows the user to write from 1 to 16 bytes of data in a single write cycle. The 2864A no longer writes directly to the array like previous E^2PROMs. Instead, the array is organized into 512 pages with 16 bytes per page. A page buffer consists of 16 bytes of storage, interposed between the write circuitry and the E^2PROM array. Writing is a 2 step operation. In the first step, the data is written into the page buffer in random fashion similar to a SRAM write operation by the system processor. The second step is transparent to the system and is initiated automatically 20 μs after the last byte has been written into the page buffer. In this application note, the first step is referred as the Page Load operation (performed by the processor) and the second step is referred as the Page Store operation (performed by the 2864A). A complete write cycle consists of the Page Load and Page Store operations. Figure 2.4 shows the write timing diagram and Figure 2.5 shows the write characteristics of a write cycle.



NOTE:
"n" ≤ 16

Figure 2.4. A.C. Waveforms for Page Write Cycle

Symbol	Parameter	2864A-20		Unit
		Min	Max	
t_{WC}	Write Cycle Time	200		ns
t_{AS}	Address Set Up Time	10		ns
t_{CS}	$\overline{CE}$ Set Up Time	0		ns
t_{WP}	Write Pulse Width	150		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{AH}	Address Hold Time	200		ns
t_{DS}	Data Set Up Time	100		ns
t_{DH}	Data Hold Time	20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		ns
t_{BLW}	Byte Load Window	3	20	μs
t_{ST}	Page Store Time		10	ms

Figure 2.5. A.C. Characteristics—Write Cycle

2.2.1 PAGE LOAD OPERATION

The Page Load Operation is initiated by loading the first byte of data into the Page Buffer. During a Page Load Operation, the address is latched on the falling edge and the data is latched on the rising edge of each $\overline{WE}$ pulse as shown in Figure 2.6. Beginning from the falling edge of the $\overline{WE}$ pulse, the user has 20 μs to load the next byte into the page buffer. This process can be repeated and the 2864A will stay in the Page Load mode as long as the user keeps the 20 μs window open by writing the next byte of data into the page buffer. The page address (A4–A12) must not change during the page load operation and data can be randomly written into the page buffer. Note that all timings can be completed within 200 ns using microprocessor and microcontroller control signals. Additional hardware is completely eliminated.

The internal 20 μs timer is referred to as the Byte Load Window (t_{BLW}). It is different from the Page Load Window architecture on some earlier E^2PROMs from other manufacturers. Figure 2.7 shows the timing of the Page Load Window architecture. The processor can write as many times as desired within a fixed Page Load Window time, as soon as the internal timer times out, the memory device will enter the store mode. In this case, the write cycle time is always equal the store time (t_{ST}) plus the Page Load Window time. This Non-Intel approach could cause a problem if the processor is slow or it has to get the data from an I/O device. The processor does not control the memory device after it initiated a write cycle.

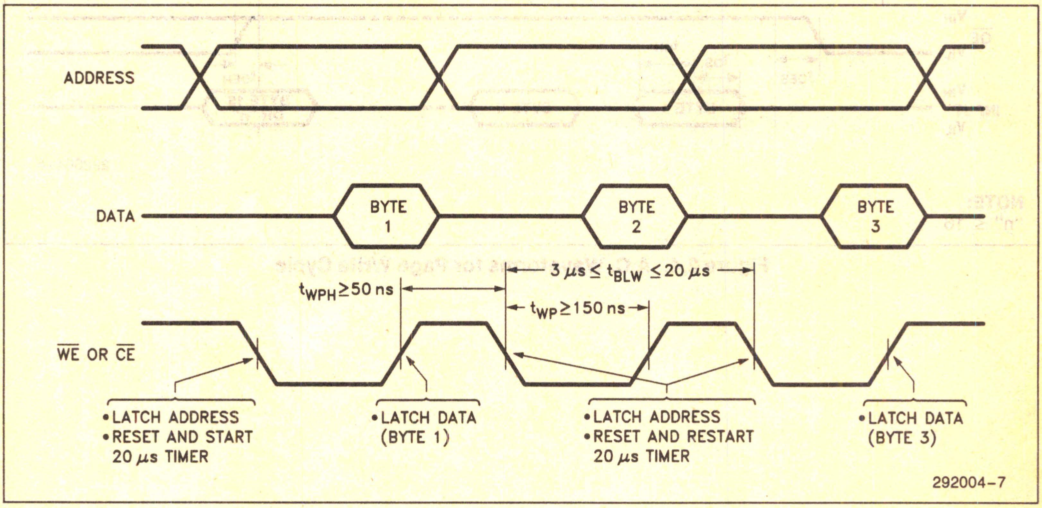


Figure 2.6. Page Load Operation. The Address is Latched and the 20 μs Timer is Reset and Restart on each Falling Edge of $\overline{WE}$. Data is Latched on each Rising Edge of $\overline{WE}$.

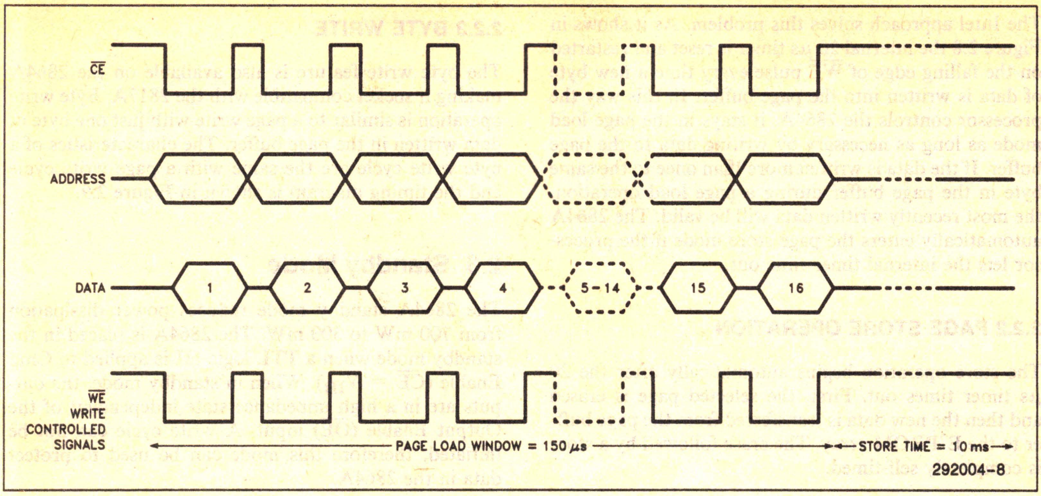

CE
ADDRESS
DATA
1
2
3
4
5-14
15
16
WE
WRITE
CONTROLLED
SIGNALS
PAGE LOAD WINDOW = 150 µs
STORE TIME = 10 ms
292004-8

Figure 2.7. Non-Intel Approach—Fixed Page Load Window

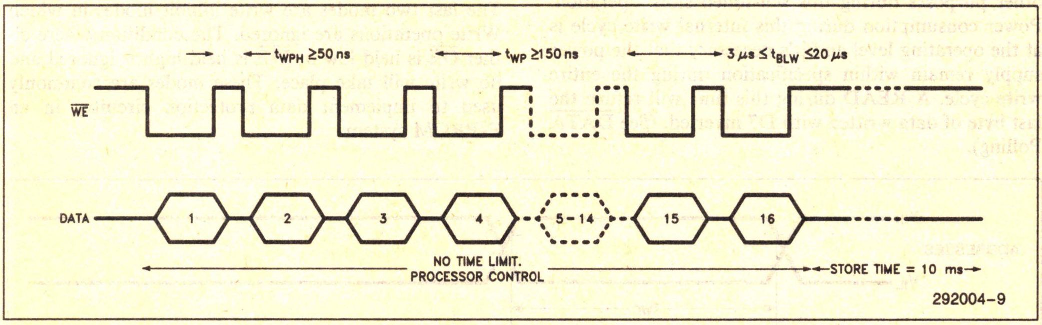

t_{WPH} ≥50 ns
t_{WP} ≥150 ns
3 µs ≤ t_{BLW} ≤20 µs
WE
DATA
1
2
3
4
5-14
15
16
NO TIME LIMIT.
PROCESSOR CONTROL
STORE TIME = 10 ms
292004-9

Figure 2.8. Intel Approach—Page Load Window is Controlled by the System

The Intel approach solves this problem. As it shows in Figure 2.8 the internal 20 μs timer is reset and restarted on the falling edge of $\overline{\text{WE}}$ pulse every time a new byte of data is written into the page buffer. In this way the processor controls the 2864A, it stays in the page load mode as long as necessary by writing data to the page buffer. If the data is written more than once to the same byte in the page buffer during a page load operation, the most recently written data will be valid. The 2864A automatically enters the page store mode if the processor lets the internal timer time out.

2.2.2 PAGE STORE OPERATION

The store operation begins automatically after the 20 μs timer times out. First, the selected page is erased and then the new data is transferred from the page buffer to the E^2PROM array. The erase followed by a store is completely self-timed.

Note that during the STORE operation, all the write control signals are ignored and the data bus is tri-stated. This feature allows the system to use the bus for other purposes during this self-timed store operation. Power consumption during this internal write cycle is at the operating level and it's necessary that the power supply remain within specification during the entire write cycle. A READ during this time will return the last byte of data written with D7 inverted. (See $\overline{\text{DATA}}$ Polling).

2.2.3 BYTE WRITE

The byte write feature is also available on the 2864A making it socket compatible with the 2817A. Byte write operation is similar to a page write with just one byte of data written in the page buffer. The characteristics of a byte write cycle are the same with a page write cycle and the timing diagram is shown in Figure 2.9.

2.3 Standby Mode

The 2864A standby mode reduces power dissipation from 700 mW to 300 mW. The 2864A is placed in the standby mode when a TTL logic HI is applied to Chip Enable ($\overline{\text{CE}} = V_{IH}$). When in standby mode, the outputs are in a high impedance state independent of the Output Enable ($\overline{\text{OE}}$) input. A write cycle can not be initiated, therefore this mode can be used to protect data in the 2864A.

2.4 Write Inhibit Modes

The last two modes are write inhibit modes in which Write operations are ignored. The condition where either $\overline{\text{OE}}$ is held low or $\overline{\text{WE}}$ is held high is ignored and no write will take place. These modes are commonly used to implement data protection circuitry in an E^2PROM system.

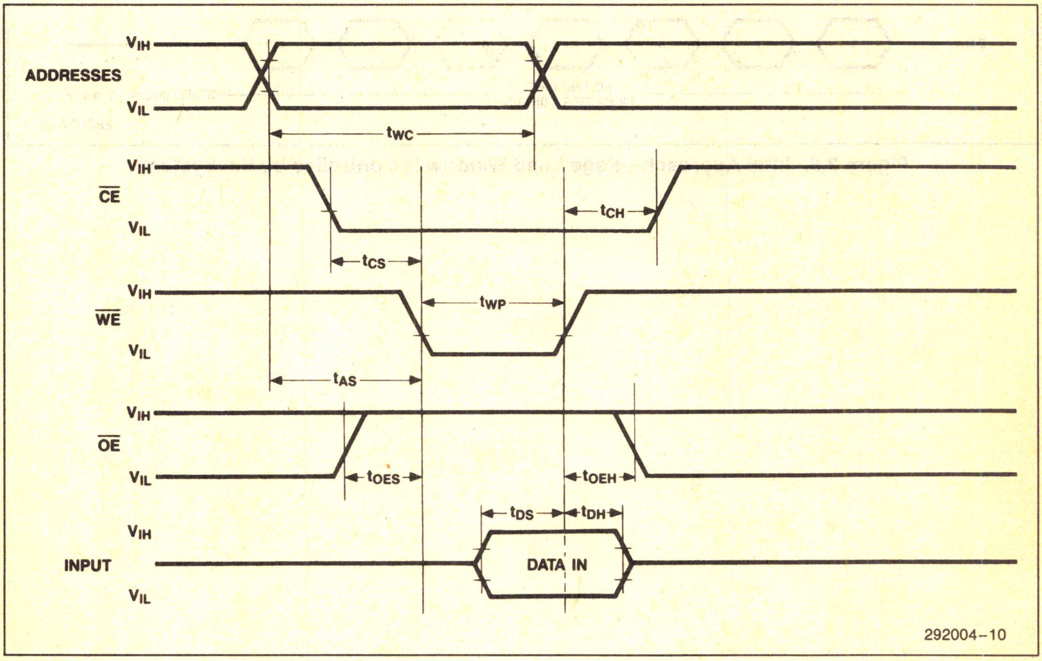


Figure 2.9. A.C. Waveform for Byte Write Cycle

3.0 DESIGN CONSIDERATIONS

3.1 $\overline{\text{DATA}}$ Polling for End of Write Detection

The detection of the end of a write cycle is often a concern for E^2PROM designers. As it takes milliseconds to reprogram (Erase/Write) an E^2PROM cell, system performance is optimized when an End-Of-Write indicator is used.

$\overline{\text{DATA}}$ polling is a software technique to detect the completion of a write cycle. This is accomplished by monitoring the device status via the system data bus using a simple read/compare instruction.

$\overline{\text{DATA}}$ Polling does not require any external hardware and the software is simple. If a read command is issued at any time during a write cycle, the most significant bit of the last byte written is inverted and routed to I/07. In this event I/00–I/06 are indeterminate. The device will not release true data until the write cycle is complete. The processor can thus compare the output with the true data at the address last written to detect the end of a write cycle. If the comparison is true, the 2864A has completed the write cycle and is now ready for additional writes. Figure 3.1 is the flowchart for $\overline{\text{DATA}}$ polling. The actual code written in 8051 assembly language is shown in Figure 3.2 and its timing is shown in Figure 3.3.

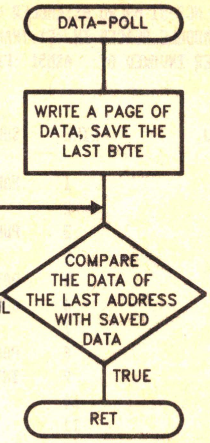
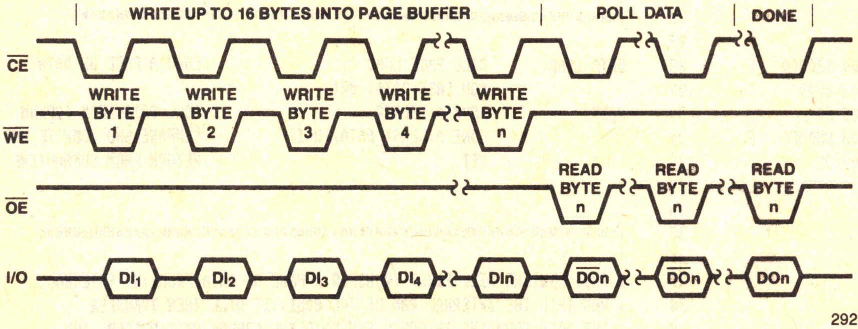

DATA-POLL
WRITE A PAGE OF DATA, SAVE THE LAST BYTE
COMPARE THE DATA OF THE LAST ADDRESS WITH SAVED DATA
FAIL
TRUE
RET
292004-12

Figure 3.1. Flowchart for $\overline{\text{DATA}}$ Polling


WRITE UP TO 16 BYTES INTO PAGE BUFFER
POLL DATA
DONE
$\overline{\text{CE}}$
WRITE BYTE 1
WRITE BYTE 2
WRITE BYTE 3
WRITE BYTE 4
WRITE BYTE n
$\overline{\text{WE}}$
READ BYTE n
READ BYTE n
READ BYTE n
$\overline{\text{OE}}$
I/O
DI_1
DI_2
DI_3
DI_4
DIn
$\overline{\text{DO}}$n
$\overline{\text{DO}}$n
DOn
292004-11

NOTES:
1. "n" can be up to 16.
2. During $\overline{\text{DATA}}$ POLLING, read the last address and use true data for comparison.

Figure 3.3. A.C. Waveform for $\overline{\text{DATA}}$ Polling

During write cycle:

—I/07 is complemented
—I/00 - I/06 are indeterminated
—A compare with byte written fails

After write cycle is completed:

—All bits are true (I/00–I/07)
—A compare with byte written passes

```
ISIS-II MCS-51 MACRO ASSEMBLER V2.1
OBJECT MODULE PLACED IN :F1:TRAN51.OBJ
ASSEMBLER INVOKED BY:   ASM51 :F1:TRAN51.A51


LOC  OBJ            LINE     SOURCE

                       1     NAME    SUB1MOD
                       2
                       3     PUBLIC  DATA_LOAD, LAST_DATA
                       4
                       5     DATA_SEG1       SEGMENT DATA
                       6     CODE_SEG1       SEGMENT CODE
                       7
 0010                  8     PAGE_SIZE       EQU     16
 0060                  9     INT_RAM_BUFF    EQU     60H
                      10
----                  11             RSEG    DATA_SEG1
0000                  12     LAST_DATA:      DS      1
                      13
----                  14             RSEG    CODE_SEG1
                      15
                      16     ;**********************************************************
                      17     ;
                      18     ; THIS IS DATA/ POLLING SOFTWARE ROUTINE. AFTER DATA IS LOADED
                      19     ; INTO THE PAGE BUFFER, THE DATA LAST WRITTEN IS USED FOR THE
                      20     ; COMPARISON.
                      21     ; THIS ROUTINES INPUTS ARE:
                      22     ; R7 AND R6 - HIGH AND LOW ADDRESS BYTES OF THE EXTERNAL RAM;
                      23     ; R5 AND R4 - HIGH AND LOW ADDRESS BYTES OF THE E2PROM PAGE TO
                      24     ;             BE WRITTEN TO.
                      25     ;
                      26     ;**********************************************************
                      27
0000 120000   F       28     DATA_LOAD:      CALL PAGE_LOAD                  ;LOAD A PAGE OF DATA
0003 8700     F       29                     MOV LAST_DATA, @R1              ;
0005 E0               30     WAIT:           MOVX A, @DPTR                   ;POLL DATA FROM E2PROM
0006 B500FC   F       31                     CJNE A, LAST_DATA, WAIT         ;COMPARE AND JUMP IF NOT =
0009 22               32                     RET                             ;RETURN FROM SUBROUTINE
                      33
                      34
                      35     ;**************************************************************
                      36     ;
                      37     ; THIS ROUTINE WILL FIRST TRANSFER A PAGE OF DATA FROM THE EXTERNAL
                      38     ; RAM INTO THE INTERNAL RAM OF THE 8051, IT WILL THEN TRANSFER
                      39     ; THE DATA FROM THE INTERNAL RAM INTO THE E2PROM PAGE BUFFER. THE
                      40     ; ROUTINE IS WRITTEN TO MEET THE 2864A SPECIFICATION.
                      41     ;
                      42     ;**************************************************************
                      43
000A 7810             44     PAGE_LOAD:      MOV R0, #PAGE_SIZE              ;R0 CONTAINS THE BUFFER SIZE
000C 8F83             45                     MOV DPH, R7                     ;ADDRESS EXT_RAM_BUFF
000E 8E82             46                     MOV DPL, R6
0010 7960             47                     MOV R1, #INT_RAM_BUFF           ;R1 POINTS TO INTERNAL RAM
0012 E0               48     AGAIN1:         MOVX A, @DPTR                   ;GET DATA FROM EXTERNAL RAM
0013 F7               49                     MOV @R1, A                      ;STORE DATA IN INTERNAL RAM
```

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Figure 3.2. 8051 Code for a Page Load Operation

```
LOC  OBJ            LINE    SOURCE

0014 09              50                     INC R1                      ;UPDATA POINTERS
0015 A3              51                     INC DPTR
0016 D8FA            52                     DJNZ R0, AGAIN1             ;LOOP UNTIL R0 = 0
                     53
0018 7810            54                     MOV R0, #PAGE_SIZE          ;RELOAD R0 WITH PAGE SIZE
001A 7960            55                     MOV R1, #INT_RAM_BUFF       ;R1 POINTS TO INTERNAL RAM
001C 8D83            56                     MOV DPH, R5                 ;ADDRESS E2PROM
001E 8C82            57                     MOV DPL, R4
0020 E7              58     XFER:           MOV A, @R1                  ;GET DATA FROM INTERNAL
0021 F0              59                     MOVX @DPTR, A               ;XFER DATA TO E2PROM
0022 09              60                     INC R1                      ;UPDATA POINTS
0023 A3              61                     INC DPTR
0024 D8FA            62                     DJNZ R0, XFER               ;LOOP UNTIL R0 = 0
0026 19              63                     DEC R1                      ;GET LAST BYTE WRITTEN
0027 1582            64                     DEC DPL                     ;GET LAST LOCATION WRITTEN
0029 E582            65                     MOV A, DPL
002B B4FF02          66                     CJNE A, #0FFH, NOTBOW       ;IF NOT BORROW THEN JUMP
002E 1583            67                     DEC DPH
0030 22              68     NOTBOW:         RET
                     69                     END
```

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Figure 3.2. 8051 Code for a Page Load Operation (Continued)

3.2 Fast Array Programming

Fast Array programming is a different way of decoding an array of E²PROMs that dramatically reduces total write time to the array without adding any system software or hardware. The concept is to perform page write operations in parallel. A page write is started in each device in rapid succession. Figure 3.4 shows the hardware for implementing fast array programming. Instead of using the highest system address lines for selecting or deselecting an individual device in an E²PROM array, address lines A4, A5, A6 are used. This decoding technique allows a page write to be done in each 2864A in the array at the same time. A page store is started in the first 2864A, after the last byte of data is loaded (A0–A3 are "1"), address bits A4–A6 are incremented and the next device is selected. The worst case total programming time can be calculated using the following formula:

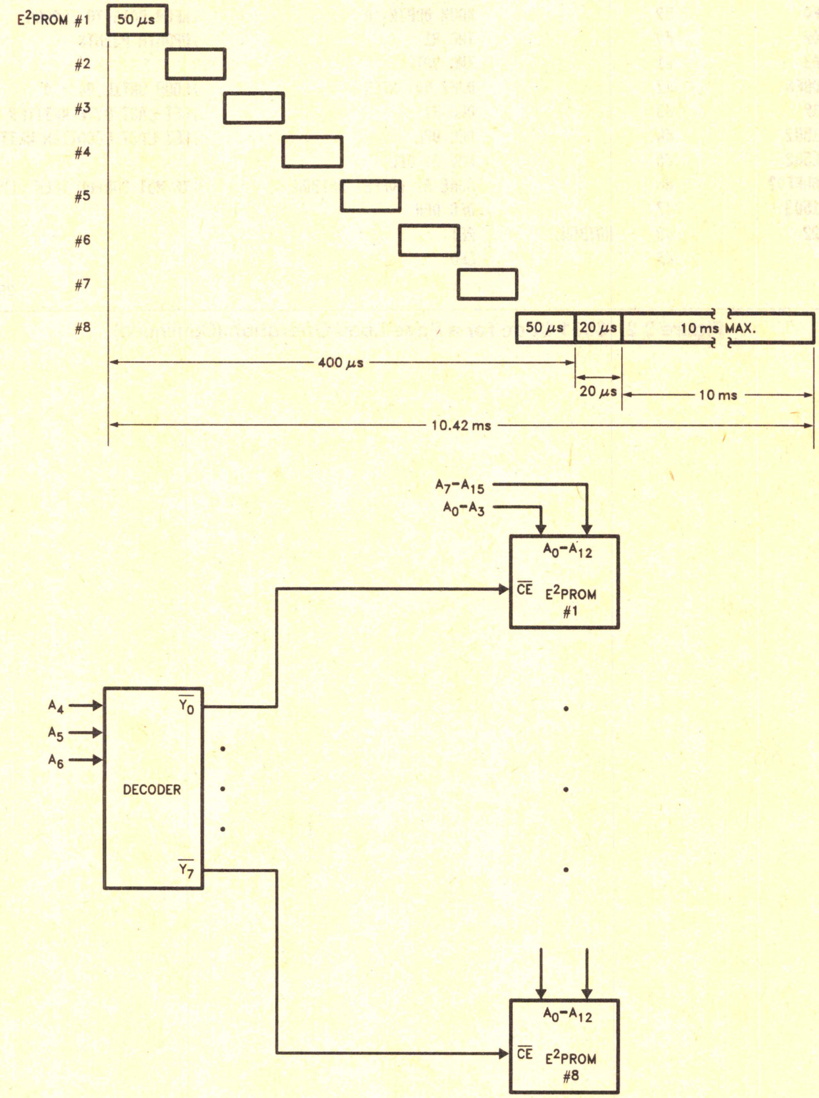
E²PROM #1
50 μs
#2
#3
#4
#5
#6
#7
#8
50 μs
20 μs
10 ms MAX.
400 μs
20 μs
10 ms
10.42 ms
A7–A15
A0–A3
A0–A12
CE
E²PROM
#1
A4
A5
A6
Y0
DECODER
Y7
A0–A12
CE
E²PROM
#8

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Figure 3.4. Decoding Technique for Fast Array Programming

$t_{PROG} = [(t_{LP} * n) + t_{ST} + t_{BLW}] * 512$

Where tLP : time it takes to load a page of data.

n : number of 2864A in the array.

t_{ST} : store time, 10 ms maximum.

t_{BLW} : byte load window, 20 µs maximum.

512 is the total number of pages in the array.

An iAPX-188 requires approximately 50 µs to load 16 bytes of data into the 2864A page buffer, t_{LP} in this system is 50 µs.

To reprogram an entire array of eight 2864As:

$$t_{PROG} = [(50\ \mu s * 8) + 10\ ms + 20\ \mu s] * 512 = 5.33\ \text{seconds}.$$

The effective write time is (5.33 sec. / 8*8192 =) 81.40 µs/byte.

For just one 2864A:

$$t_{PROG} = [(50\ \mu s * 1) + 10\ ms + 20\ \mu s] * 512 = 5.15\ \text{seconds}.$$

The effective write time is (5.15. sec / 8192 =) 629.37 µs/byte.

As can be seen from the above example, by using the Fast Array Programming technique, the total programming time for an array of 2864As is reduced by a factor equal to the number of 2864As in the array.

Some cautions should be taken when implementing fast array programming. This technique can cause all 2864As in the system to be drawing full write operation current simultaneously. This is due to the fact that the 2864A will draw full active current while the write operation continues, even though the device is deselected, proper design techniques for power, ground bussing, as well as decoupling should be used. If $\overline{\text{DATA}}$ polling is used to detect the end of write of the E²PROMs in the array, the last address and data of every 2864A has to be saved. The software should be written to perform $\overline{\text{DATA}}$ polling on every device in the array.

3.3 Data Protection

Like any non-volatile media that can be rewritten in-circuit or reprogrammed (Floppy disk, tape, battery backed RAM, NVRAM . . . , E²PROM is subjected to unstable system control signals that may occur during system power up or power down.

Whenever power is applied to or removed from the system the behavior of the system is unpredictable. An unwanted write cycle can occur and erroneous data can be written into the E²PROM. The 2864A has V_{CC} sense circuitry on chip that will disable the internal programming circuitry when V_{CC} is ≤ 3.0V, typically. Figure 3.5 illustrates the system write command signal during the system power up and power down.

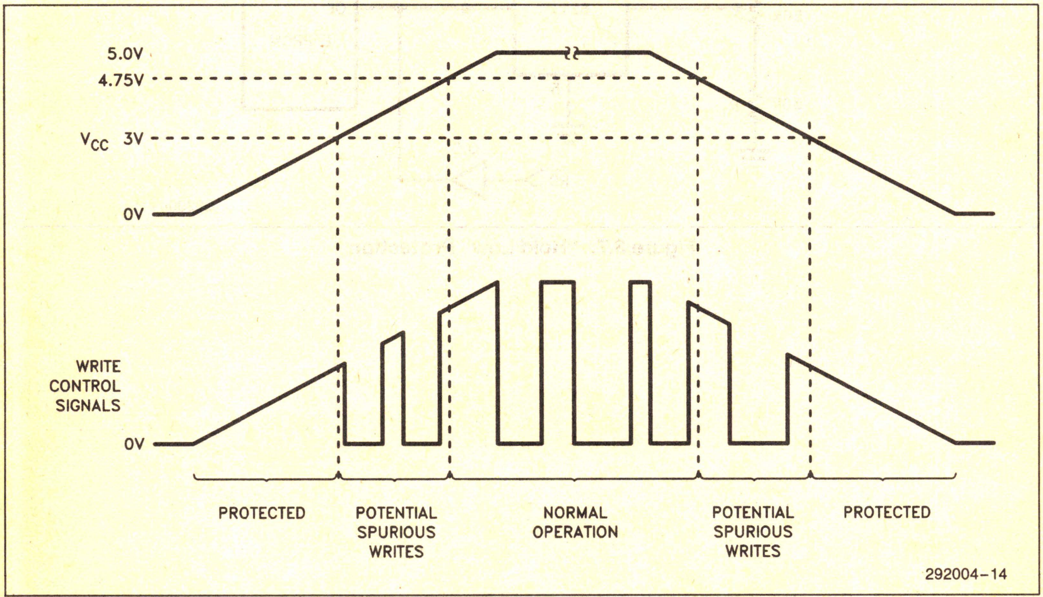


Figure 3.5. Write Control Signals During Power Up/Down

It is the user responsibility to determine whether an additional data protection circuitry is needed or not. Most applications will require some forms of protection above 3.0V. The concept of data protection is to put the 2864A into a write inhibit mode whenever the V_{CC} falls below a preset voltage level. Figure 3.6 summarizes three write inhibit modes of the 2864A. Several simple, low cost and reliable circuits can be derived to implement a data protection scheme for the E^2PROM.

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Implementation
1	X	X	Held High
X	0	X	Held Low
X	X	1	Held High

Figure 3.6. Write Inhibit Mode Table

3.3.1 $\overline{\text{OE}}$ HELD-LOW DESIGN

It is easier to keep a signal at a low level than to keep it at a high level when V_{CC} is falling from 5.0V to 0.0V or rising from 0.0V to 5.0V. Figure 3.7 shows a simple design that will keep the $\overline{\text{OE}}$ signal at a low level whenever the supply voltage is below the protection level set by the user. This design used the Intersil ICL8211 for voltage level detection. The trip voltage can be set anywhere from 3.0V to 4.75V using a 50K potentiometer. The open collector output of the ICL-8211 will only return to high level (or follow the supply voltage level) if the supply voltage is above the preset protection level. The system $\overline{\text{RD}}$ signal is buffered through an open collector output hex buffer and is wire-ORed with the output of the ICL-8211. The $\overline{\text{OE}}$ signal will be delayed for a few nanoseconds (the propagation delay of the hex buffer) and it should not effect the overall system timing.

3.3.2 $\overline{\text{CE}}$ OR $\overline{\text{WE}}$ HELD-HIGH DESIGN

Another way to protect the data of the E^2PROM is to make sure that the voltage level of the $\overline{\text{CE}}$ signal or $\overline{\text{WE}}$ signal is at a high level until the V_{CC} level has reached its normal operating level. This can be easily done as shown in Figure 3.8. In this case the output of the ICL-8211 is used to qualify either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ signal.

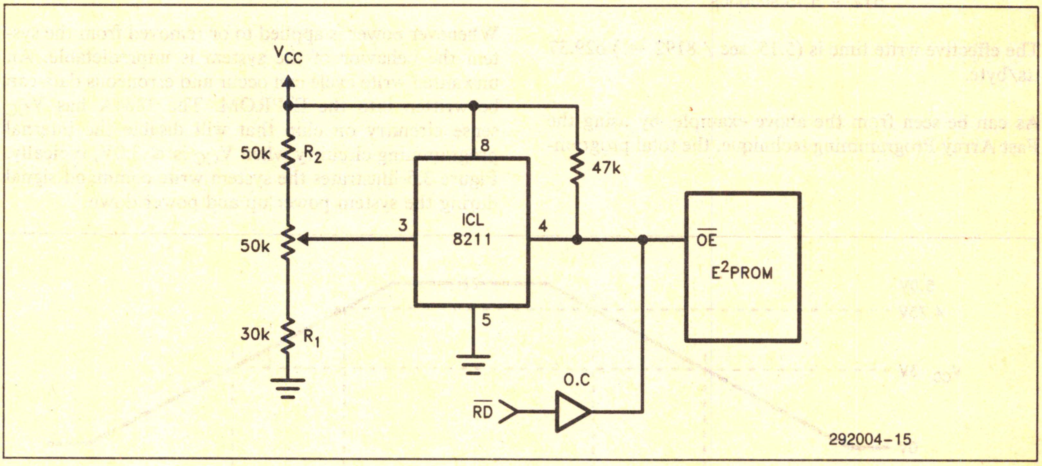


Figure 3.7. "Hold Low" Protection

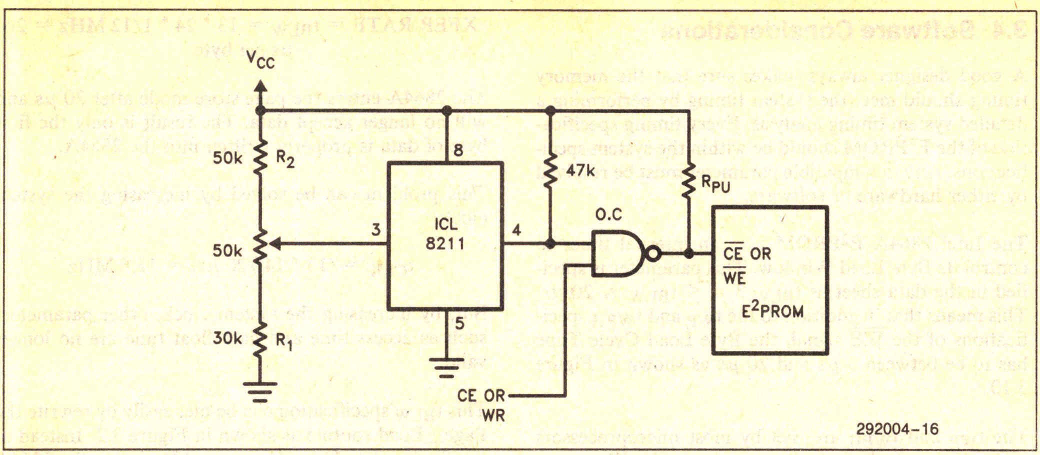
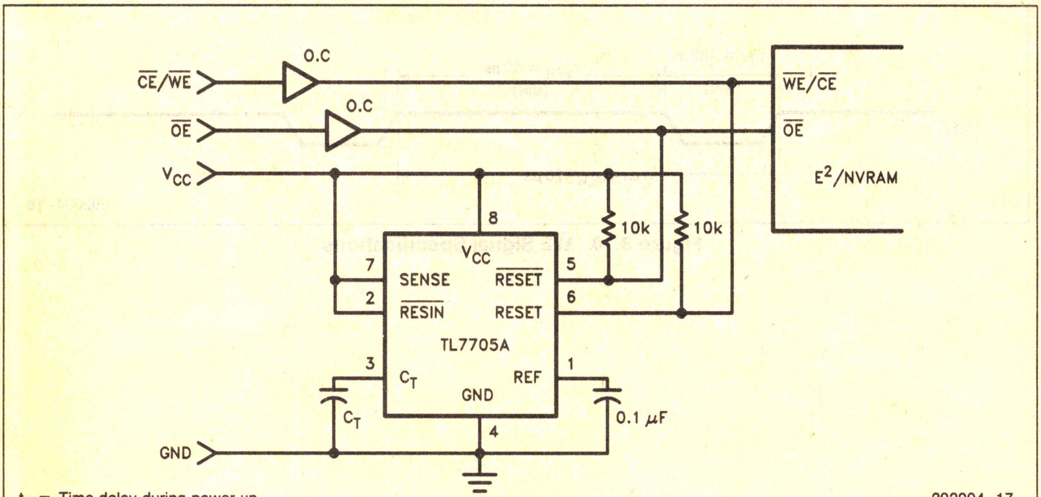

VCC
50k
R2
50k
30k
R1
8
3
4
5
ICL 8211
47k
RPU
O.C
CE OR WE
E2PROM
CE OR WR
292004-16

Figure 3.8. "Hold High" Protection

Another alternative is to use the Glitch Guard integrated circuit from Texas Instruments, the TL-7705A. During power-up or power-down, this device senses the supply voltage and keeps the Reset and $\overline{\text{Reset}}$ outputs active (high and low respectively) until the sensed voltage reaches its nominal value. The trip voltage is internally preset from 4.5V to 4.6V with 15 mV hysteresis. In addition, the outputs of the TL-7705A can be delayed until the system is stable and ready. Figure 3.9 is a sample circuit using the TL-7705A, either Held Low or Held High design can be used.

These circuits have been built and tested extensively. They have a very low sensitivity to the supply voltage or temperature variations and offer high accuracy voltage sensing. The components used are all readily available at low cost and occupy little board space.

DATA PROTECTION CIRCUIT USING TL7705A


CE/WE
OE
VCC
GND
O.C
O.C
WE/CE
OE
E2/NVRAM
10k
10k
8
VCC
7
SENSE
2
RESIN
RESET
5
RESET
6
TL7705A
3
CT
REF
1
GND
4
CT
0.1 µF
292004-17

t_d = Time delay during power up
= $1.3 \times 10^4 \times C_T$
C_T is in Farads
t_d is in seconds

Figure 3.9. Data Protection Circuit Using TL7705A

3.4 Software Considerations

A good designer always makes sure that the memory timing should meet the system timing by performing a detailed system timing analysis. Every timing specification of the E^2PROM should be within the system specifications. Any incompatible parameter must be resolved by either hardware or software.

The Intel 2864A E^2PROM uses an internal timer to control its Byte Load Window. This parameter is specified in the data sheet as t_{BLW} $3\ \mu \leq t_{BLW} \leq 20\ \mu s$. This means that in addition to the t_{WP} and t_{WPH} specifications of the $\overline{WE}$ signal, the Byte Load Cycle Time has to be between 3 μs and 20 μs as shown in Figure 3.10.

The t_{WP} and t_{WPH} are met by most microprocessors and microcontrollers during a write cycle. The t_{BLW} specifications of the 2864A require some considerations when writing the 2864A page load routine.

The "Page_Load" routine is outlined in Figure 3.11. This routine will transfer a page of data from the external Ram into the 2864A page buffer in a 12 MHz system. The page load begins at line 10 in this routine, with the first write command to the 2864A. The data transfer rate can be calculated by counting how many instructions must be executed before line 10 is executed again. In this example, the system must execute 13 instructions, each one requiring 24 clock cycles:

$$\text{XFER RATE} = t_{BLW} = 13 * 24 * 1/12\ \text{MHz} = 26\ \mu s \text{ per byte.}$$

The 2864A enters the page store mode after 20 μs and will no longer accept data. The result is only the first byte of data is properly written into the 2864A.

This problem can be solved by increasing the system clock:

$$t_{CLK} = (13 * 14)/20\ \mu s) = 15.6\ \text{MHz}$$

But, by increasing the system clock, other parameters such as access time and data float time are no longer valid.

This t_{BLW} specification can be met easily by rewrite the Page_Load routine as shown in Figure 3.2. Instead of tranferring data from the external Ram into the 2864A page buffer, the first part of this routine transfers data from external Ram into internal Ram of the 8051. Note that this part does not affect the t_{BLW} specification. The second part of the routine will transfer the data from internal Ram of the 8051 into the 2864A's page buffer. Since the 8051 does not have to fetch the data from the external world and the loop is now shorter (5 instructions or 96 clock cycles), the data transfer rate is much faster:

$$\text{XFER RATE} = t_{BLW} = 96 * 1/12\ \text{MHz} = 8.2\ \mu s \text{ per byte.}$$

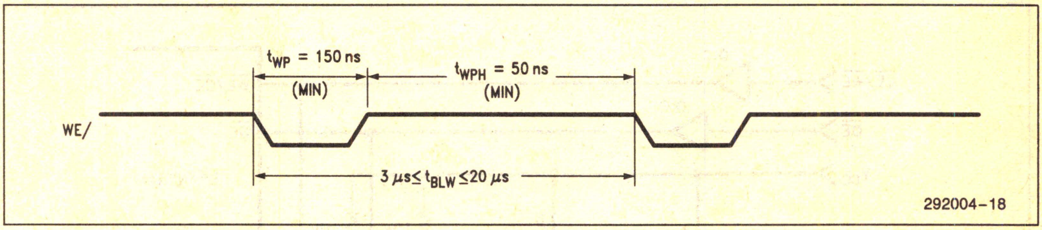
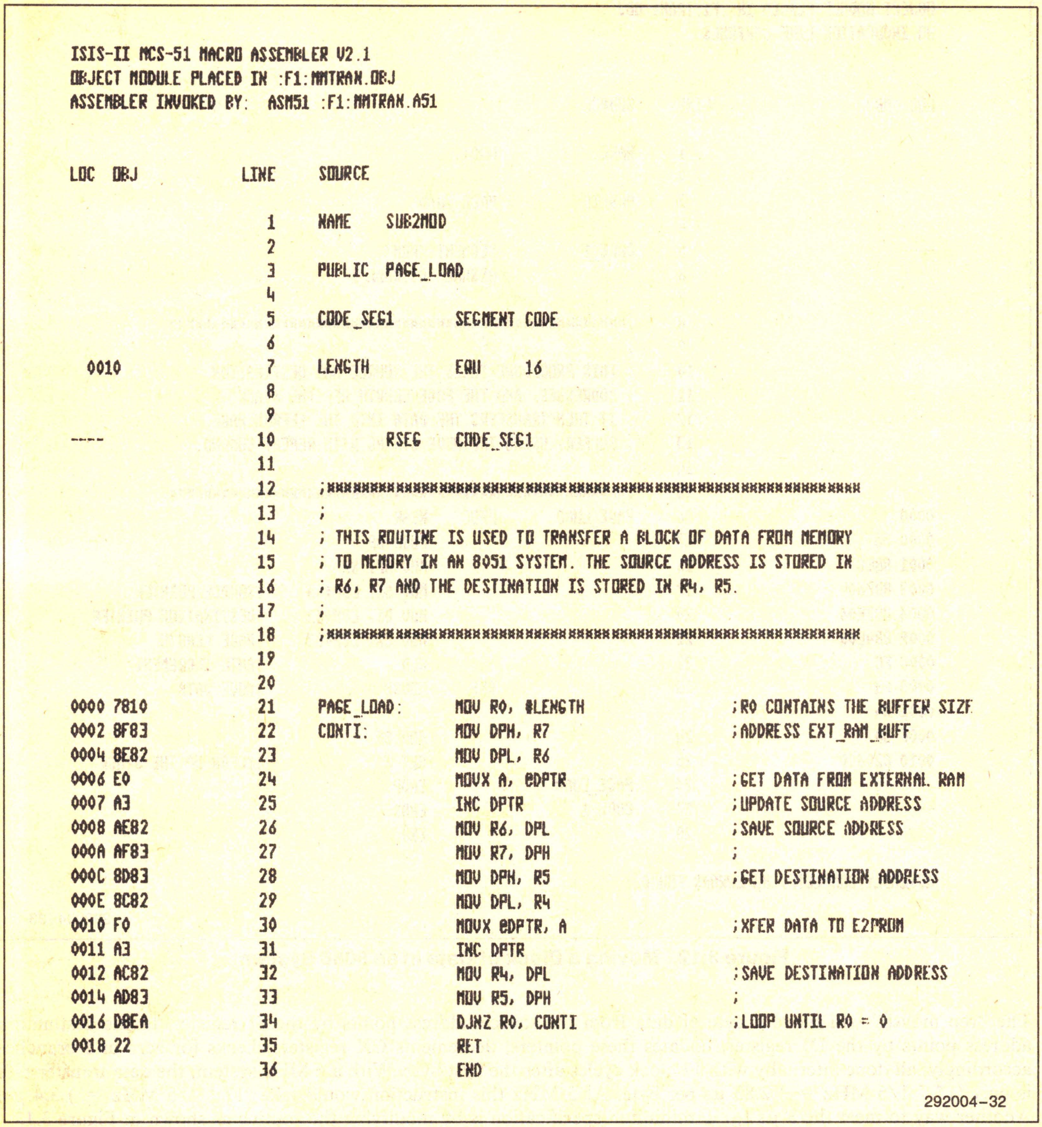


Figure 3.10. $\overline{\text{WE}}$ Signal Specifications

This routine will ensure to keep the 2864A in the Page Load Mode until all data is transferred.



```
ISIS-II MCS-51 MACRO ASSEMBLER V2.1
OBJECT MODULE PLACED IN :F1:MMTRAN.OBJ
ASSEMBLER INVOKED BY:  ASM51 :F1:MMTRAN.A51


LOC  OBJ            LINE     SOURCE

                       1     NAME     SUB2MOD
                       2
                       3     PUBLIC   PAGE_LOAD
                       4
                       5     CODE_SEG1        SEGMENT  CODE
                       6
  0010                 7     LENGTH           EQU     16
                       8
                       9
----                  10             RSEG     CODE_SEG1
                      11
                      12     ;**************************************************************
                      13     ;
                      14     ; THIS ROUTINE IS USED TO TRANSFER A BLOCK OF DATA FROM MEMORY
                      15     ; TO MEMORY IN AN 8051 SYSTEM. THE SOURCE ADDRESS IS STORED IN
                      16     ; R6, R7 AND THE DESTINATION IS STORED IN R4, R5.
                      17     ;
                      18     ;**************************************************************
                      19
                      20
0000 7810             21     PAGE_LOAD:       MOV R0, #LENGTH                  ;R0 CONTAINS THE BUFFER SIZE
0002 8F83             22     CONTI:           MOV DPH, R7                      ;ADDRESS EXT_RAM_BUFF
0004 8E82             23                      MOV DPL, R6
0006 E0               24                      MOVX A, @DPTR                    ;GET DATA FROM EXTERNAL RAM
0007 A3               25                      INC DPTR                         ;UPDATE SOURCE ADDRESS
0008 AE82             26                      MOV R6, DPL                      ;SAVE SOURCE ADDRESS
000A AF83             27                      MOV R7, DPH                      ;
000C 8D83             28                      MOV DPH, R5                      ;GET DESTINATION ADDRESS
000E 8C82             29                      MOV DPL, R4
0010 F0               30                      MOVX @DPTR, A                    ;XFER DATA TO E2PROM
0011 A3               31                      INC DPTR
0012 AC82             32                      MOV R4, DPL                      ;SAVE DESTINATION ADDRESS
0014 AD83             33                      MOV R5, DPH                      ;
0016 D8EA             34                      DJNZ R0, CONTI                   ;LOOP UNTIL R0 = 0
0018 22               35                      RET
                      36                      END
```

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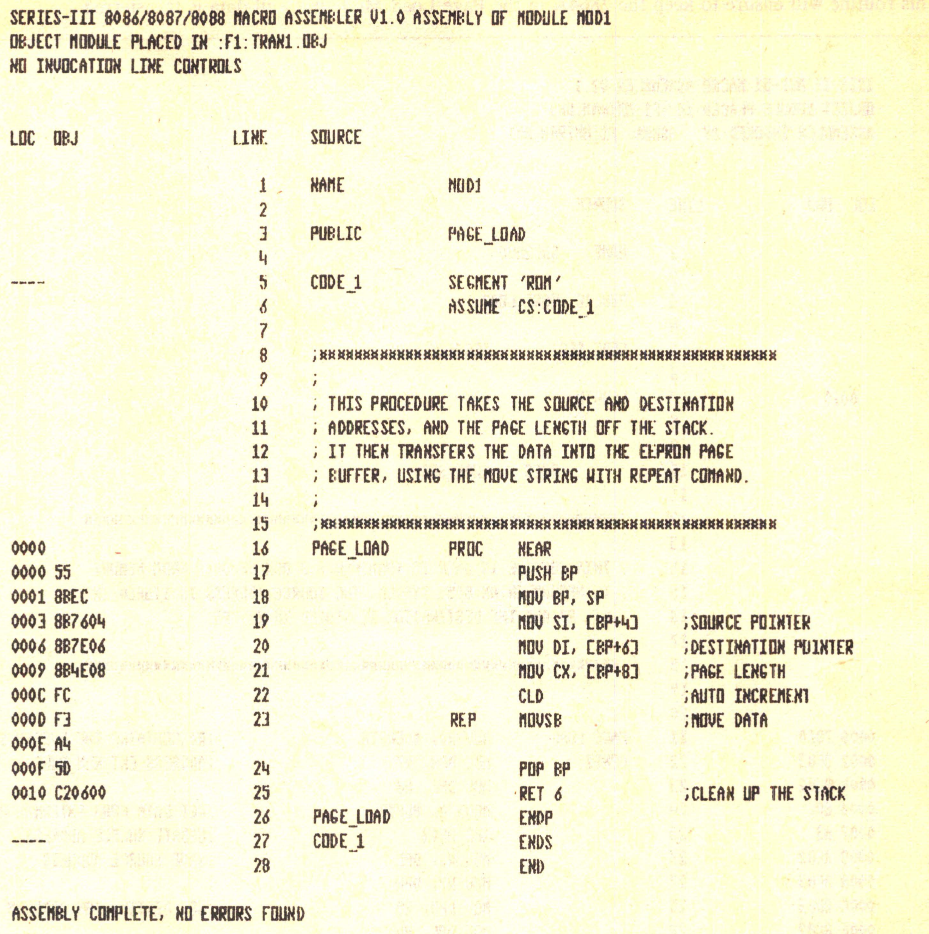
Figure 3.11. 8051 Code to Transfer Data From External Ram to the 2864A

Systems that do not support the "Block move" or "move String" instructions require the programmer to set up a loop and keep track of the pointers and the counter within the loop. In this case, the t_{BLW} max. specification (t_{BLW} max = 20 μs) can be easily violated as shown in the above example. Conversely, systems with the move string instructions is automatically handling the housekeeping and therefore may violate the t_{BLW} min. specification (t_{BLW} = 3 μs).

An example of how this spec could be violated can be shown via an 8086 system. A block of data can be moved within the system memory with one instruction as shown in Figure 3.12.



```
SERIES-III 8086/8087/8088 MACRO ASSEMBLER V1.0 ASSEMBLY OF MODULE MOD1
OBJECT MODULE PLACED IN :F1:TRAN1.OBJ
NO INVOCATION LINE CONTROLS


LOC  OBJ                 LINE     SOURCE

                            1     NAME            MOD1
                            2
                            3     PUBLIC          PAGE_LOAD
                            4
----                        5     CODE_1          SEGMENT 'ROM'
                            6                     ASSUME  CS:CODE_1
                            7
                            8     ;*****************************************************
                            9     ;
                           10     ; THIS PROCEDURE TAKES THE SOURCE AND DESTINATION
                           11     ; ADDRESSES, AND THE PAGE LENGTH OFF THE STACK.
                           12     ; IT THEN TRANSFERS THE DATA INTO THE EEPROM PAGE
                           13     ; BUFFER, USING THE MOVE STRING WITH REPEAT COMAND.
                           14     ;
                           15     ;*****************************************************
0000                       16     PAGE_LOAD       PROC    NEAR
0000 55                    17                             PUSH BP
0001 8BEC                  18                             MOV BP, SP
0003 8B7604                19                             MOV SI, [BP+4]      ;SOURCE POINTER
0006 8B7E06                20                             MOV DI, [BP+6]      ;DESTINATION POINTER
0009 8B4E08                21                             MOV CX, [BP+8]      ;PAGE LENGTH
000C FC                    22                             CLD                 ;AUTO INCREMENT
000D F3                    23                     REP     MOVSB               ;MOVE DATA
000E A4
000F 5D                    24                             POP BP
0010 C20600                25                             RET 6               ;CLEAN UP THE STACK
                           26     PAGE_LOAD               ENDP
----                       27     CODE_1                  ENDS
                           28                             END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

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Figure 3.12. Moving a Block of Data in an 8086 System

The "rep movsb" will move a byte of data from the source address points by the SI register, to the destination address points by the DI register, updates these pointers, decrements CX register, checks for zero and branches accordingly, all done internally with 17 clock cycles after the first byte. With a 6 MHz system, the data transfer rate is only (17 * 1/6 MHz =) 2.83 μs per byte. At 5 MHz this instruction would take (17 * 1/5 MHz =) 3.4 μs. Another way to meet the 3 μs t_{BLW} minimum specification is by modifying the routine as shown in Figure 3.13.

```
SERIES-III 8086/8087/8088 MACRO ASSEMBLER V1.0 ASSEMBLY OF MODULE MOD1
OBJECT MODULE PLACED IN :F1:TRAN2.OBJ
NO INVOCATION LINE CONTROLS


LOC  OBJ                LINE     SOURCE

                           1     NAME          MOD1
                           2
                           3     PUBLIC        PAGE_LOAD
                           4
----                       5     CODE_1        SEGMENT 'ROM'
                           6                   ASSUME  CS:CODE_1
                           7
                           8     ;*****************************************************
                           9     ;
                          10     ; THIS PROCEDURE TAKES THE SOURCE AND DESTINATION
                          11     ; ADDRESSES, AND THE PAGE LENGTH OFF THE STACK.
                          12     ; IT THEN TRANSFERS THE DATA INTO THE EEPROM PAGE
                          13     ; BUFFER, USING THE LOOP INSTRUCTION.
                          14     ;
                          15     ;*****************************************************
0000                      16     PAGE_LOAD     PROC     NEAR
0000 55                   17                          PUSH BP
0001 8BEC                 18                          MOV BP, SP
0003 8B7604               19                          MOV SI, [BP+4]      ;SOURCE POINTER
0006 8B7E06               20                          MOV DI, [BP+6]      ;DESTINATION POINTER
0009 8B4E08               21                          MOV CX, [BP+8]      ;PAGE LENGTH
000C FC                   22                          CLD                 ;AUTO INCREMENT
000D A4                   23     AGAIN:               MOVSB               ;MOVE DATA
000E E2FD                 24                          LOOP AGAIN          ;LOOP UNTIL CX = 0

0010 5D                   25                          POP BP
0011 C20600               26                          RET 6               ;CLEAN UP THE STACK
                          27     PAGE_LOAD            ENDP
----                      28     CODE_1               ENDS
                          29                          END

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

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Figure 3.13. Page Load Routine in an 8086 System that Meets t_{BLW} Specification

The "loop" prefix is used to replace the "rep" prefix. This instruction itself requires 17 cycles. The MOVSB requires 18 cycles and the data transfer rate can be calculated using the following formula:

$$\begin{array}{rl} \text{XFER\_RATE} &= (17 + 18) * t_{CYCLE} \\ \text{6 MHz system: XFER\_RATE} &= 35 * 166.66 \text{ ns} = 5.83\ \mu s \\ \text{8 MHz system: XFER\_RATE} &= 35 * 125.00 \text{ ns} = 4.37\ \mu s \\ \text{10 MHz system: XFER\_RATE} &= 35 * 100.00 \text{ ns} = 3.50\ \mu s \end{array}$$

3.5 Upgrade Path

The 2864A is available in a JEDEC standard 28-pin package, allowing a direct upgrade from the Intel 2817A, and to higher densities in future. Figure 3.14 shows an E^2PROM socket design that can accept the entire product family and Figure 3.15 shows the pinouts of 16K, 64K, and 256K E^2PROMs.

The 2864A is socket compatible with 2817A. A 2864A device can drop into an existing 2817A socket without any modifications. The 2864A follows the 28 pin JEDEC standard, the designer may connect the proper address line to any "NC" pin as suggested in Figure 3.14. A jumperable option on pin 1 allows upgradability from 16K up to the 256K density. Once the socket is so designed, the next upgrade will be a simple replacement.

3.6 Endurance And Data Retention

The 2864A has a minimum endurance of 10,000 write cycles per page with a 10 year data retention for each write cycle. This means that each page in the E^2PROM can be rewritten at least 10,000 times without degrading device operation, and that data will remain valid for at least 10 years.

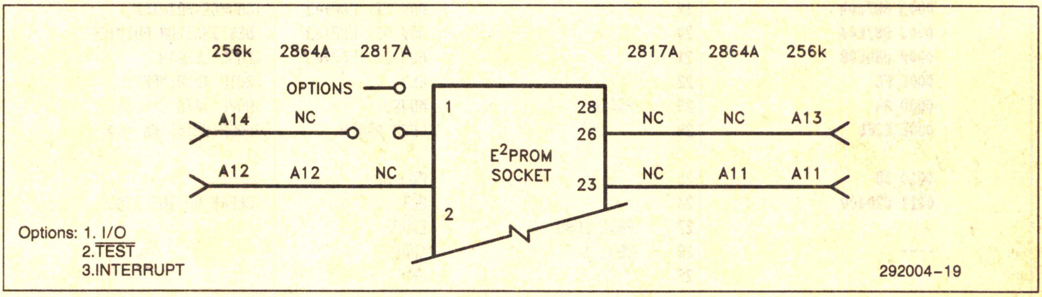
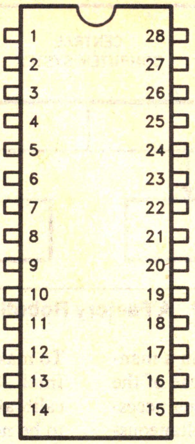


Figure 3.14. 28 Pin Site E^2PROM Socket

256K	2864A	2817A
A_{14}	NC	R/$\overline{B}$
A_{12}	A_{12}	NC
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
IO_0	IO_0	IO_0
IO_1	IO_1	IO_1
IO_2	IO_2	IO_2
GND	GND	GND



2817A	2864A	256K
V_{CC}	V_{CC}	V_{CC}
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
NC	NC	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
NC	NC	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
IO_7	IO_7	IO_7
IO_6	IO_6	IO_6
IO_5	IO_5	IO_5
IO_4	IO_4	IO_4
IO_3	IO_3	IO_3

292004-20

Figure 3.15. E^{2}PROM Pinouts

4.0 APPLICATIONS

4.1 Robotics

One of the most revolutionary concepts in industrial manufacturing environments is the use of robots for manufacturing processes. Automotive manufacturers for example, are using robots in painting, welding, as well as moving heavy objects. Robots reduce manufacturing cost and increase productivity. The Intel 2864A can make robotics more efficient and more intelligent through the capability of in-circuit reprogramming of its contents.

A modern robot can now perform several different tasks. System downtime caused by switching tasks becomes insignificant. In just a few seconds, a different application program can be downloaded to a robot station, instructing the robot to perform a new task. In addition, the robot can be either totally controlled by the system without human intervention or be "taught" by an operator.

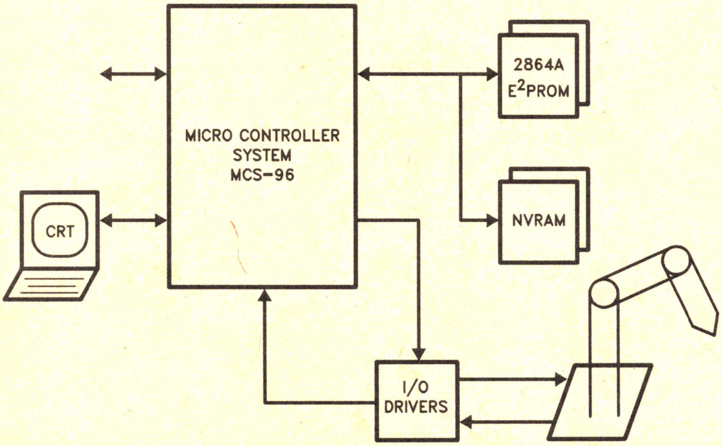


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Figure 4.1. A Typical Robot Station

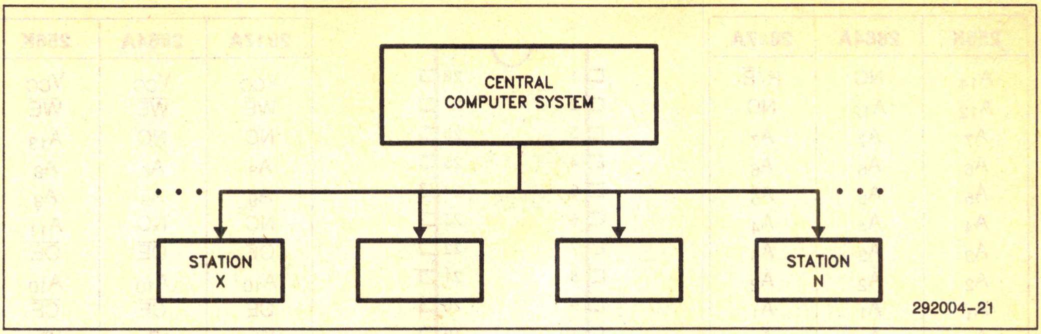


Figure 4.2. A Factory Robotics Network

The block diagram for a typical robot station in a manufacturing floor is shown in Figure 4.1. Because of the complex processing and numerical calculations necessary to control severals motors in a robot simultaneously, a high performance 16-bit microcontroller, such as the Intel 8096, is commonly used. The system boot code and the system control program are stored in the internal ROM of the 8096. NVRAMs are used as system ram in addition to the internal RAM of the 8096 during the system normal operation. In the event of a power corruption, critical system data is stored in the non-volatile portion of the NVRAM to provide an "Intelligent restart" capability. I/O drivers are used to provide necessary information and control signals to drive robot's motors as well as collect feedback from the robot. A serial communication channel is also available to connect the station to a host computer, or a factory robotics network as shown in Figure 4.2.

To make the system more flexible and cost effective, the Intel 2864As are used to store application programs, calibration parameters and other information the needs to be non-volatile but can still be changed dynamically while in system. A terminal also is available allowing an operator to "teach" the robot and gain control of the station.

Previous designs suffered from the ability to hold application programs in RAM in the case of power failure. The cost of down time of a production line makes it economical to use E^2PROM. The 2864A offers excellent reliability and environmental tolerance, in addition to high density and system flexibility, all needed for robotics systems.

4.2 Point Of Sale Terminal

With the capability of remote reconfiguration and high density, E^2PROM has proven to be a preferred memory for Point Of Sale Terminals. Pricing information and product descriptions are typically stored in memory in the form of look-up tables. There are three important characteristics associated with these tables:

1. Data contained within these tables must be retained when power is removed.
2. These tables must be large enough to accommodate several products with complex encoding schemes.
3. Data in these tables must be altered relatively easily as pricing and product information change frequently.

E^2PROM has all of the above characteristics and is found in many modern Point Of Sale Terminals. Figure 4.3 is a block diagram for such a system. The terminal is controlled by a high performance microcontroller. The 2864As are used for data look-up table storage. Typical I/O devices for a terminal also exist in the system as shown. The most important interface indicated in the block diagram is the serial Communication link. This datacom or telecom link provides the system with remote update capability. The contents of the 2864As can be changed from a central host computer without need for costly human service.

In addition to containing product description and pricing information, the 2864A can be used to store special data to a particular memory location for inventory purposes. For example, if a block of memory within the 2864A is set aside for reorder codes, then as a location runs short of a particular item, the system can automatically place a reorder request to the central computer. Another capability gained from the use of E^2PROM is that daily totals in sales volume and product quantities can also be stored in the 2864A. This information can be accessed by both the local store as well as the central office at anytime.

4.3 Operating System

With 64K bit density, the 2864A can now be used to store system firmware, operating system, or even application programs in a cost effective manner. There is a major advantage of using E^2PROM over EPROM in applications where data or programs are frequently updated. Frequent updates no longer prompt major service cost of sending a technician to each location to replace the EPROMs. With a simple phone call, a new software version can be sent to a remote system. Since the 2864A E^2PROM and the 2764A EPROM both use Jedec 28-pin sites, and both have the same density, the EPROM to E^2PROM conversion can be easily done with one jumper change as shown in Figure 4.4.

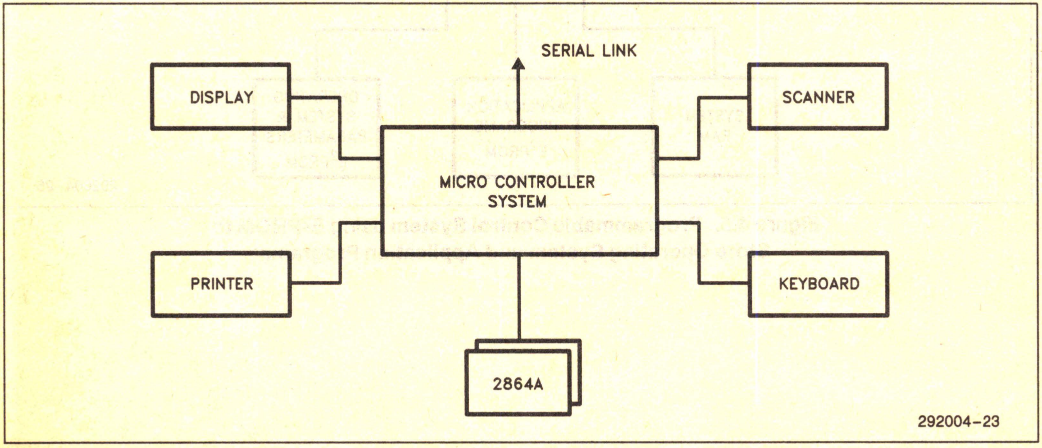


Figure 4.3. Point Of Sale Terminal Block Diagram

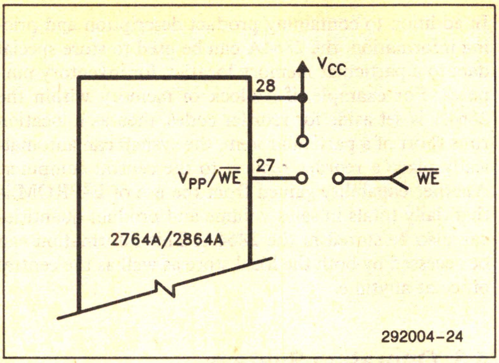

VCC
28
27
VPP/WE
WE
2764A/2864A
292004-24

Figure 4.4. 2764A to 2864B Conversion

Today's real time, multitasking operating system kernels are fast and powerful. Most require from 2K bytes to less than 30K bytes depending on features and capabilities. At the lowest level, the kernel communicates directly with the hardware. Part of the kernel, therefore, must be custom-tailored to each computer system's hardware features. The 2864A allows users to reconfigure the operating system to match various system's hardware. This is normally done by running an "install" program when the user first receives the system. In addition to that, other important parameters in an operating system, such as interrupt priority allocation, the maximum processor time allocated for each process or the "time slice", the number of mailboxed, etc., which vary with the applications and the system RAM can also be stored in the 2864A. Firmware patching or software updates can be done quicky and remotely with the cost of a phone call. Figure 4.5 shows a typical block diagram for a microprocessor system using 2864A to store the operating system.

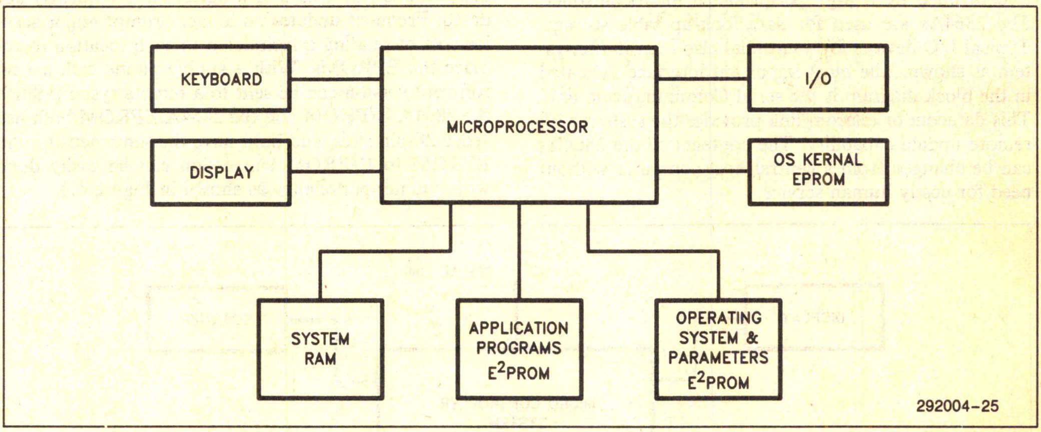

KEYBOARD
DISPLAY
MICROPROCESSOR
I/O
OS KERNAL EPROM
SYSTEM RAM
APPLICATION PROGRAMS E2PROM
OPERATING SYSTEM & PARAMETERS E2PROM
292004-25

Figure 4.5. Programmable Control System using E²PROM to Store Operating System and Application Programs

5.0 SUMMARY

In this application note, the operation of the 2864A has been discussed. Design considerations include $\overline{\text{DATA}}$ Polling, fast array programming technique and several data protection examples were detailed. Applications where E^{2}PROMs could be used to enhance system performance, eliminate service cost and improve system flexibility were shown. In summary, designing today's E^{2}PROMs with its "user friendly" characteristic has become a trivial task to the system designers.

6.0 APPENDIX

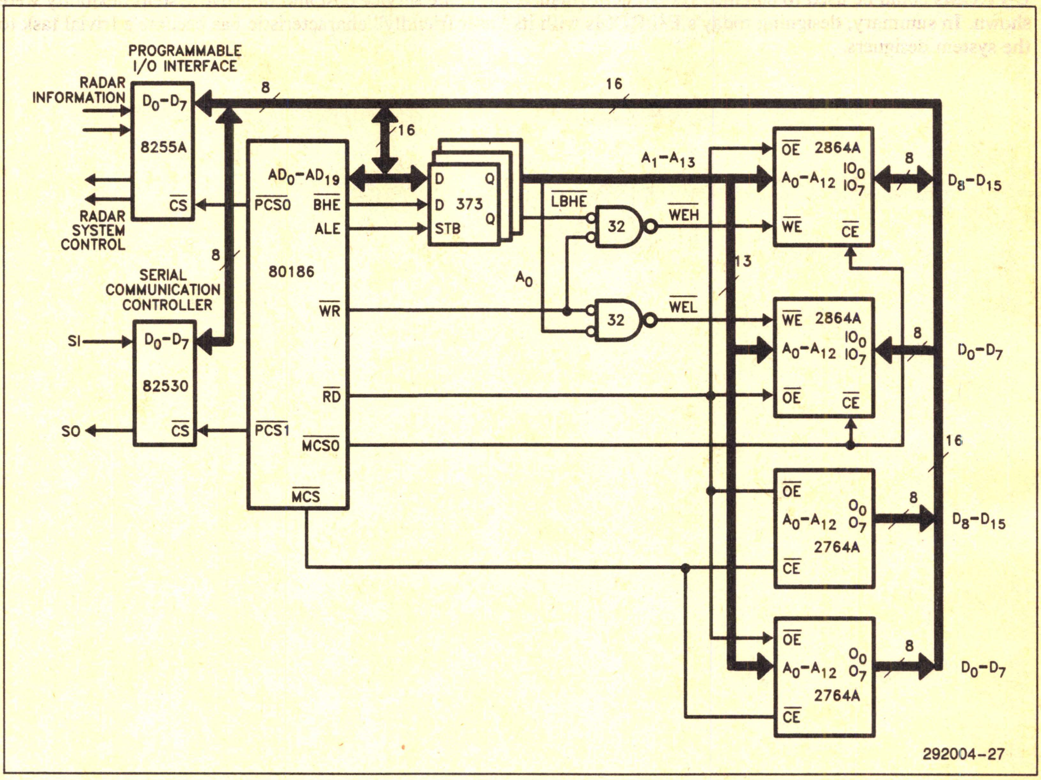

PROGRAMMABLE I/O INTERFACE
RADAR INFORMATION
D_0-D_7
8255A
CS
RADAR SYSTEM CONTROL
SERIAL COMMUNICATION CONTROLLER
SI
D_0-D_7
82530
SO
CS
8
8
16
16
AD_0-AD_{19}
PCS0
BHE
ALE
80186
WR
RD
PCS1
MCS0
MCS
D
Q
D 373
STB
Q
LBHE
A_0
32
32
WEH
WEL
A_1-A_{13}
13
OE 2864A
A_0-A_{12}
IO_0
IO_7
WE
CE
8
D_8-D_{15}
WE 2864A
A_0-A_{12}
IO_0
IO_7
OE
CE
8
D_0-D_7
16
OE
A_0-A_{12}
O_0
O_7
2764A
CE
8
D_8-D_{15}
OE
A_0-A_{12}
O_0
O_7
2764A
CE
8
D_0-D_7
292004-27

Figure 6.1. 2864A in a Real Time Process Controller with Remote Down Loading Capability

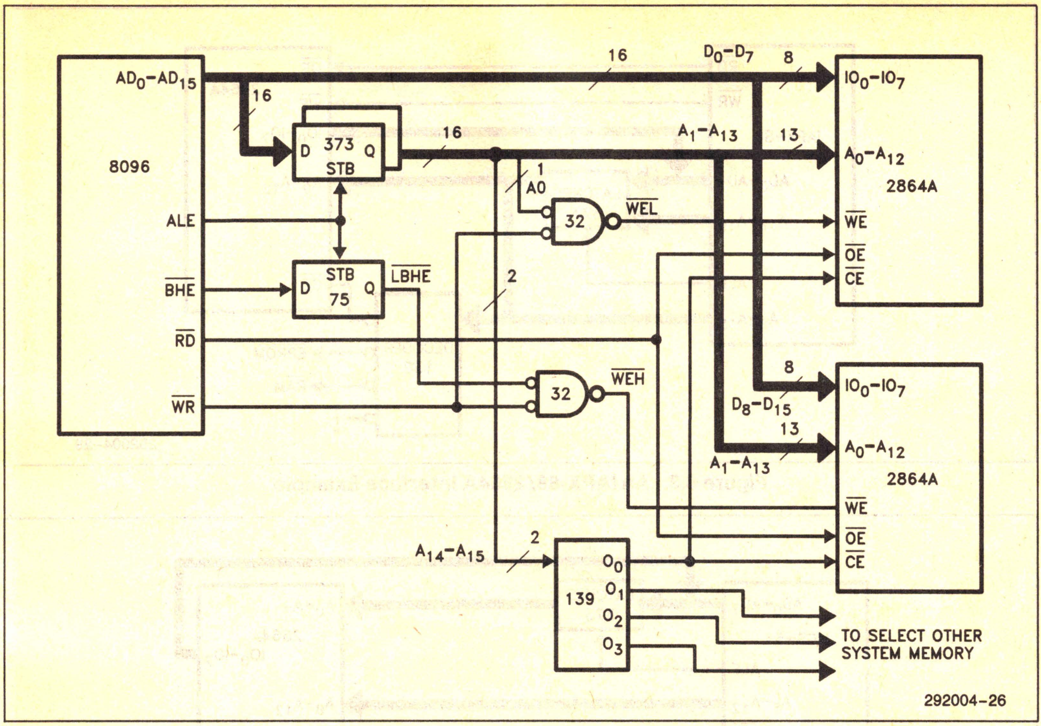

AD0–AD15
16
16
D0–D7
8
IO0–IO7
8096
D 373 Q
STB
16
A1–A13
13
A0–A12
2864A
1
A0
32
WEL
WE
ALE
OE
CE
STB
D Q
75
LBHE
BHE
2
RD
8
IO0–IO7
WEH
32
D8–D15
WR
13
A0–A12
A1–A13
2864A
WE
OE
A14–A15
2
O0
CE
139
O1
O2
O3
TO SELECT OTHER
SYSTEM MEMORY
292004-26

Figure 6.2. 2864A/8096 Interface

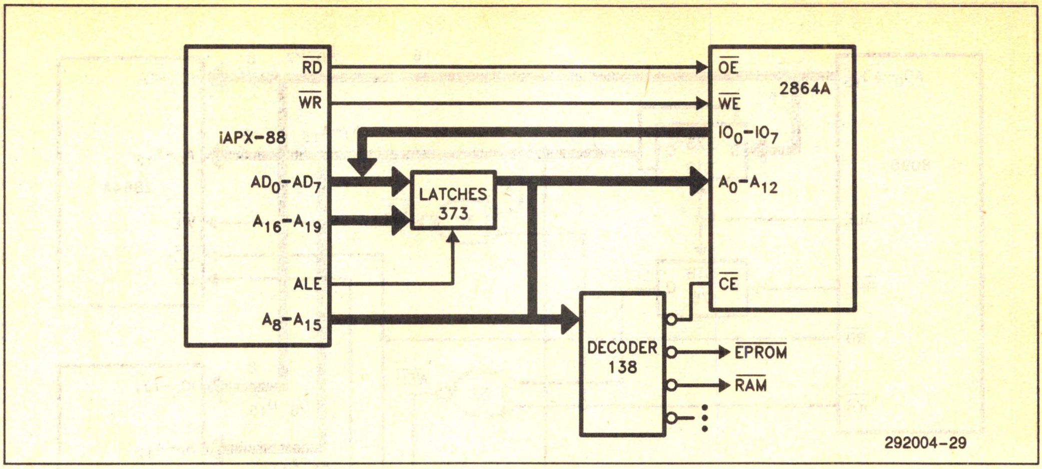

iAPX-88
$\overline{RD}$
$\overline{WR}$
AD_0-AD_7
$A_{16}-A_{19}$
ALE
A_8-A_{15}
LATCHES 373
DECODER 138
$\overline{OE}$
$\overline{WE}$
IO_0-IO_7
A_0-A_{12}
$\overline{CE}$
2864A
$\overline{EPROM}$
$\overline{RAM}$
292004-29

Figure 6.3. An iAPX-88/2864A Interface Example

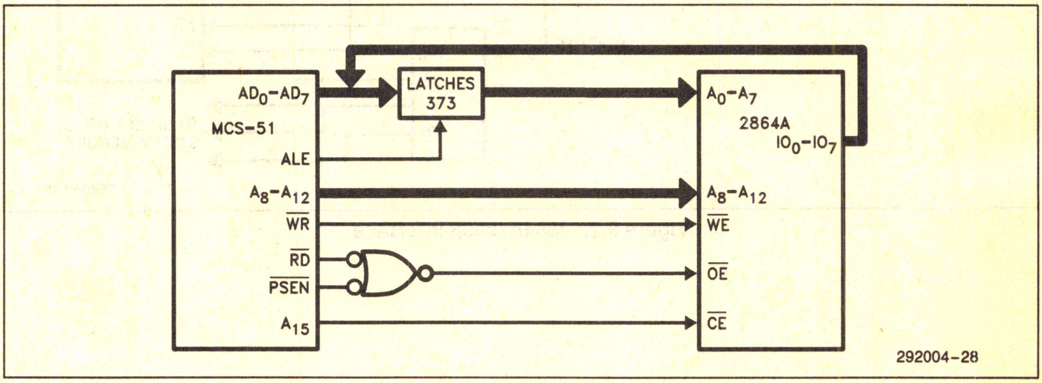

MCS-51
AD_0-AD_7
ALE
A_8-A_{12}
$\overline{WR}$
$\overline{RD}$
$\overline{PSEN}$
A_{15}
LATCHES 373
2864A
A_0-A_7
IO_0-IO_7
A_8-A_{12}
$\overline{WE}$
$\overline{OE}$
$\overline{CE}$
292004-28

Figure 6.4. 2864A In a MCS-51 System

intel®

RELIABILITY REPORT

RR-59B

November 1986

E²PROM and NVRAM Reliability Data Summary

© Intel Corporation, 1986

Order Number: 293001-002

THE IMPORTANCE OF RELIABILITY

Reliability of the non-volatile memories in your end product is critical to your total system reliability. The use of Intel E^{2}PROMs/NVRAMs can make a difference. Reliability is not just tested, but designed into each component Intel manufactures.

QUALITY ≠ RELIABILITY

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product. While Intel is a quality leader, we also adhere to stringent reliability standards which we have established for ourselves.

Consider Quality vs. Reliability

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end use of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

MONITOR PROGRAM

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is a proven tool that Intel has used since 1974 and is now available to its customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. But it's much more than burn-in and device testing. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program. It is the most comprehensive reliability program anywhere.

The paramount objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts—and the performance—that they ordered by specifying Intel. Reliability qualification assures that all new production meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained, day in, day out, over the duration of a device's life. This reliability improves the lifetime reputation of your product, reducing the required number of field service calls.

E^{2}PROM/NVRAM RELIABILITY DATA SUMMARY

Intel routinely publishes this "E^{2}PROM/NVRAM Reliability Data Summary", a continuing update of reliability information covering Intel's entire product line. This document includes a discussion on reliability testing methodology and the most current failure rate calculations, failure analyses and lifetest results.

Intel's commitment to the reliability of our products is clearly reflected in the information we make available to customers. We believe that supplying detailed reliability information to our customers is part of the total solution Intel offers, and is an important part of Intel's leadership in microelectronics technology.

E^{2}PROM/NVRAM RELIABILITY TESTING

Intel E^{2}PROM/NVRAMs undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and/or during ongoing monitor checks.

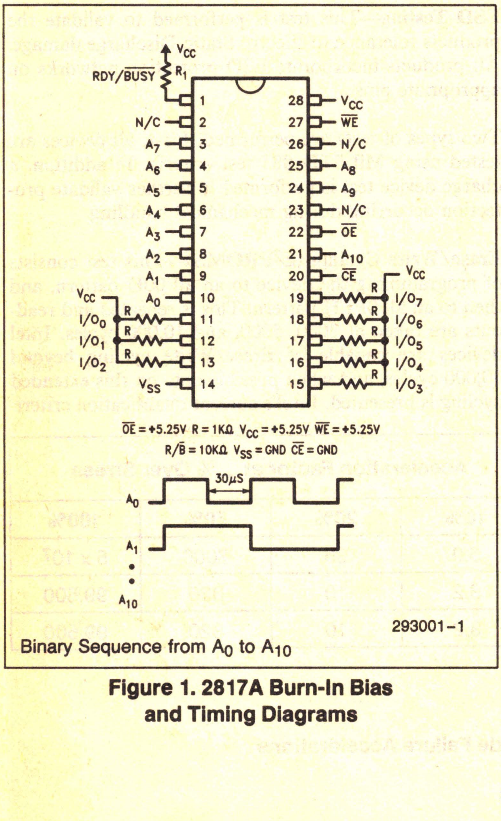
Intel continually reviews its testing procedures and makes improvements to its methodology whenever overall reliability can be enhanced. Our goal is to be the industry leader in delivering reliable parts and no compromises are accepted.

Information on Intel's reliability testing procedures follows.

High Temperature Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and the outputs are exercised, but not monitored or loaded. A checkerboard data pattern is used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with the failure analysis. In order to best determine long-term failure rate, all devices used for lifetesting are subjected to standard INTEL screening. The 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation. (See Figures 1 and 1A for typical burn-in bias and timing diagrams.)

Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy(1,2,3,4) and the Arrhenius Plot as shown in Figure 2*. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. The failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution to arrive at a confidence level associated failure rate. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Devices submitted to other stresses received a 168 hour lifetest prior to stressing.

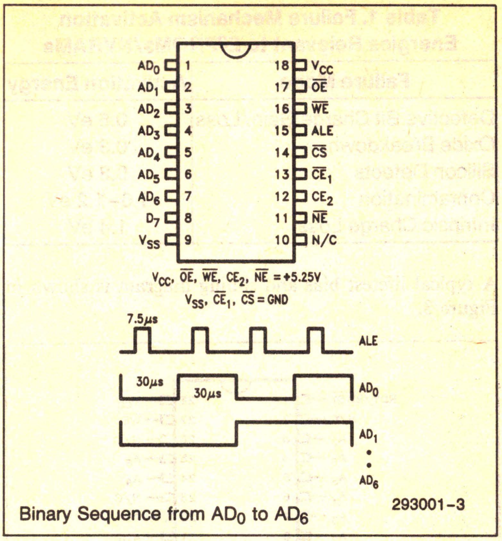
*The activation energies for various failure mechanisms are listed in Table 1.



V_{CC}
RDY/$\overline{BUSY}$
R_1
N/C
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0
V_{CC}
I/O_0
I/O_1
I/O_2
V_{SS}
R
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
V_{CC}
$\overline{WE}$
N/C
A_8
A_9
N/C
$\overline{OE}$
A_{10}
$\overline{CE}$
V_{CC}
I/O_7
I/O_6
I/O_5
I/O_4
I/O_3
$\overline{OE}$ = +5.25V R = 1KΩ V_{CC} = +5.25V $\overline{WE}$ = +5.25V
R/$\overline{B}$ = 10KΩ V_{SS} = GND $\overline{CE}$ = GND
30μS
A_0
A_1
A_{10}
293001-1

Binary Sequence from A_0 to A_{10}

Figure 1. 2817A Burn-In Bias and Timing Diagrams



AD_0
AD_1
AD_2
AD_3
AD_4
AD_5
AD_6
D_7
V_{SS}
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
V_{CC}
$\overline{OE}$
$\overline{WE}$
ALE
$\overline{CS}$
$\overline{CE}_1$
CE_2
$\overline{NE}$
N/C
V_{CC}, $\overline{OE}$, $\overline{WE}$, CE_2, $\overline{NE}$ = +5.25V
V_{SS}, $\overline{CE}_1$, $\overline{CS}$ = GND
7.5μs
ALE
30μs
30μs
AD_0
AD_1
AD_6
293001-3

Binary Sequence from AD_0 to AD_6

Figure 1A. 2001 Burn-In Bias and Timing Diagrams

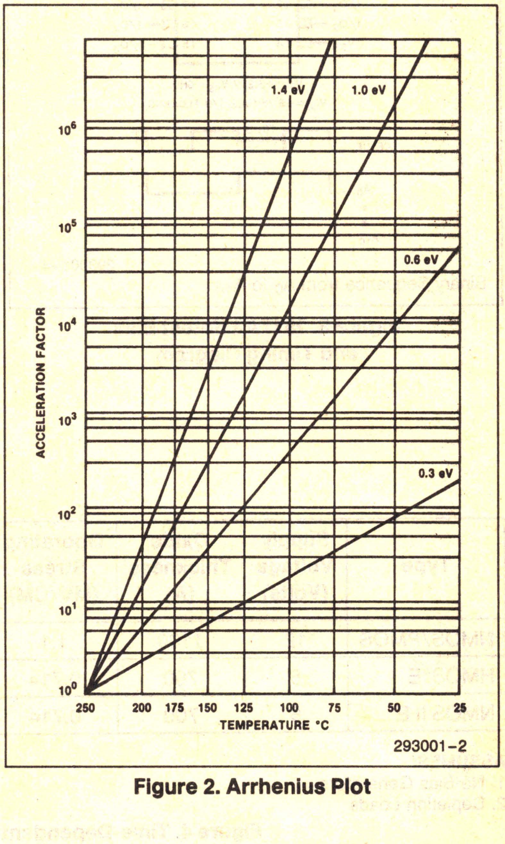
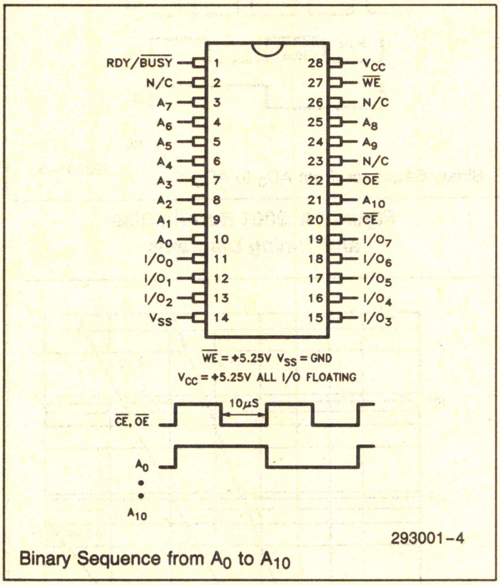


Figure 2. Arrhenius Plot

Table 1. Failure Mechanism Activation Energies Relevant to E²PROMs/NVRAMs

Failure Mode	Activation Energy
Defective Bit Charge Gain/Loss	0.6 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 eV
Contamination	1.0–1.2 eV
Intrinsic Charge Loss	1.4 eV

A typical lifetest bias and timing diagram is shown in Figure 3.



Binary Sequence from A_0 to A_{10}

Figure 3. 2817A Lifetest Bias and Timing Diagram

High Temperature 6.5V Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic lifetest except V_{CC} at 6.5V. The acceleration factor due to this test can be found in Figure 4. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 99% programmed pattern to a 150°C bake with no applied bias. In addition to data retention, this test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability. This test is sometimes referred to as *Data Retention Bake Test.*

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. **Two hundred cycles** are performed with a complete cycle taking 20 minutes. This test is to detect mechanical reliability problems and microcracks.

Low Temperature Lifetest—This test is performed at −10°C to detect the effects of **hot electron** injection into the gate oxide as well as package related failures (e.g., metal corrosion, etc.)[3].

ESD Testing—This test is performed to validate the products tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks on appropriate pins.

Two types of tests are performed. First, all devices are tested using Mil STD 883 test criteria. In addition, a charge device test is performed to further validate protection occurring during mechanical handling.

Erase/Write Cycling (E²PROMS)—This test consists of programming the device to an all 00H pattern, and then to an all 0FFH pattern. This is repeated and readouts are taken at 2000, 5000, and 10,000 cycles. Intel devices are capable of Erase/Write cycling beyond 10,000 cycles, and when possible data on this extended cycling is presented. Intel's current qualification criteri-

Type	Supply Voltage (Volts)	Oxide Thickness (A)	Operating Stress (MV/CM)	Acceleration Factor at __% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5 x 10^7
HMOS*E	5	700	0.714	3.2	10	320	99,500
NMOS II E	5	700	0.714	3.2	10	320	99,500

ASSUMES:
1. No Bias Generators
2. Depletion Loads

Figure 4. Time-Dependent Oxide Failure Accelerations

*HMOS and CHMOS are patented processes of Intel Corporation.

on is less than 5% failures in the specified number of cycles. This does not mean that after the specified number of cycles the device is no longer functional, but if the device is used in an application that requires more cycles than this, the failure rate may be unacceptable. Figure 5 shows a typical ELT bias and timing diagrams.

Store/Recall cycling (NVRAMS)—This test is the same as Erase/Write cycling except the entire device array is stored at once.

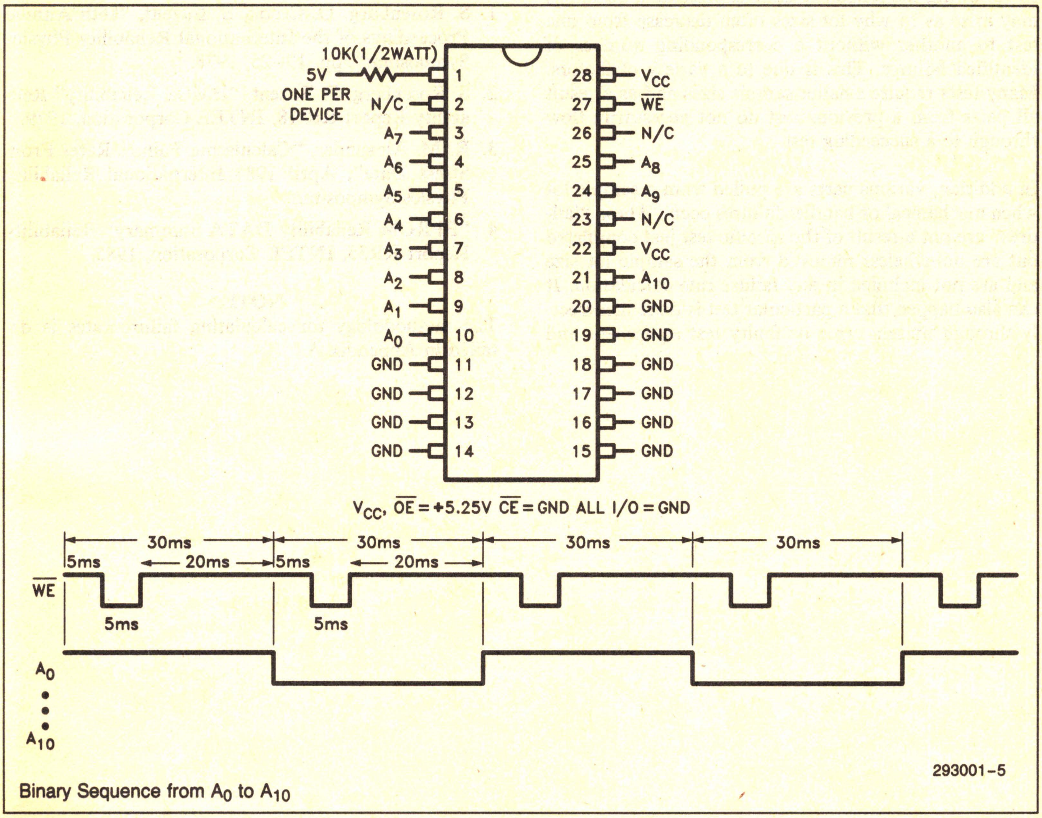

10K(1/2WATT)
5V
ONE PER DEVICE
1
N/C 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
GND 11
GND 12
GND 13
GND 14
28 VCC
27 WE
26 N/C
25 A8
24 A9
23 N/C
22 VCC
21 A10
20 GND
19 GND
18 GND
17 GND
16 GND
15 GND
VCC, OE = +5.25V CE = GND ALL I/O = GND
30ms
30ms
30ms
30ms
5ms
20ms
5ms
20ms
WE
5ms
5ms
A0
A10
293001-5
Binary Sequence from A0 to A10

Figure 5. 2817A Erase/Write Cycling ELT Configuration (85°C)

RELIABILITY DATA SUMMARY

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler failures occur. These "failures" are not a result of the specific test just completed but are nonetheless removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

REFERENCES

1. S. Rosenburg, D. Crook, B. Euzent, "16th Annual Proceedings of the International Reliability Physics Symposium", pp. 19–25, 1978.
2. S. Rosenberg, B. Euzent, "HMOS Reliability" Reliability Report RR-18, INTEL Corporation, 1979.
3. R. M. Alexander, "Calculating Failure Rates From Stress Data", April 1984 International Reliability Physics Symposium.
4. "EPROM Reliability DATA Summary" Reliability Report RR35, INTEL Corporation, 1985.

NOTE:

The methodology for calculating failure rates is detailed in Appendix A.

2001

The Intel 2001 (CERDIP) is a 1K Non-Volatile Random Access Memory (NVRAM).

Number of Bits:	1024
Organization:	128 x 8
Pin Out:	18 pin
Die Size:	112 x 155 mils
Process:	HMOS-E
Cell Size:	37.5 x 51.5 μM
Programming Voltage:	INTERNAL
Technology:	NMOS

Table 1. Reliability Data Summary

Lot ID	Burn-In		125° Lifetest		
	48 Hour	168 Hour	500 Hour	1000 Hour	2000 Hour
1984	1 / 839	2 / 838	0 / 298	0 / 297	0 / 297
1985	0 / 3494	1 / 3494	— —	— —	— —
Total	1 / 4333 (C)	3 / 4332 (D)	0 / 298 (E)	0 / 297 (F)	0 / 297 (G)

Lot ID	150°C Bake				High Voltage Lifetest			
	72 Hour	500 Hour	1000 Hour	2000 Hour	48 Hour	168 Hour	500 Hour	1000 Hour
1984	0 / 299	0 / 299	0 / 299	0 / 299	— —	— —	— —	— —
1985	— —	— —	— —	— —	0 / 216	0 / 216	— —	— —
Total	0 / 299 (R)	0 / 299 (S)	0 / 299 (T)	0 / 299 (U)	0 / 216 (N)	0 / 216 (O)	0 / 0 (P)	0 / 0 (Q)

Table 2. Failure Rate Predictions

Actual Device Hrs	AE (eV)	Equivalent Hours 55°C	Equivalent Hours 70°C	Lifetest Failures	Failure Rate/1000 Hr (60% U.C.L.) 55°C	Failure Rate/1000 Hr (60% U.C.L.) 70°C
1.06E+06	0.3	6.23E+06	4.02E+06			
3.63E+04	0.3 + 10	2.13E+06	1.37E+06	0	0.0123	0.0191
1.06E+06	0.6	3.65E+07	1.52E+07	0	0.0028	0.0068
1.06E+06	1.0	3.86E+08	8.96E+07	3	0.0011	0.0047
		Total Combined Failure Rate			0.0162	0.0305
				FIT	162	305

FAILURE ANALYSIS:

(C)

1984: 1 Charge Loss

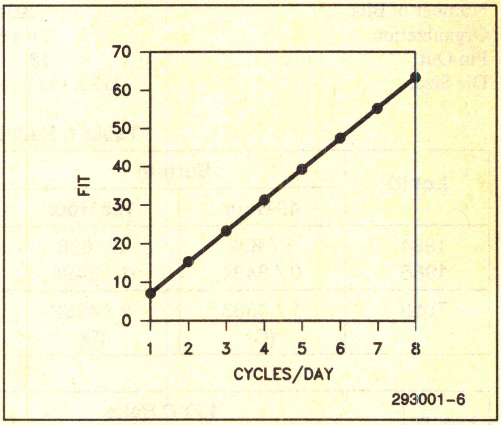
(D)

1984: 2 Functional (Contamination) 1.0 eV
1985: 1 Functional (Contamination) 1.0 eV

2001 (Continued)

Lot ID	Thousands of Erase Write Cycles		
	2	5	10
1984	1 / 525	0 / 524	0 / 523
Totals	1 / 525	0 / 524	0 / 523
	A	B	C

Failure Rate vs. Cycles/Day
2001



FAILURE ANALYSIS:

(A)

1984: 1 Charge Loss

2004

The Intel 2004 (CERDIP) is a 4K Non-Volatile Random Access Memory (NVRAM).

Number of Bits:	4096
Organization:	512 x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard

Die Size	161 x 188 mils
Process:	HMOS-E
Cell Size:	37.5 x 51.5 μM
Programming Voltage:	Internal
Technology:	NMOS

Table 1. Reliability Data Summary

	Burn-In		125°C Lifetest			Temp Cycles
Lot ID	**48 Hour**	**168 hour**	**500 Hour**	**1000 Hour**	**2000 Hour**	**200 Cycle**
1983	0 / 841	0 / 833	0 / 208	0 / 110	—— ——	0 / 83
1984	0 / 788	2 / 784	0 / 200	0 / 199	0 / 198	0 / 25
1985	0 / 4052	3 / 4052	0 / 207	0 / 207	0 / 207	—— ——
Total	0 / 5681 (C)	5 / 5669 (D)	0 / 615 (E)	0 / 516 (F)	0 / 405 (G)	0 / 108 (V)

150° Bake				
Lot ID	**72 Hour**	**500 Hour**	**1000 Hour**	**2000 Hour**
1983	2 / 339	6 / 337	0 / 106	—— ——
1984	0 / 200	0 / 200	0 / 200	0 / 200
1985	0 / 200	0 / 200	0 / 200	0 / 200
Total	2 / 739 (R)	6 / 737 (S)	0 / 506 (T)	0 / 400 (U)

Table 2. Failure Rate Predictions

Actual Device Hrs	AE (eV)	Equivalent Hours		Lifetest Failures	Failure Rate/1000 Hr (60% U.C.L.)	
		55°C	70°C		55°C	70°C
1.55E+06	0.3	9.06E+06	5.84E+06	0	0.0114	0.0176
1.55E+06	0.6	5.30E+07	2.20E+07	2	0.0059	0.0142
1.55E+06	1.0	5.59E+08	1.30E+08	3	0.0007	0.0032
Total Combined Failure Rate					0.0180	0.0351
				FIT	180	351

FAILURE ANALYSIS:

(D)

1984:	2 Functional 1.0 eV
1985:	2 Charge Gain 0.6 eV
1985:	1 Surface Charge 1.0 eV

(R)

1983: 2 Charge Loss

(S)

1983: 6 Charge Loss

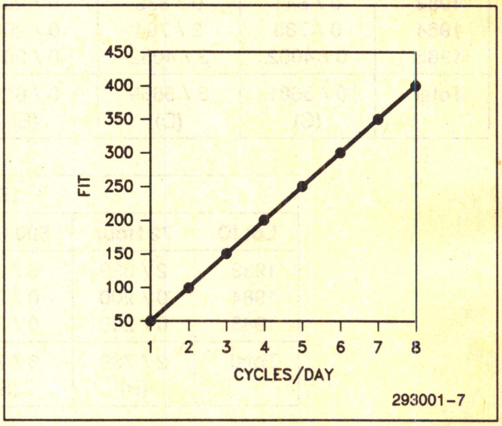
2004 (Continued)

Lot ID	Thousands of Erase Write Cycles						
	2	5	10	25	50	75	100
1983	0 / 828	8 / 828	8 / 819				
1984	0 / 345	0 / 343	12 / 343				
1985	0 / 742	4 / 742	6 / 738	1 / 372	2 / 371	1 / 369	8 / 368
Totals	0 / 1915	12 / 1913	26 / 1900	1 / 372	2 / 371	1 / 369	8 / 368
	A	B	C	D	E	F	G

FAILURE ANALYSIS:

1983 (B)	8 Charge Loss
1983 (C)	8 Charge Loss
1984 (C)	12 Charge Loss
1985 (B)	3 Charge Loss 1 Ram Fail
1985 (C)	5 Charge Loss 1 Ram Fail
1985 (D)	1 Charge Loss
1985 (E)	2 Charge Loss
1985 (D)	1 Charge Loss
1985 (G)	8 Charge Loss

Failure Rate vs. Cycles/Day
2004



2816A

The Intel 2816A is a 16K Electrically Erasable Programmable Read Only Memory (E^2PROM).

Number of bits:	16,384
Organization:	2K x 8
Pin Out:	24 pin, JEDEC Approved Industry Standard
Die Size:	128 x 182 mils
Process:	HMOS-E
Cell Size:	15 x 20 μM
Technology:	NMOS

Table 1. Reliability Data Summary

Lot ID	Burn-In		125°C Lifetest			Temp Cycles
	48 Hour	168 Hour	500 Hour	1000 Hour	2000 Hour	200 Cycle
F6 Q4	0 / 557	0 / 555	0 / 138	0 / 138	0 / 49	0 / 25
F6 Q5	0 / 527	0 / 527	0 / 125	0 / 125	—— ——	0 / 25
F6 Q6	0 / 682	0 / 682	0 / 128	0 / 128	0 / 98	0 / 25
F6 GOBI	0 / 2543	0 / 2543	—— ——	—— ——	—— ——	—— ——
Total	0 / 4309	0 / 4307	0 / 391	0 / 391	0 / 147	0 / 75
	(C)	(D)	(E)	(F)	(G)	(V)

Lot ID	150°C Bake			High Voltage Lifetest			
	72 Hour	500 Hour	1000 Hour	48 Hour	168 Hour	500 Hour	1000 Hour
F6 Q4	0 / 100	0 / 100	0 / 100	0 / 100	0 / 100	0 / 100	0 / 50
F6 Q5	0 / 100	0 / 100	0 / 100	0 / 100	0 / 100	0 / 100	—— ——
F6 Q6	0 / 100	0 / 100	0 / 100	—— ——	—— ——	—— ——	—— ——
F6 GOBI	—— ——	—— ——	—— ——	—— ——	—— ——	—— ——	—— ——
Total	0 / 300	0 / 300	0 / 300	0 / 200	0 / 200	0 / 200	0 / 50
	(R)	(S)	(T)	(N)	(O)	(P)	(Q)

Table 2. Failure Rate Predictions

Actual Device Hrs	AE (eV)	Equivalent Hours		Lifetest Failures	Failure Rate/1000 Hr (60% U.C.L.)	
		55°C	70°C		55°C	70°C
9.89E+05	0.3	5.13E+06	3.50E+06			
1.25E+05	0.3 + 10	6.48E+06	4.42E+06	0	0.0089	0.0130
9.89E+05	0.6	2.66E+07	1.24E+07	0	0.0039	0.0083
9.89E+05	1.0	2.38E+08	6.69E+07	0	0.0004	0.0015
Total Combined Failure Rate					0.0132	0.0229
				FIT	132	229

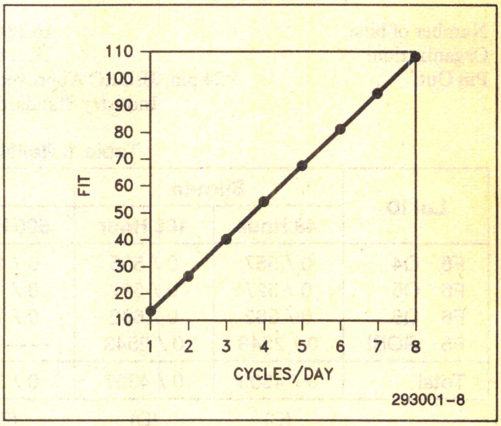
2816A (Continued)

D2816A			
Lot ID	**Thousands of Erase Write Cycles**		
	2	**5**	**10**
F6 Q4	1 / 213	0 / 210	0 / 207
F6 Q5	0 / 211	0 / 207	0 / 205
F6 Q6	1 / 198	0 / 197	0 / 197
Totals	2 / 622	0 / 614	0 / 609
	A	B	C

FAILURE ANALYSIS:

F6 Q4 (A) 1 Column failure
F6 Q6 (A) 1 Byte latch-up

Failure Rate vs. Cycles/Day
D2816A



2817A

The Intel 2817A is a 16K Electrically Erasable Programmable Read Only Memory (E^2PROM)

Number of bits:	16,384
Organization:	2K x 8
Pin Out:	28 pin, JEDEC Approved Industry Standard
Die Size:	132 x 206 mils
Process:	HMOS-E
Cell Size:	15 x 20 μM
Programming Voltage:	Internal
Technology:	NMOS

Table 1. Reliability Data Summary

Lot ID	Burn-In		125°C Lifetest			Temp Cycles		
	48 Hour	168 Hour	500 Hour	1000 Hour	2000 Hour	200 Cycle	500 Cycle	1000 Cycle
F6Q1	0 / 345	0 / 345	1 / 69	0 / 68	——	0 / 25	0 / 25	0 / 25
F6Q2	0 / 445	1 / 445	0 / 111	0 / 111	0 / 100	0 / 25	0 / 25	0 / 25
F6Q3	0 / 438	0 / 438	0 / 75	0 / 75	0 / 49	0 / 25	0 / 25	0 / 25
F6GOBI	3 / 5200	4 / 5197	——	——	——	——	——	——
506-201	0 / 1014	0 / 1014	0 / 100	0 / 99	——	0 / 78	0 / 78	0 / 78
515-202	0 / 1241	0 / 1239	0 / 100	0 / 99	——	0 / 78	0 / 78	0 / 78
518-204	0 / 1040	1 / 1019		——	——	——	——	——
523-200	0 / 736	0 / 733	0 / 100	0 / 100	——	0 / 78	0 / 78	0 / 78
528-202	0 / 943	0 / 952	0 / 100	——	——	0 / 78	1 / 78	0 / 78
532-205	0 / 939	0 / 933	——	——	——	——	——	——
534-202	0 / 1058	0 / 1058	——	——	——	——	——	——
537-206	0 / 1017	0 / 1017	——	——	——	——	——	——
Total	3 / 14416	6 / 14390	1 / 655	0 / 552	0 / 149	0 / 387	1 / 387	0 / 387
	(C)	(D)	(E)	(F)	(G)	(V)	(W)	(X)

Lot ID	150°C Bake			High Voltage Lifetest			
	72 Hour	500 Hour	1000 Hour	48 Hour	168 Hour	500 Hour	1000 Hour
F6 Q1	0 / 67	1 / 67	0 /66	——	——	——	——
F6 Q2	0 / 109	0 / 109	0 /109	0 / 100	0 / 100	0 / 100	——
F6 Q3	0 / 74	0 / 74	0 / 74	0 / 75	0 / 75	0 / 75	0 / 50
Total	0 / 250	1 / 250	0 / 249	0 / 175	0 / 175	0 / 175	0 / 50
	(R)	(S)	(T)	(N)	(O)	(P)	(Q)

2817A (Continued)

Table 2. Failure Rate Predictions

Actual Device Hrs	AE (eV)	Equivalent Hours		Lifetest Failures	Failure Rate/1000 Hr (60% U.C.L.)	
		55°C	70°C		55°C	70°C
2.37E+06	0.3	1.23E+07	8.39E+06			
1.13E+05	0.3 + 10	5.83E+06	3.98E+06	0	0.0057	0.0083
2.37E+06	0.6	6.36E+07	2.97E+07	2	0.0049	0.0105
2.37E+06	1.0	5.71E+08	1.60E+08	5	0.0011	0.0039
Total Combined Failure Rate					0.0117	0.0228
				FIT	117	228

FAILURE ANALYSIS:

(C)

F6GOBI: 1 Row Oxide Breakdown
F6GOBI: 1 Byte Mode Failure
F6GOBI: 1 Programming Time Failure

(D)

F6Q2: 1 Charge Gain 0.6 eV
F6GOBI: 1 Access Time Degradation 1 eV
F6GOBI: 1 Shorted Contact 1 eV
F6GOBI: 2 Programming Time Failure 1 eV
518–204: 1 Broken Bond Wire 1 eV

(E)

F6Q1: 1 Charge Gain 0.6 eV

(S)

F6Q1: 1 charge Gain

(W)

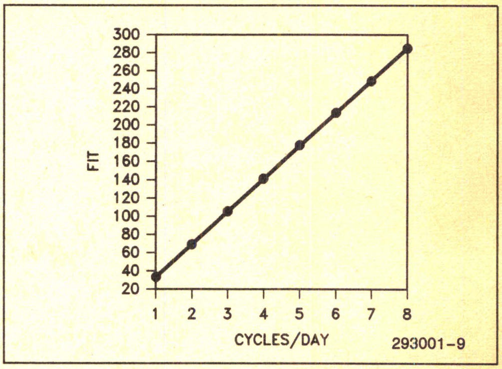
528–202: 1 Fails to Block Program

Lot ID	Thousands of Erase Write Cycles			
	2	5	10	20
F6 Q1	0 / 169	0 / 169	1 / 169	4 / 168
F6 Q2	1 / 192	1 / 190	0 / 190	
F6 Q3	1 / 193	0 / 192	0 / 192	3 / 192
HG qual 1	0 / 100	0 / 100	0 / 100	
HG qual 2	0 / 80	0 / 80	0 / 80	
HG qual 3	0 / 100	1 / 100	1 / 100	
515–202	0 / 100	0 / 100	0 / 100	
506–201	0 / 100	0 / 100	0 / 100	
Totals	2 / 1034	1 / 1031	2 / 1031	7 / 360

FAILURE ANALYSIS:

F6 Q1 (C) leaky bit
F6 Q1 (D) leaky bit on 4 units
F6 Q2 (A) row oxide breakdown
F6 Q2 (B) column failure
F6 Q3 (A) byte latch-up
F6 Q3 (D) leaky bit on 3 units
HG qual 3 (C) leaky bit

Failure Rate vs. Cycles/Day
2817A



2864A

The Intel 2864A is a 64K Electrcially Erasable Programmable Read Only Memory (E^2PROM).

Number of Bits: 65,536
Organization: 8K x 8
Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 217 x 166 mils
Process: NMOS
Cell Size: 17 x 12 μM
Programming Voltage: Internal
Technology: NMOS

Table 1. Reliability Data Summary

Lot ID	Burn-In		125°C Lifetest		
	48 Hour	168 Hour	500 Hour	1000 Hour	2000 Hour
Q1	0 / 274	1 / 274	0 / 97	0 / 96	0 / 88
Q2	0 / 275	0 / 275	0 / 100	0 / 100	0 / 100
Q3	1 / 473	0 / 471	0 / 95	0 / 88	0 / 43
Q4	0 / 194	0 / 194	— —	— —	— —
Q5	0 / 195	0 / 195	— —	— —	— —
PQ1	4 / 622	0 / 618	0 / 100	— —	— —
PQ2	2 / 635	0 / 629	0 / 100	— —	— —
PQ3	2 / 631	0 / 629	0 / 100	— —	— —
DQ1	0 / 144	0 / 144	0 / 48	0 / 48	0 / 48
GOBI 1 2k GA	2 / 504	2 / 447	— —	— —	— —
GOBI 1 4k GA	0 / 504	1 / 480	— —	— —	— —
GOBI 2 2k GA	2 / 535	1 / 532	— —	— —	— —
GOBI 2 4k GA	2 / 542	3 / 511	— —	— —	— —
GOBI 3 2k GA	2 / 505	— —	— —	— —	— —
GOBI 3 4k GA	0 / 496	— —	— —	— —	— —
MON1 GA	0 / 500	0 / 500	0 / 100	— —	— —
6.5V ELT GA	0 / 98	0 / 98	— —	— —	— —
Total	17 / 7029	8 / 5899	0 / 740	0 / 332	0 / 279
	(C)	(D)	(E)	(F)	(G)

Lot ID	250°C Bake				Temp Cycles	
	48 Hour	168 Hour	500 Hour	1000 Hour	200 Cycles	500 Cycles
Q1	0 / 50	0 / 50	0 / 50	0 / 50	0 / 75	0 / 75
Q2	0 / 50	0 / 50	0 / 50	0 / 50	0 / 75	0 / 75
Q3	0 / 50	0 / 50	0 / 50	0 / 50	0 / 78	0 / 78

2864A (Continued)

Table 2. Failure Rate Predictions

Actual Device Hrs	AE (eV)	Equivalent Hours 55°C	Equivalent Hours 70°C	Lifetest Failures	Failure Rate/1000 Hr (60% U.C.L.) 55°C	Failure Rate/1000 Hr (60% U.C.L.) 70°C
1.40E+06	0.3	7.25E+06	4.95E+06			
1.65E+04	0.3 + 10	8.53E+05	5.83E+05	1	0.0257	0.0376
1.40E+06	0.6	3.76E+07	1.75E+07	0	0.0027	0.0059
1.40E+06	1.0	3.37E+08	9.45E+07	7	0.0025	0.0089
Total Combined Failure Rate					0.0309	0.0523
				FIT	309	523

FAILURE ANALYSIS:

(C)

Q3: Infant Cycling
PQ2: Infant Cycling
PQ1: Infant Cycling
PQ3: Infant Cycling
GOBI1 2k: 1 Contamination
1 Page Timing
GOBI2 2k: 2 Contamination
GOBI2 4k: 2 Contamination
GOBI3 2k: 2 Leaky Oxides

(D)

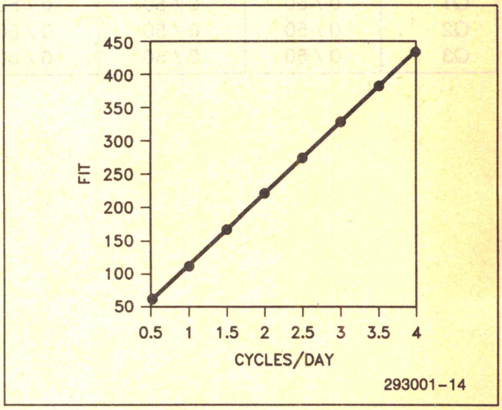
Q1: Half of the Array Won't Program 0.3 eV
GOBI1 2k: 2 Contamination
GOBI1 4k: Broken Bond Wire
GOBI2 2k: Contamination
GOBI2 4k: 3 Contamination

Lot ID	Thousands of Erase Write Cycles 2.5	5	7.5	10
Qual 1+2	2 / 200	3 / 198	0 / 195	1 / 192
Qual 3	0 / 107	0 / 107	0 / 107	2 / 107
Totals	2 / 307	3 / 305	0 / 302	3 / 299
	A	B	C	D

FAILURE ANALYSIS:

Qual 1 (A) oxide short trap up
Qual 1 (B) 2-oxide shorts trap up
Qual 1 (D) oxide short
Qual 3 (D) single row failure

Failure Rate vs. Cycles/Day
2864A



APPENDIX A
FAILURE RATE CALCULATIONS FOR 60% UPPER CONFIDENCE LEVEL

Step 1. Accumulate data from 48 hours of burn-in through lifetest of each lot. (Note: 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation.)

Step 2. Determine the failure mechanism for each failure and assign an activation energy (E_A) corresponding to each failure mechanism. (See Table 1 below.)

Table 1. Failure Mechanisms Activation Energies Relevant to E²PROMs/NVRAMS

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours from 48 hours of burn-in through lifetest.

Example: 125°C Burn-In/Lifetest and a 2 lot sample

$$\frac{X}{Y} = \frac{\#\text{ failures}}{\text{total }\#\text{ devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0 / 1000	1 / 1000	0 / 999	0 / 998	0 / 994
Lot #2	0 / 221	0 / 201	1 / 201	1 / 100	0 / 99
Totals	0 / 1221	0 / 1201	1 / 1200	1 / 1098	0 / 1093

Device Hours = (Number of Devices) (Number of Hours)

$$\begin{aligned}\text{Total Device Hours} &= 1201\ (168\text{ hrs} - 48\text{ hrs}) + 1200\ (500\text{ hrs} - 168\text{ hrs})\\ &\quad + 1098\ (1000\text{ hrs} - 500\text{ hrs}) + 1093\ (2000\text{ hrs} - 1000\text{ hrs})\\ &= 1201\ (120\text{ hrs}) + 1200\ (332) + 1098\ (500\text{ hrs})\\ &\quad + 1093\ (1000\text{ hrs})\\ &= 2.185 \times 10^6\text{ Device Hours}\end{aligned}$$

Step 4. Use E_A tables to find the equivalent device hours to a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \bullet \exp\left[\frac{E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°Kelvin (Boltzmann's constant)

A = proportionality constant

R = mean rate to failure

E_A = activation energy

T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A \bullet \exp\left[\frac{E_A}{KT_1}\right]}{A \bullet \exp\left[\frac{E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

$$R_1 = R_2 \bullet \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398.15$°K, $T_1 = 328.15$°K

$$R_2 = 0.024\ R_1, \text{ or } R_1 = 41.7\ R_2$$

Therefore, 1 hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy $E_A = 0.6$ eV. then 41.7 is the thermal acceleration factor for ΔT.

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:

The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the desired and actual burn-in/lifetest temperatures.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\ (IV\ @\ T_{Ambient}) + T_{ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	# Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

Using the data table and the equation below, the failure rates for individual failures mechanisms and the total combined failure rate can be predicted. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL:

$$\%\ \text{Fail/1K Hours} = \left[\frac{1.049\ (\#\ \text{failures for a particular } E_A) + 1.0305}{\text{Equivalent Hrs @ } T_1}\right]\left[10^5\right]$$

Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient} = 125°C$ and I_{CC} active is 65 mA at $T_{Ambient} = 55°C$.

Also assume that $\theta_{JA} = 35°C/W$.

Then,

$$T_2 = (35°C/W)\ (57\ mA)\ (5V) + 125°C$$

$$\approx 135°C = 408.15°K$$

$$T_1 = (35°C/W)\ (60\ mA)\ (5V) + 55°C$$

$$\approx 65°C = 338.15°K$$

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C % Fail/ 1K Hrs
0.3	2.185×10^6	5.85	1.278×10^7	0	0.0081
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
			Total Combined Failure Rate =		0.0126
			=		126 FITs

Example 2:

Assume that an additional lot of 800 HMOS*-E devices is burned in using a 6.5 V lifetest. Using Table 2 below, a voltage acceleration factor of 55 results from a 20% overstress (5.5V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0 / 800	1 / 800	0 / 799

$$\text{Device Hours} = 800\ (48\ hrs - 0\ hrs) + 800\ (168\ hrs - 48\ hrs) + 799\ (500\ hrs - 168\ hrs)$$

$$= 3.997 \times 10^5$$

Table 2. Time-Dependent Oxide Failure Accelerations

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/CM)	Acceleration Factor at __% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5×10^7
HMOS*E	5	700	0.714	3.2	10	320	99,500
NMOS II E	5	700	0.714	3.2	10	320	99,500

ASSUMES:

1. No Bias Generators
2. Depletion Loads

*HMOS is a patented process of Intel Corporation.

Since this voltage accelerated stress is used to predict an oxide breakdown failure rate, the 5.5V burn-in/lifetest 55°C equivalent hours for $E_A = 0.3$ eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours as follows:

125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C
5.5V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 × 55)	1.286×10^8
			Total Equivalent $E_A = 0.3$ eV Device Hours =	1.414×10^8

The following failure rate predictions include the total equivalent 55°C, $E_A = 0.3$ eV device hours found above:

E_A (eV)	Actual Device Hours @125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C	# Fail	55°C % Fail/ 1K Hrs
0.3	2.185×10^6	5.85	—	—	—
0.3 + 55(1)	3.997×10^5	(5.85 × 55)	1.414×10^8	1	0.0015
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
				Total Combined Failure Rate =	0.0060
				=	60 FITs

NOTES:

1. The notation 0.3 + 55 is used to show that 6.5V and 5.5V burn-in lifetest equivalent hours have been combined.
2. Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.

APPENDIX B
E²PROM/NVRAM BIT MAPS AND DIE PHOTOGRAPHS

X-DECODER

HEX	AD3	AD2	AD1	AD0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

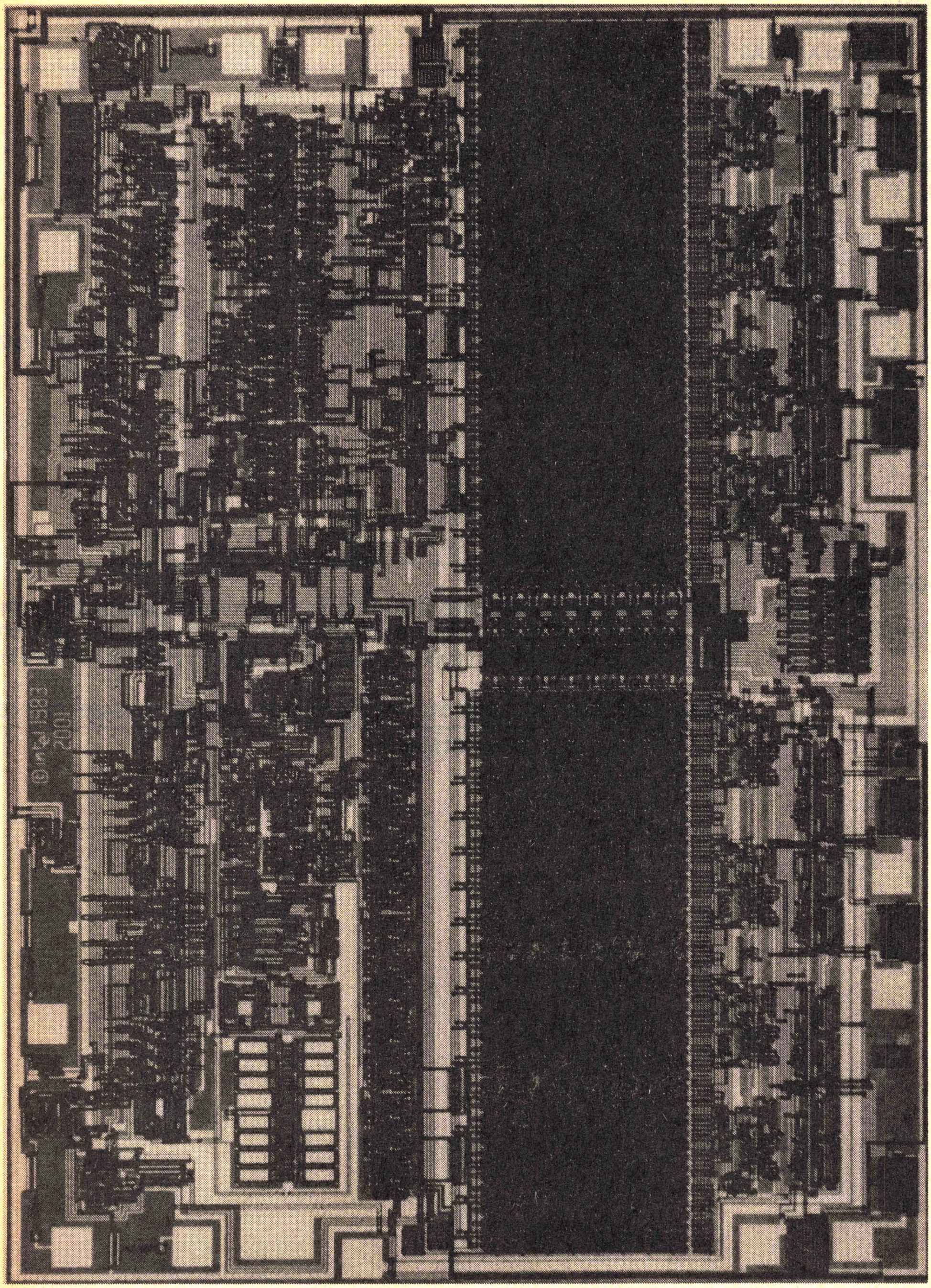
AD0	AD1	AD2	AD3	AD4	AD5	AD6	D7
OUTPUT 0	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6	OUTPUT 7

Y-DECODER

BINARY								
AD4	01010101	01010101	01010101	01010101	01010101	10101010	10101010	10101010
AD5	00110011	00110011	00110011	00110011	00110011	11001100	11001100	11001100
AD6	00001111	00001111	00001111	00001111	00001111	11001100	11001100	11001100
HEX	01234567	01234567	01234567	01234567	01234567	76543210	76543210	76543210

NOTE:
Outputs 0–4 are identical, outputs 5–7 are mirrored.

2001 Bit Map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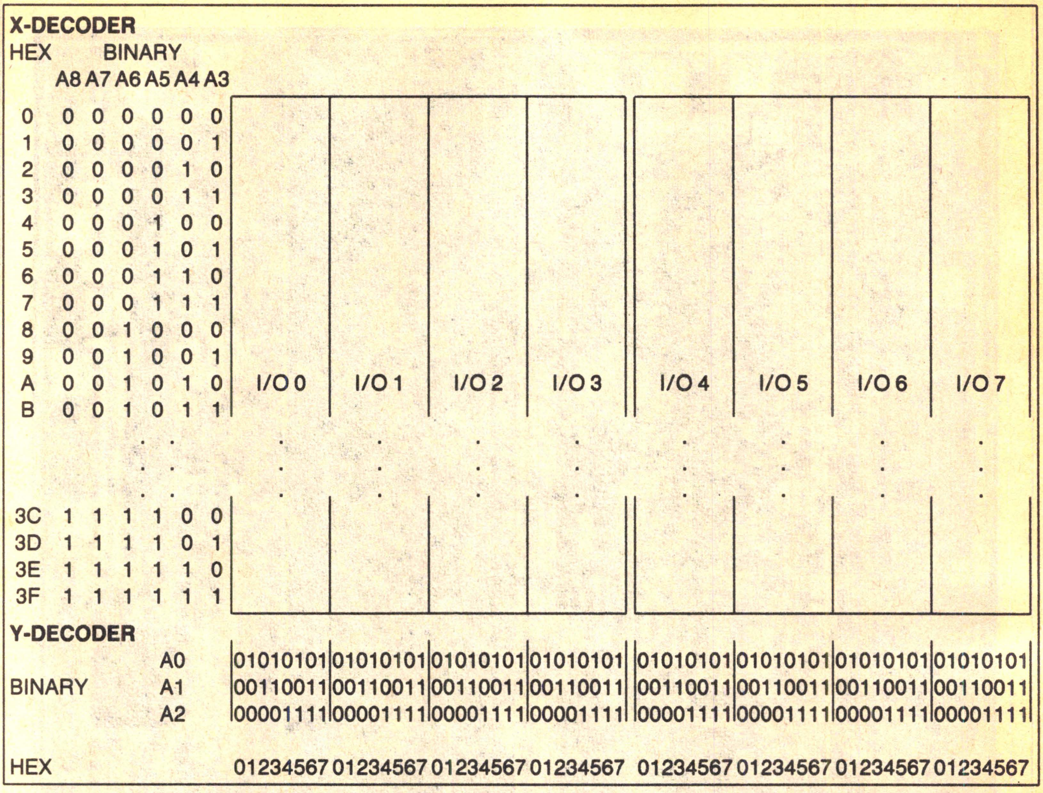
2001

293001-10

2001 Die Photograph



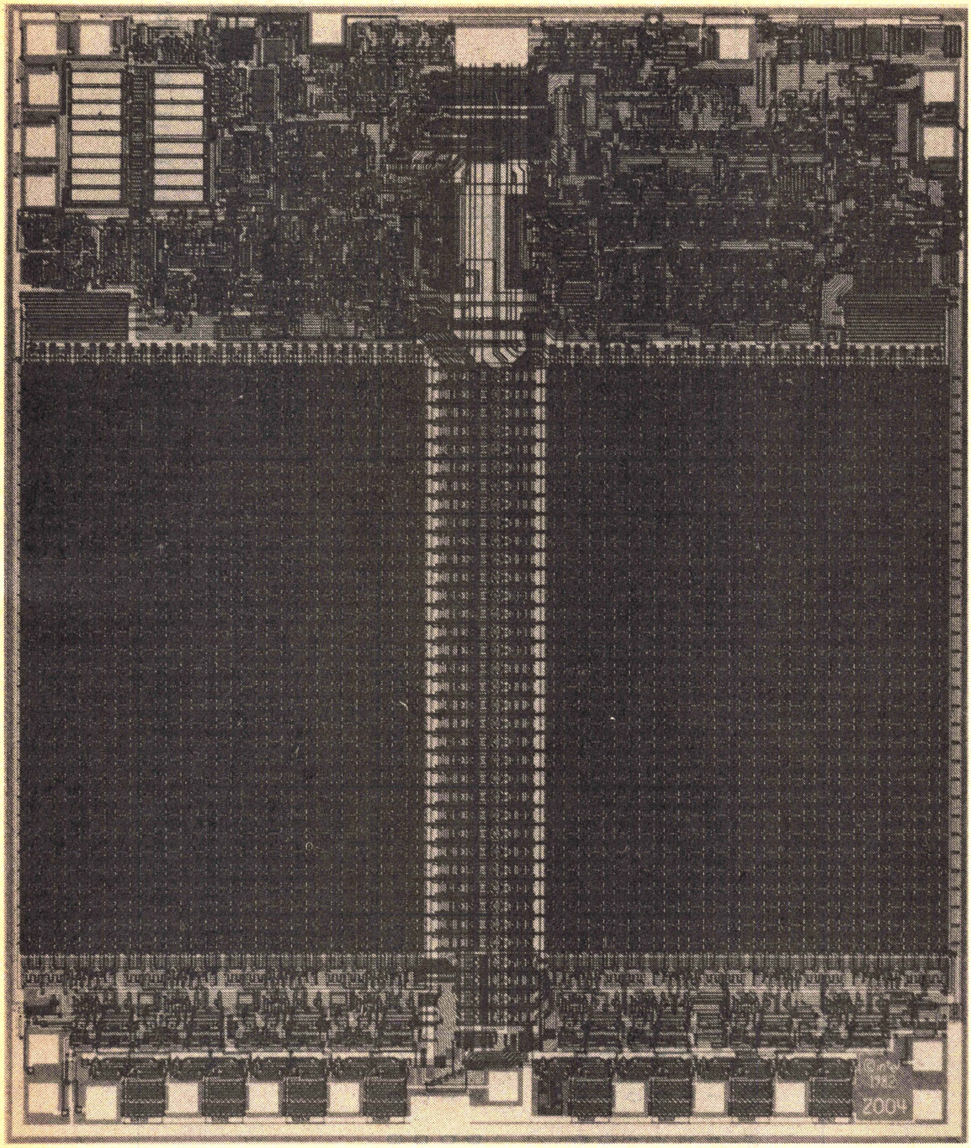
X-DECODER

HEX	A8	A7	A6	A5	A4	A3
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	0	0	1	0	0	1
A	0	0	1	0	1	0
B	0	0	1	0	1	1
.			.	.		
3C	1	1	1	1	0	0
3D	1	1	1	1	0	1
3E	1	1	1	1	1	0
3F	1	1	1	1	1	1

Y-DECODER

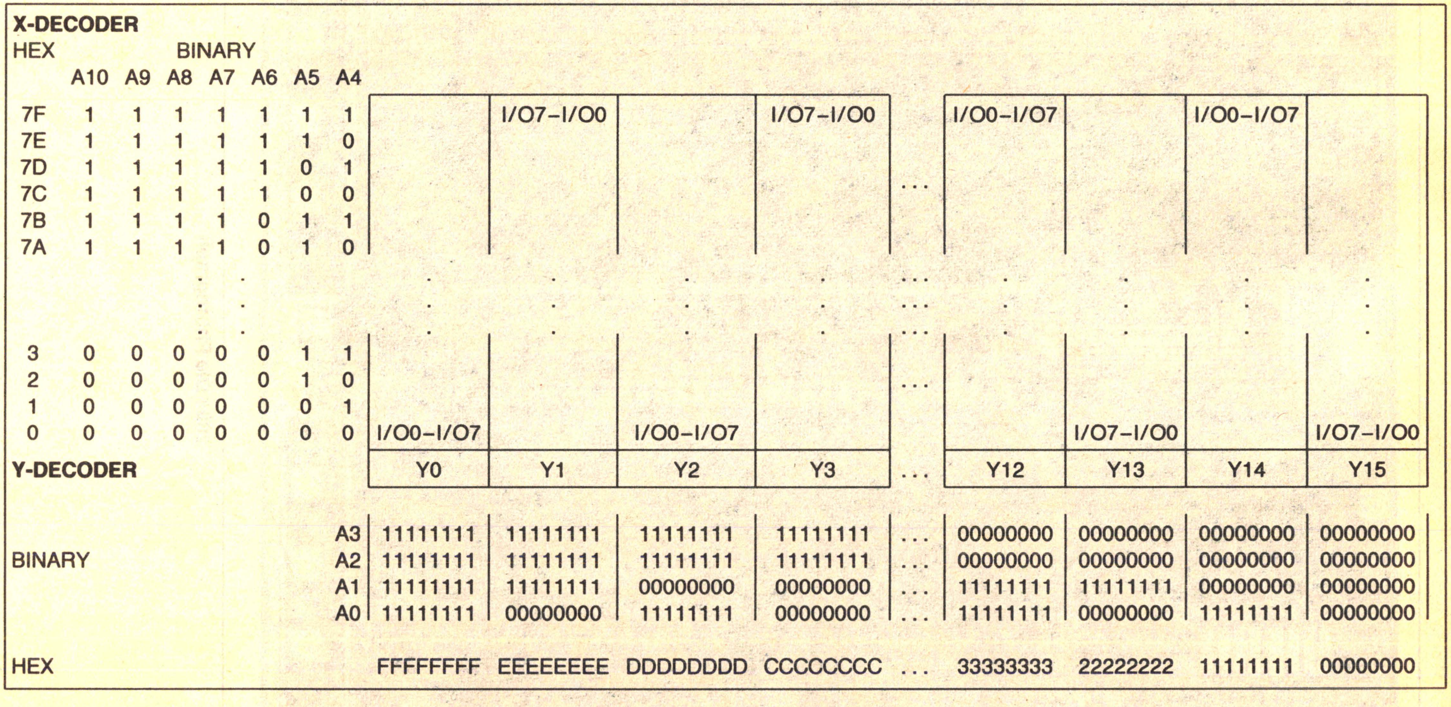
		I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
BINARY	A0	01010101	01010101	01010101	01010101	01010101	01010101	01010101	01010101
	A1	00110011	00110011	00110011	00110011	00110011	00110011	00110011	00110011
	A2	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
HEX		01234567	01234567	01234567	01234567	01234567	01234567	01234567	01234567

2004 Bit Map



293001-11

2004 Die Photograph



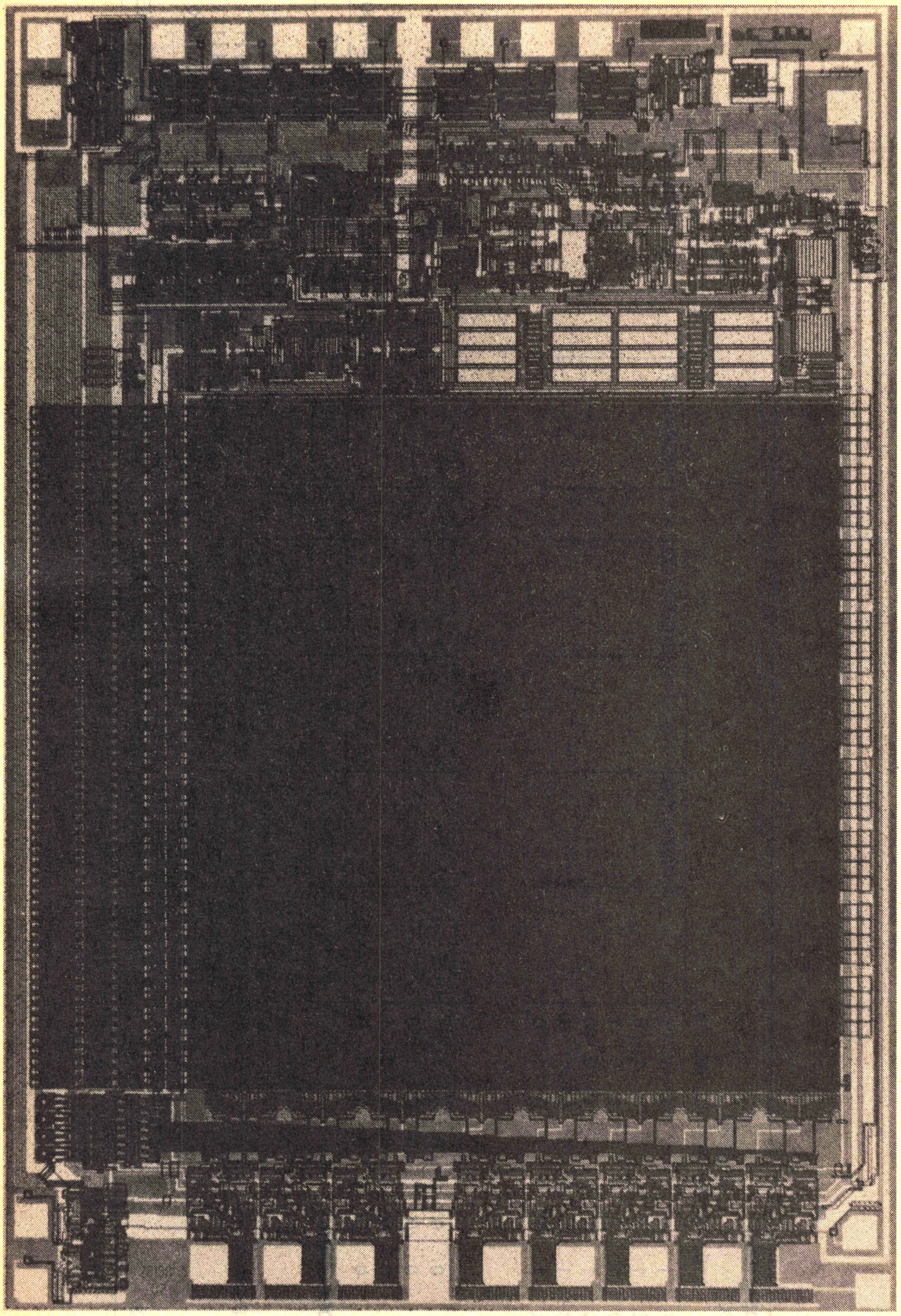
X-DECODER

HEX	A10	A9	A8	A7	A6	A5	A4
7F	1	1	1	1	1	1	1
7E	1	1	1	1	1	1	0
7D	1	1	1	1	1	0	1
7C	1	1	1	1	1	0	0
7B	1	1	1	1	0	1	1
7A	1	1	1	1	0	1	0
⋮				⋮	⋮		
3	0	0	0	0	0	1	1
2	0	0	0	0	0	1	0
1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0

Y-DECODER

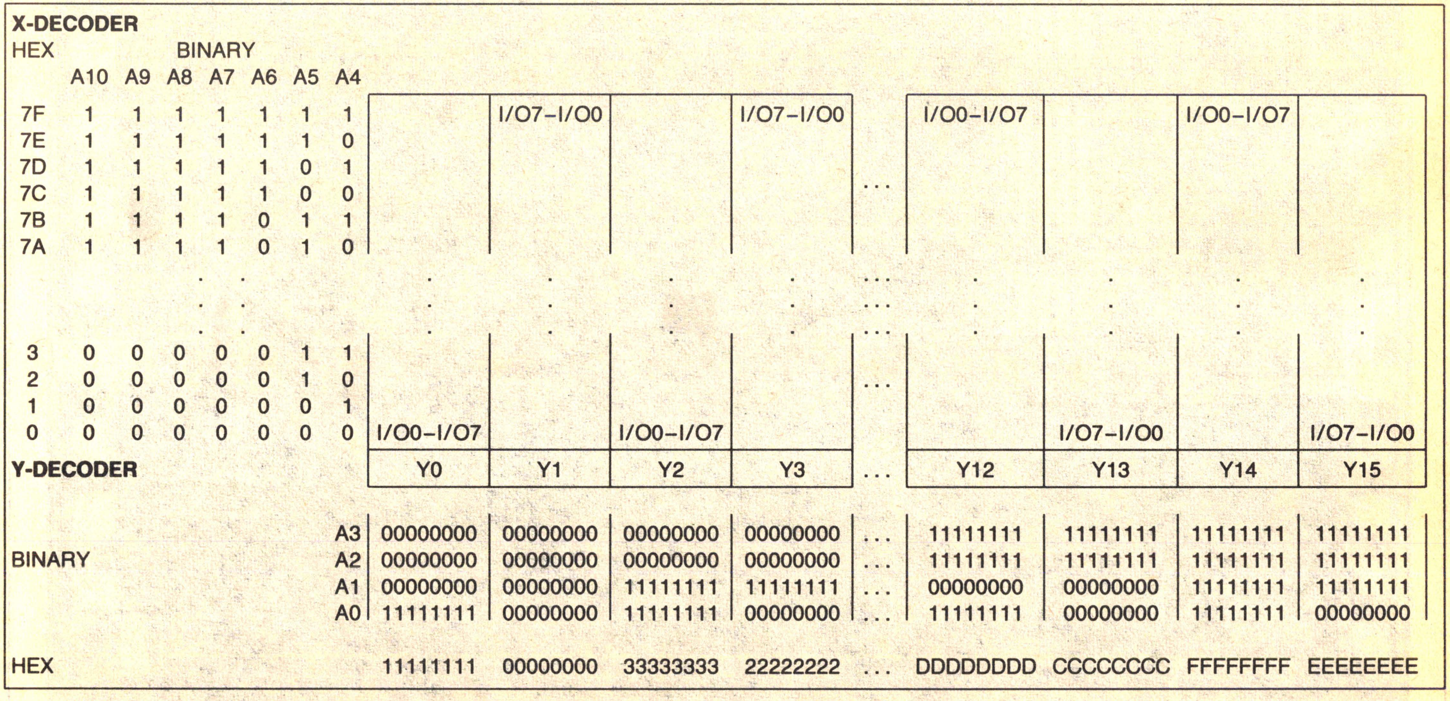
		Y0	Y1	Y2	Y3	…	Y12	Y13	Y14	Y15
BINARY	A3	11111111	11111111	11111111	11111111	…	00000000	00000000	00000000	00000000
	A2	11111111	11111111	11111111	11111111	…	00000000	00000000	00000000	00000000
	A1	11111111	11111111	00000000	00000000	…	11111111	11111111	00000000	00000000
	A0	11111111	00000000	11111111	00000000	…	11111111	00000000	11111111	00000000
HEX		FFFFFFFF	EEEEEEEE	DDDDDDDD	CCCCCCCC	…	33333333	22222222	11111111	00000000

2816A Bit Map



293001-12

2816A Die Photograph



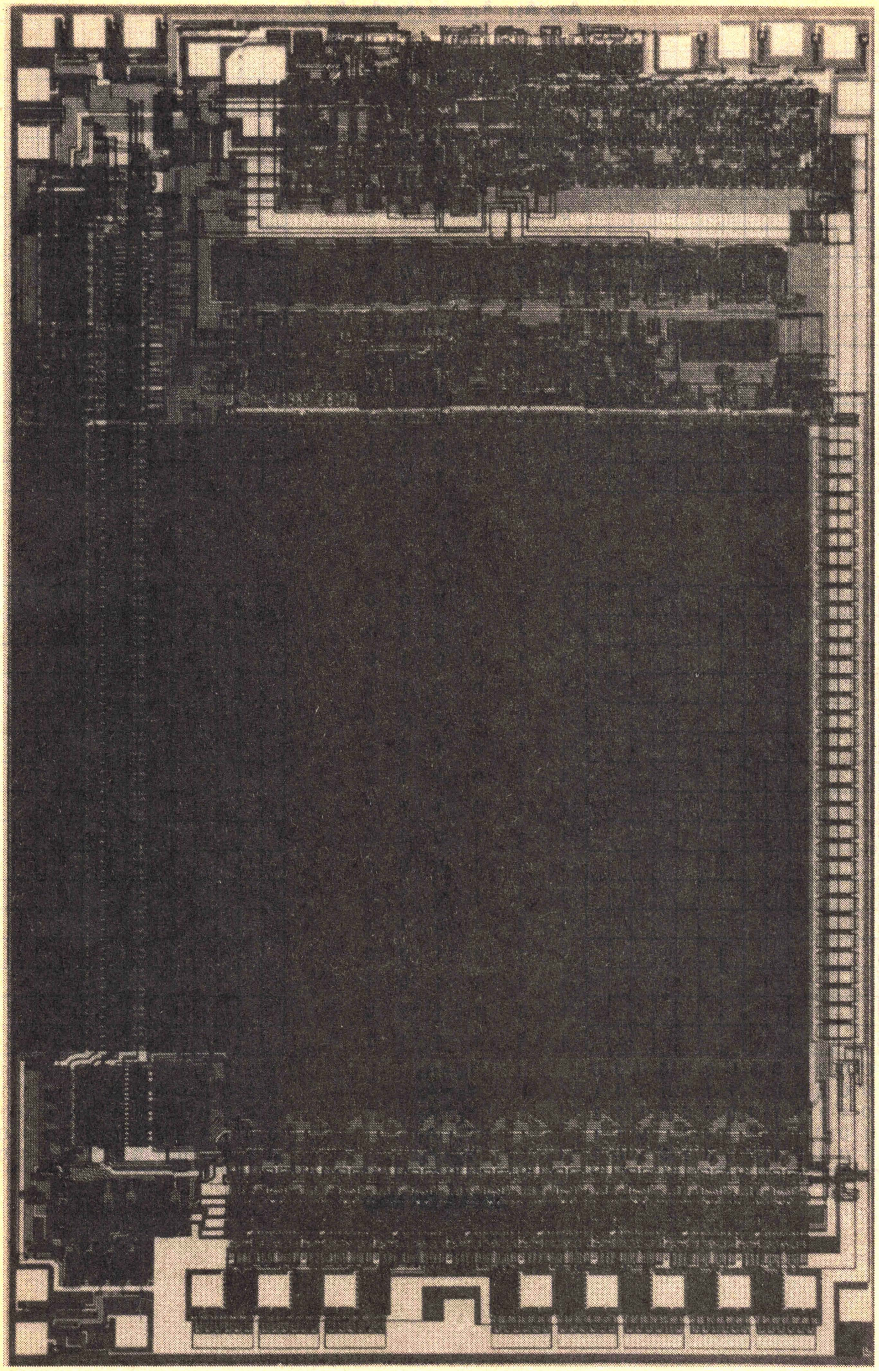
X-DECODER

HEX	A10	A9	A8	A7	A6	A5	A4
7F	1	1	1	1	1	1	1
7E	1	1	1	1	1	1	0
7D	1	1	1	1	1	0	1
7C	1	1	1	1	1	0	0
7B	1	1	1	1	0	1	1
7A	1	1	1	1	0	1	0
.				.	.		
3	0	0	0	0	0	1	1
2	0	0	0	0	0	1	0
1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0

Y-DECODER

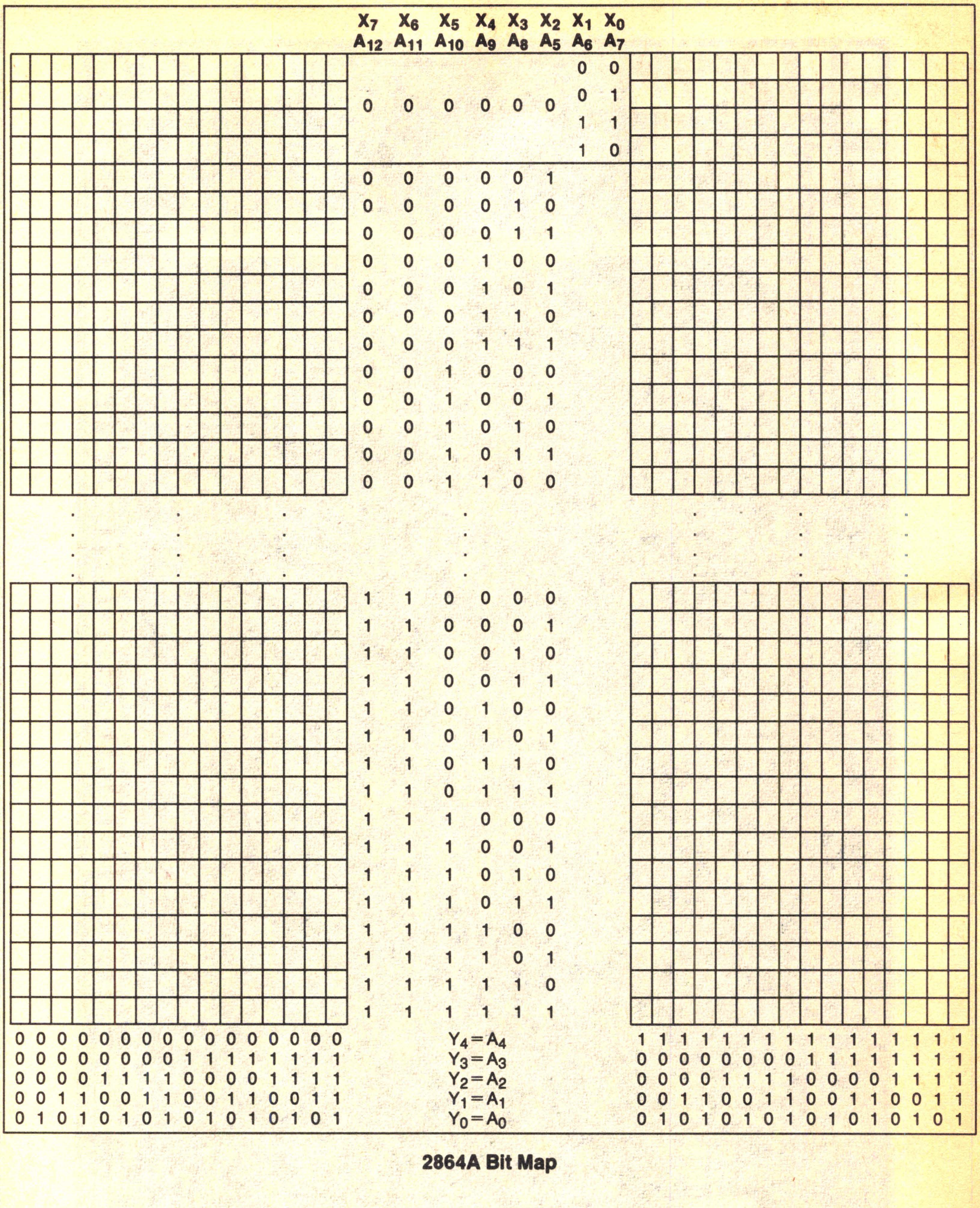
	Y0	Y1	Y2	Y3	...	Y12	Y13	Y14	Y15
BINARY A3	00000000	00000000	00000000	00000000	...	11111111	11111111	11111111	11111111
A2	00000000	00000000	00000000	00000000	...	11111111	11111111	11111111	11111111
A1	00000000	00000000	11111111	11111111	...	00000000	00000000	11111111	11111111
A0	11111111	00000000	11111111	00000000	...	11111111	00000000	11111111	00000000
HEX	11111111	00000000	33333333	22222222	...	DDDDDDDD	CCCCCCCC	FFFFFFFF	EEEEEEEE

2817A Bit Map



293001-13

2817A Die Photograph


X7 A12
X6 A11
X5 A10
X4 A9
X3 A8
X2 A5
X1 A6
X0 A7
0 0
0 1
1 1
1 0
0 0 0 0 0 0
0 0 0 0 0 1
0 0 0 0 1 0
0 0 0 0 1 1
0 0 0 1 0 0
0 0 0 1 0 1
0 0 0 1 1 0
0 0 0 1 1 1
0 0 1 0 0 0
0 0 1 0 0 1
0 0 1 0 1 0
0 0 1 0 1 1
0 0 1 1 0 0
1 1 0 0 0 0
1 1 0 0 0 1
1 1 0 0 1 0
1 1 0 0 1 1
1 1 0 1 0 0
1 1 0 1 0 1
1 1 0 1 1 0
1 1 0 1 1 1
1 1 1 0 0 0
1 1 1 0 0 1
1 1 1 0 1 0
1 1 1 0 1 1
1 1 1 1 0 0
1 1 1 1 0 1
1 1 1 1 1 0
1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Y4=A4
Y3=A3
Y2=A2
Y1=A1
Y0=A0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1

2864A Bit Map

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